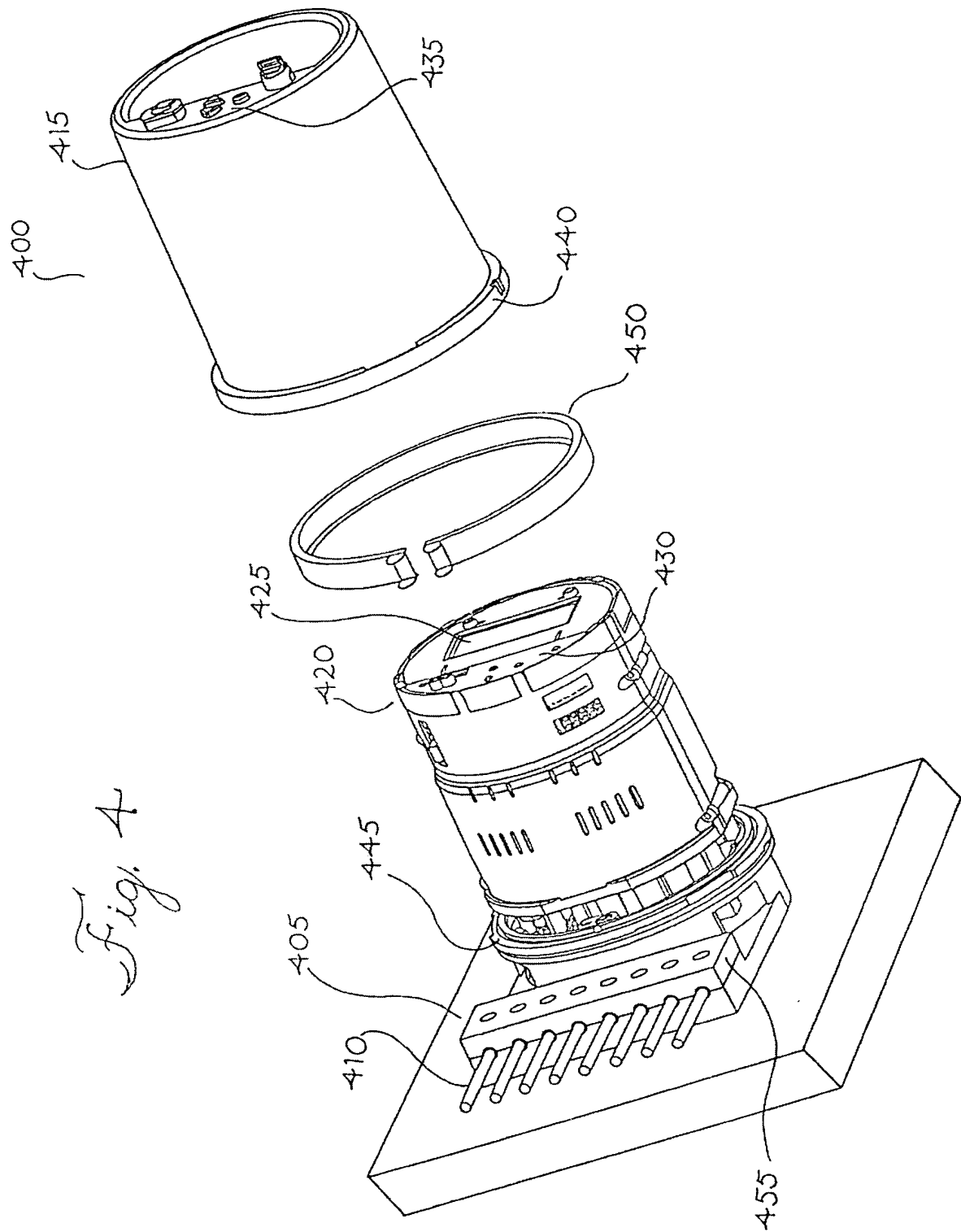
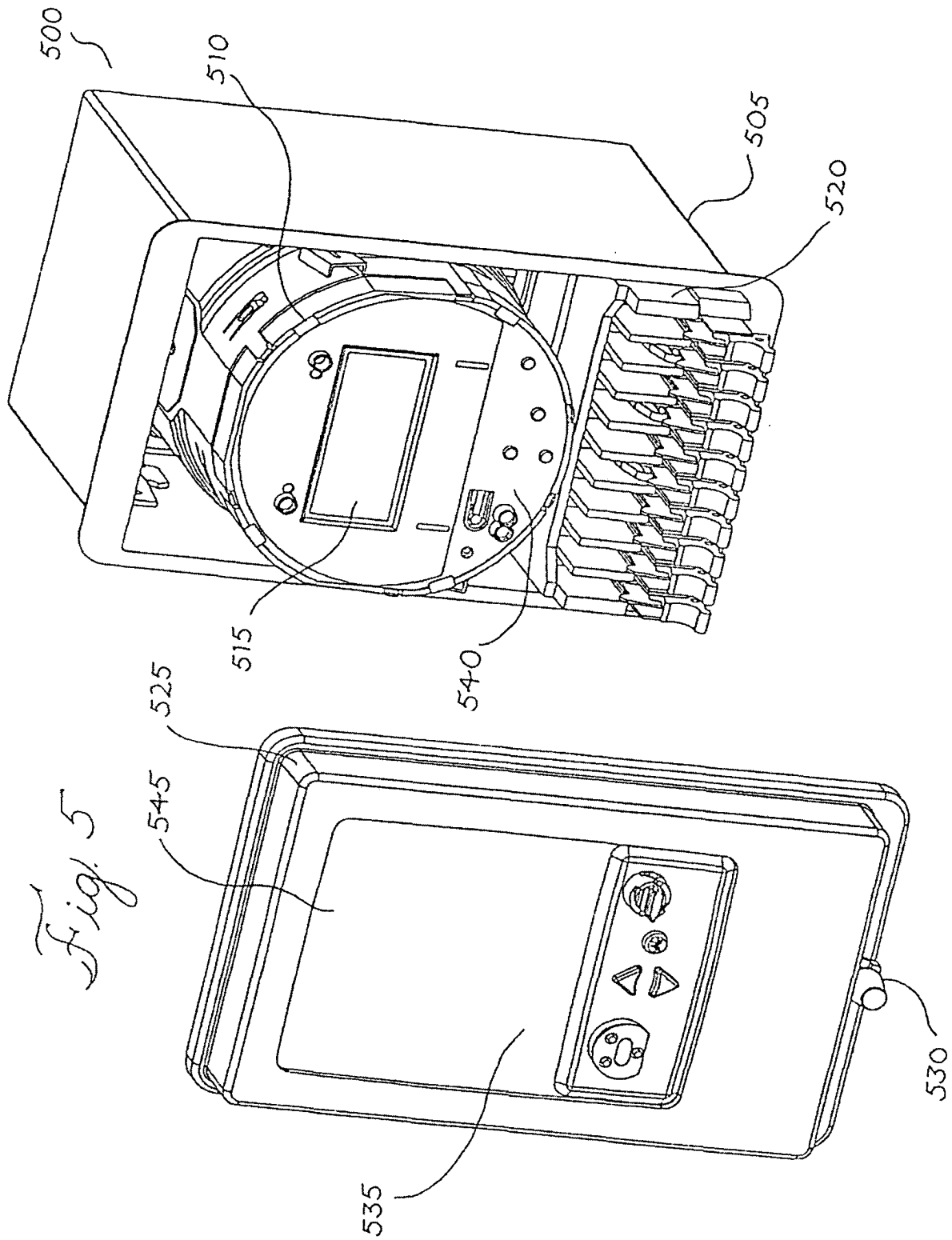
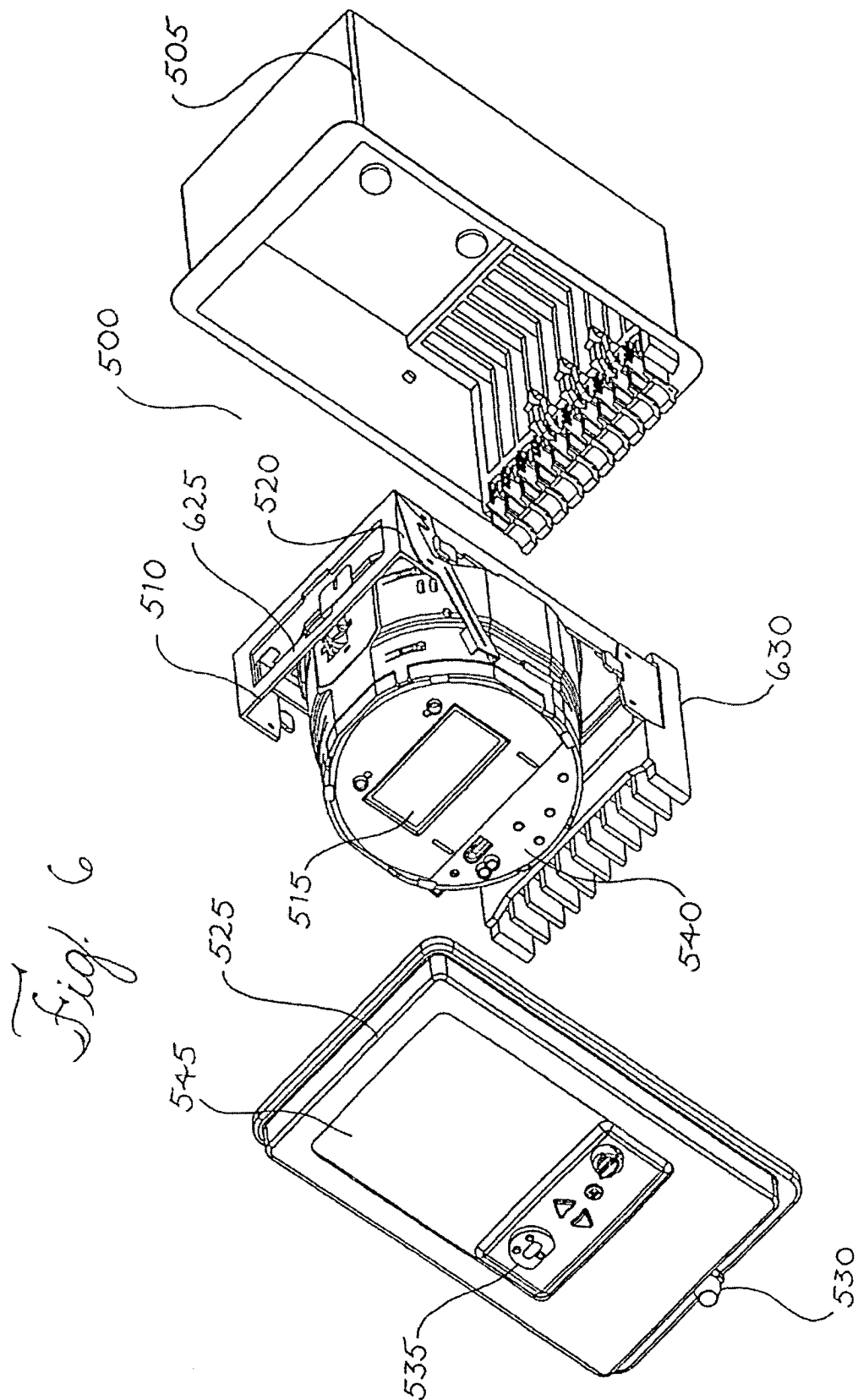


Fig. 3







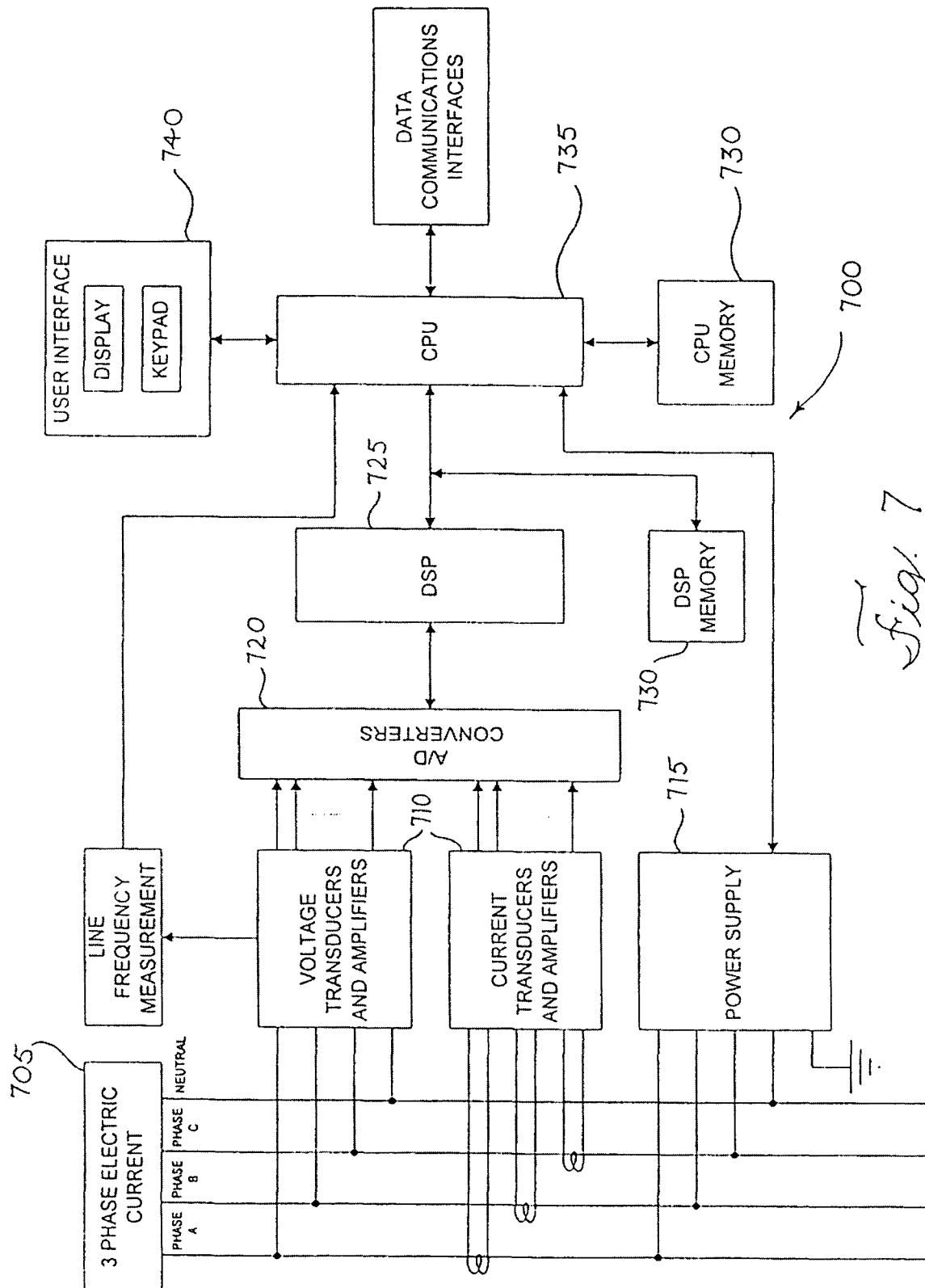


Fig. 7

700

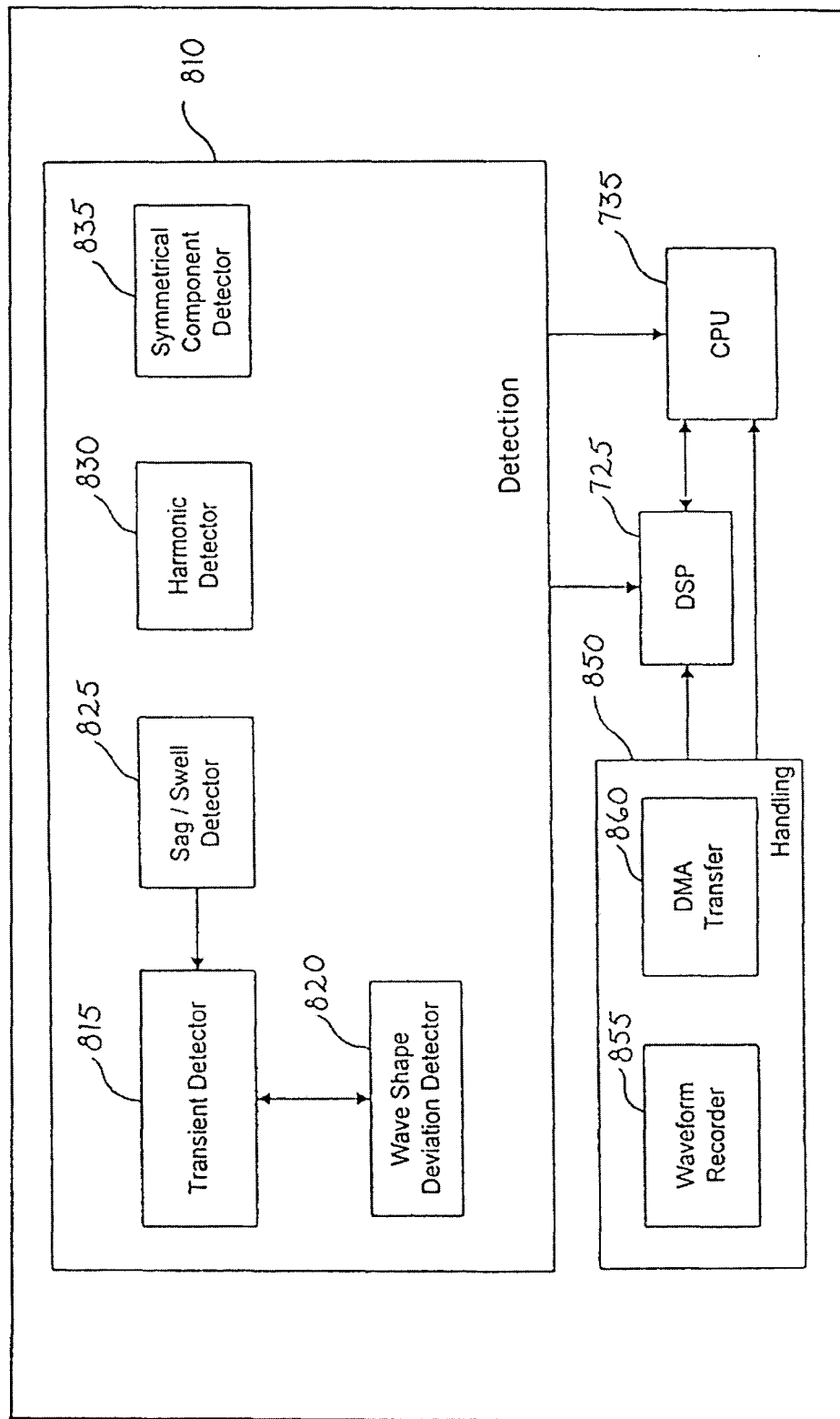


Fig. 8

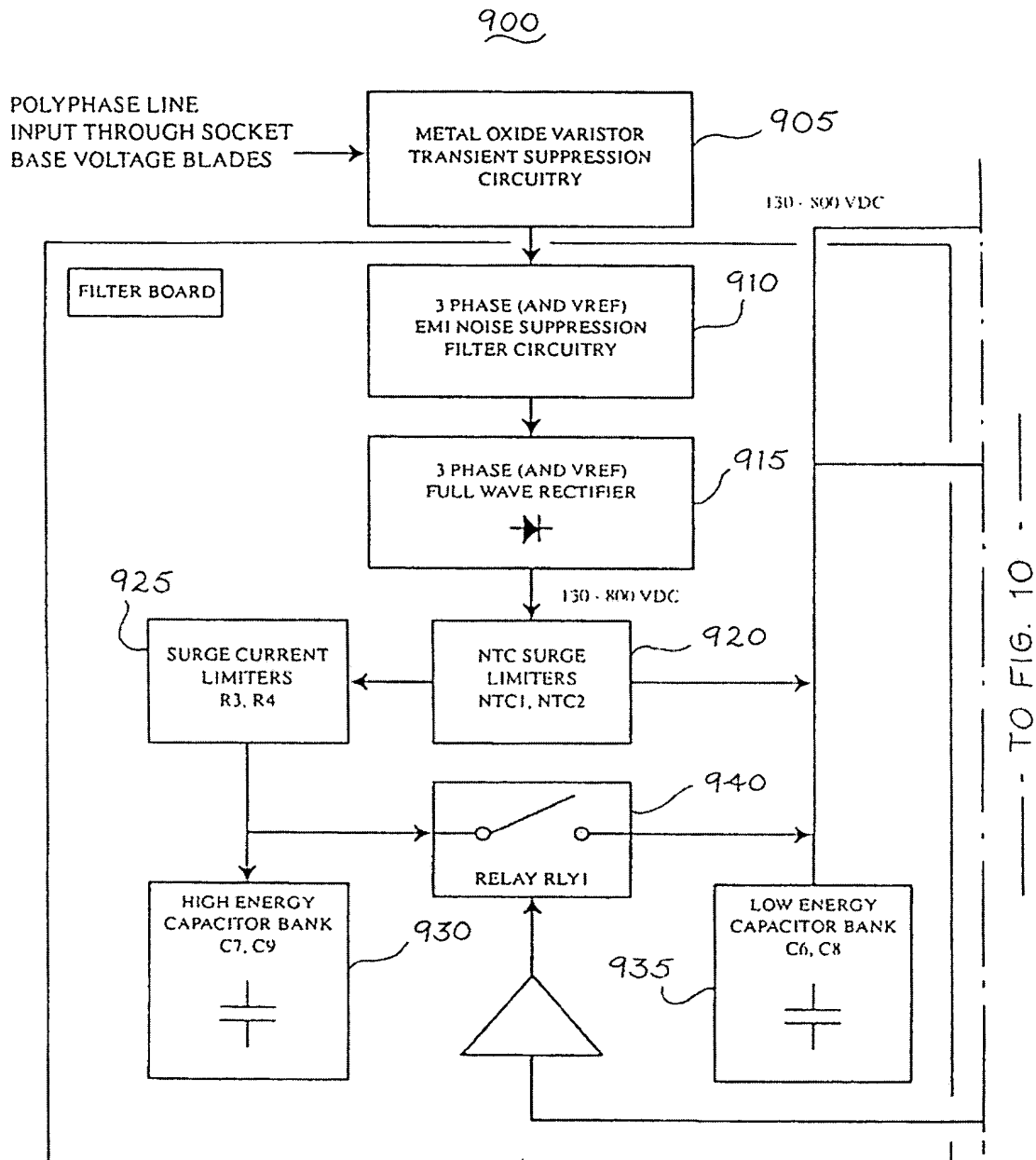


Fig. 9

(11/58)

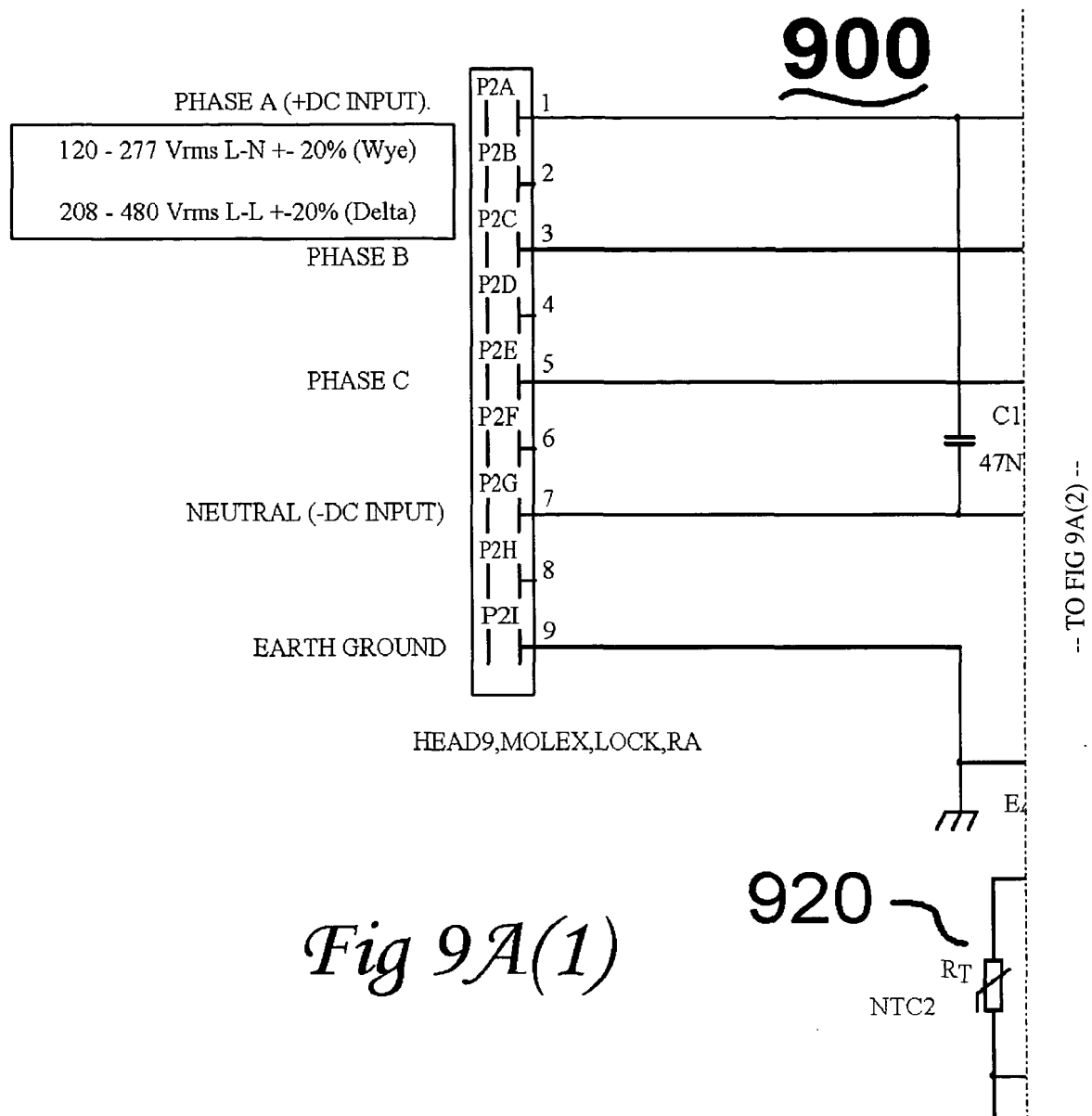


Fig. 9A(2) (12/58)

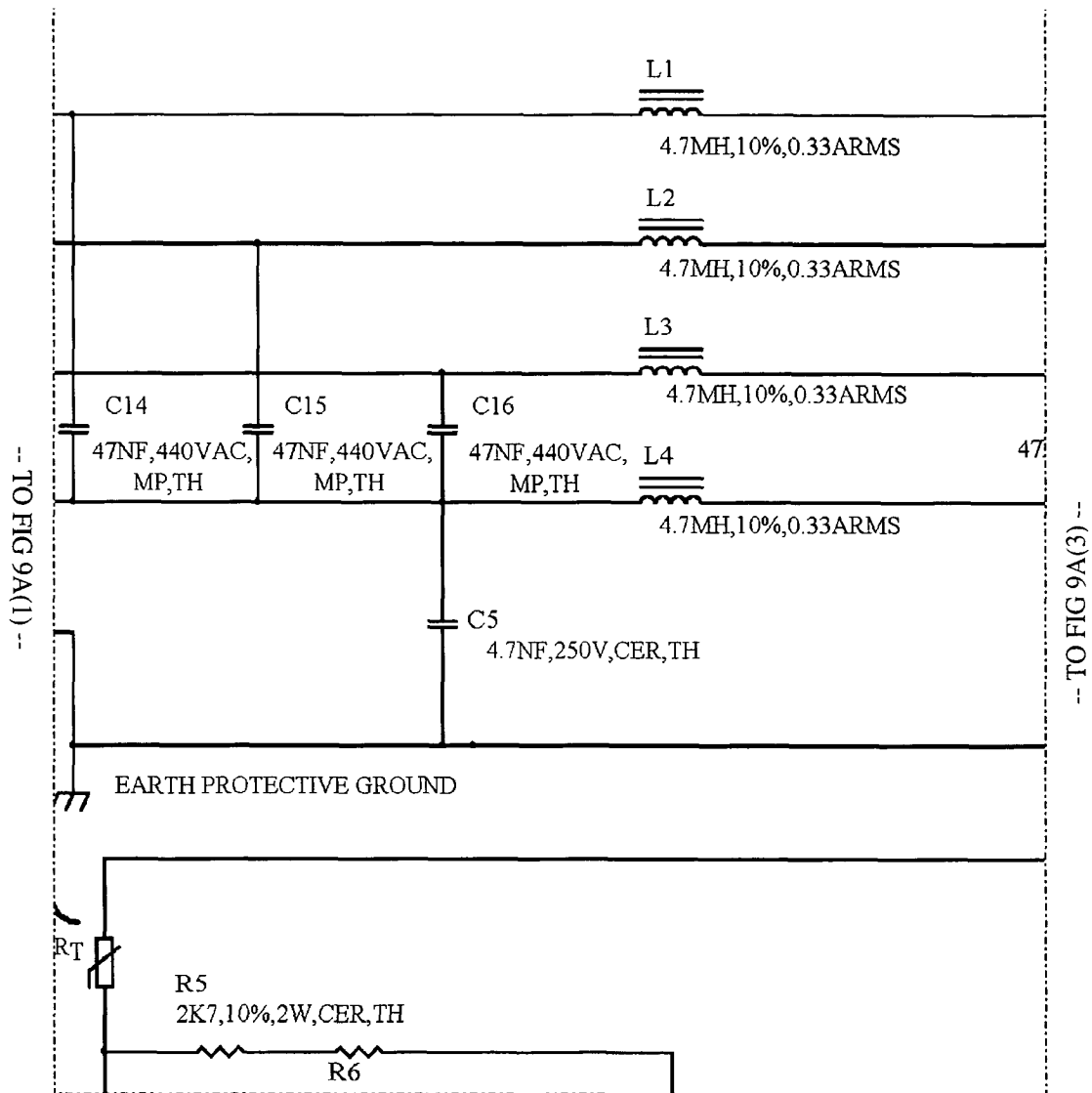


Fig. 9A(3) (13/58)

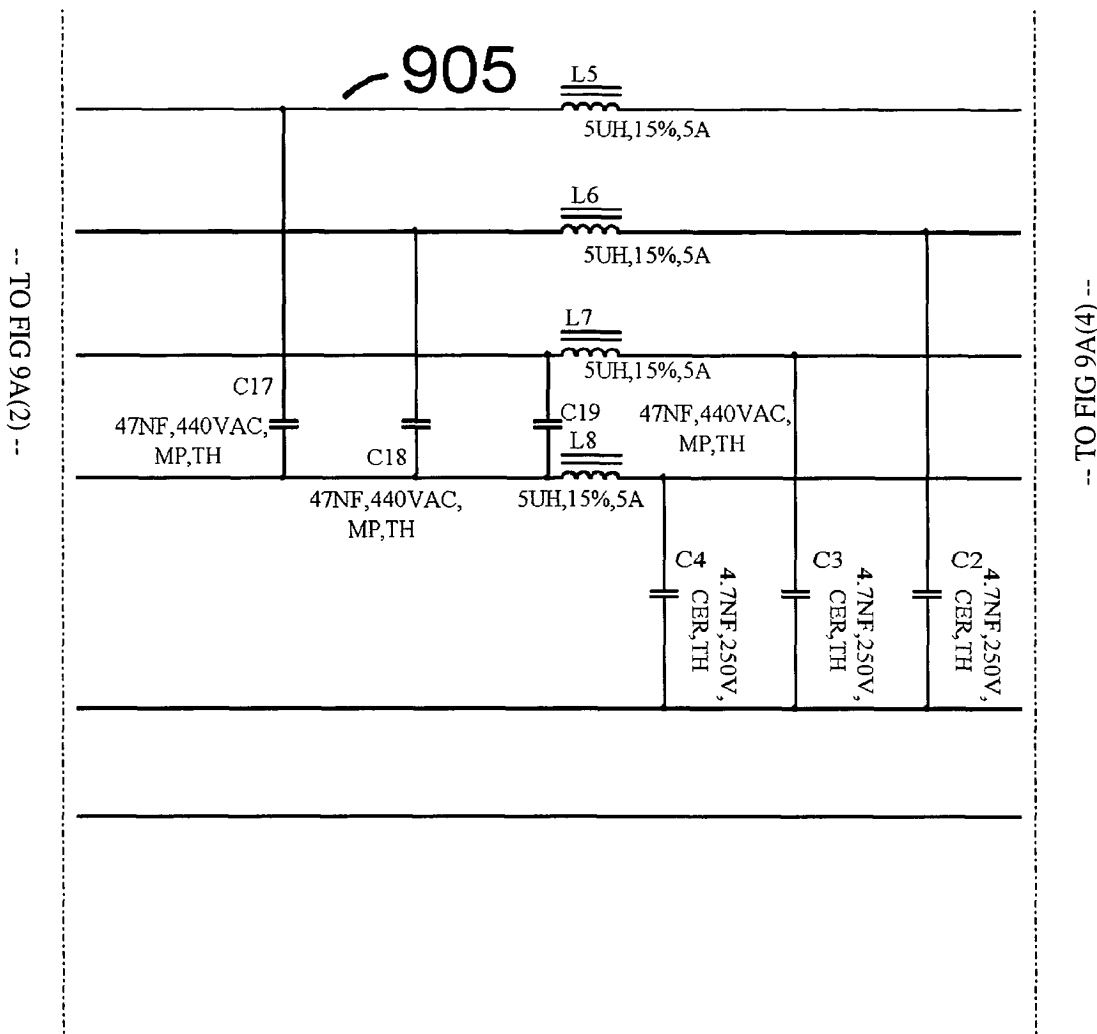


Fig. 9A(4) (14/58)

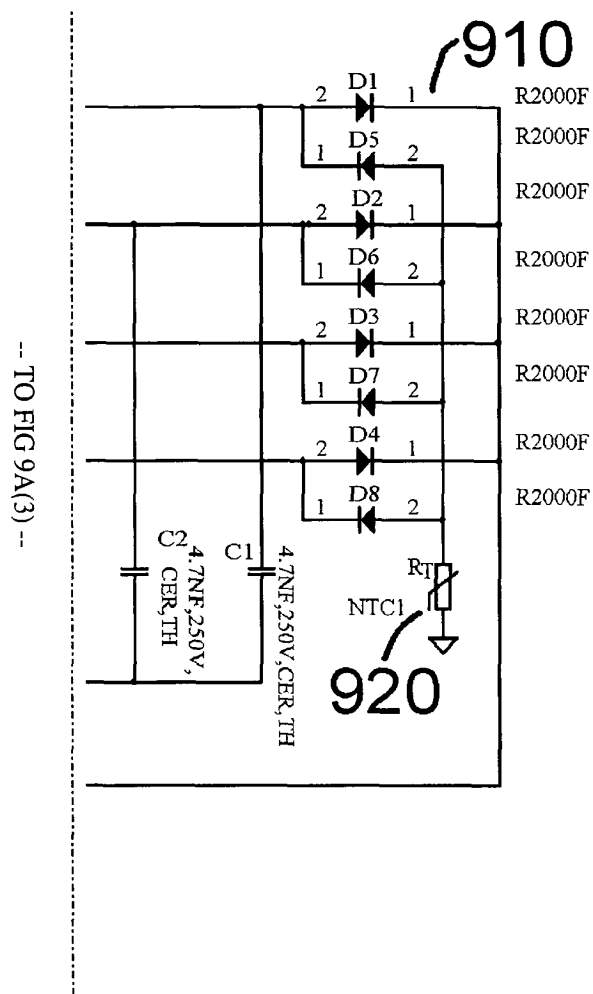


Fig. 9A(5) (15/58)

-- TO FIG 9A(1) --

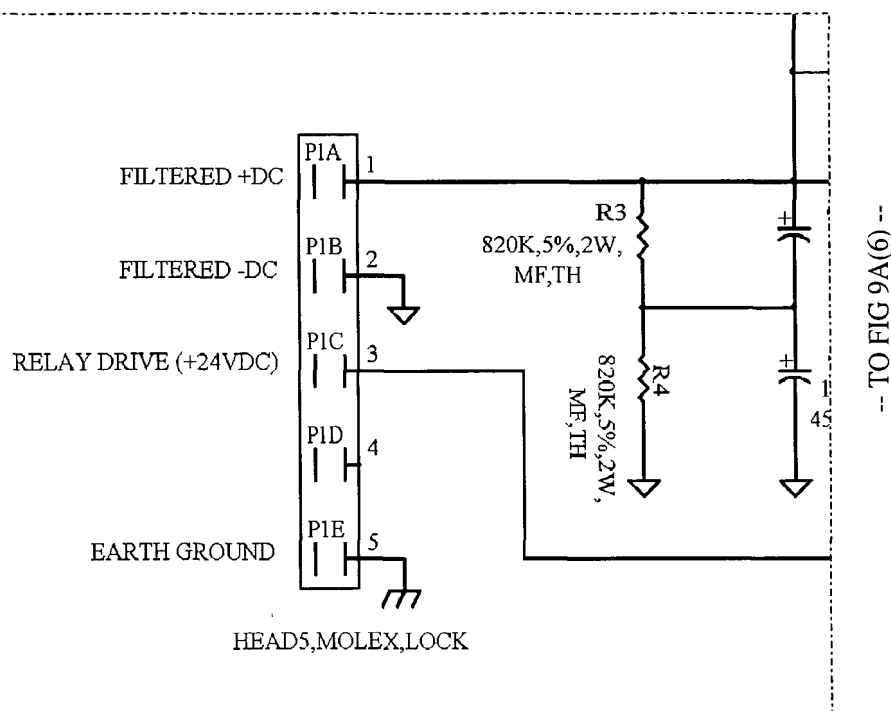
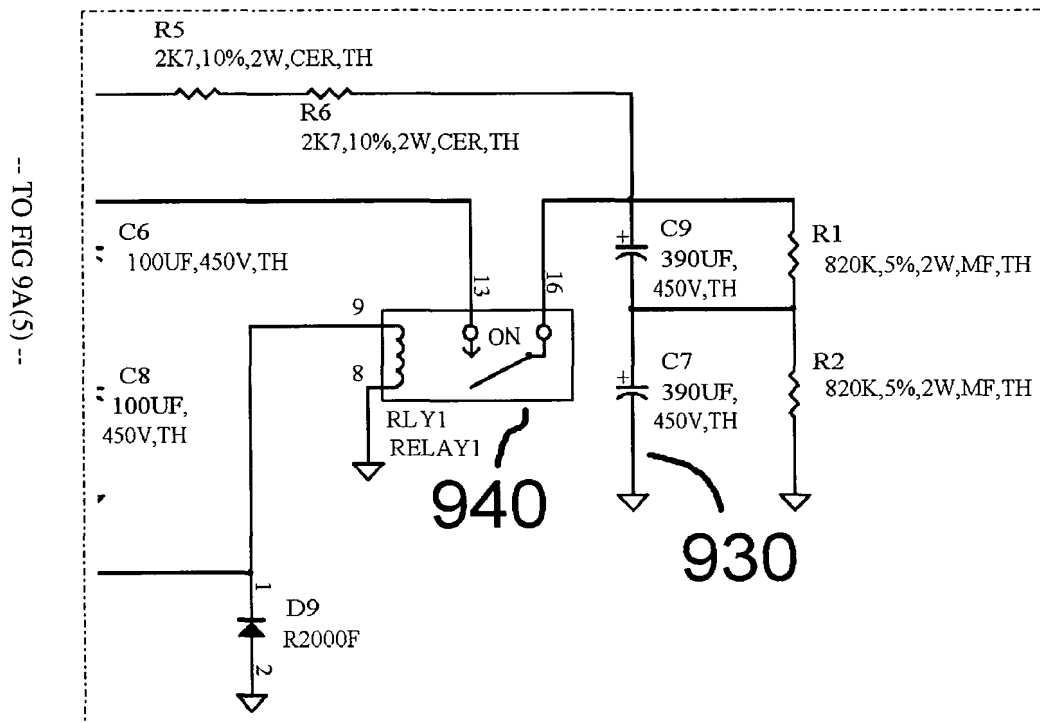


Fig. 9A(6) (16/58)

-- TO FIG 9A(2) --



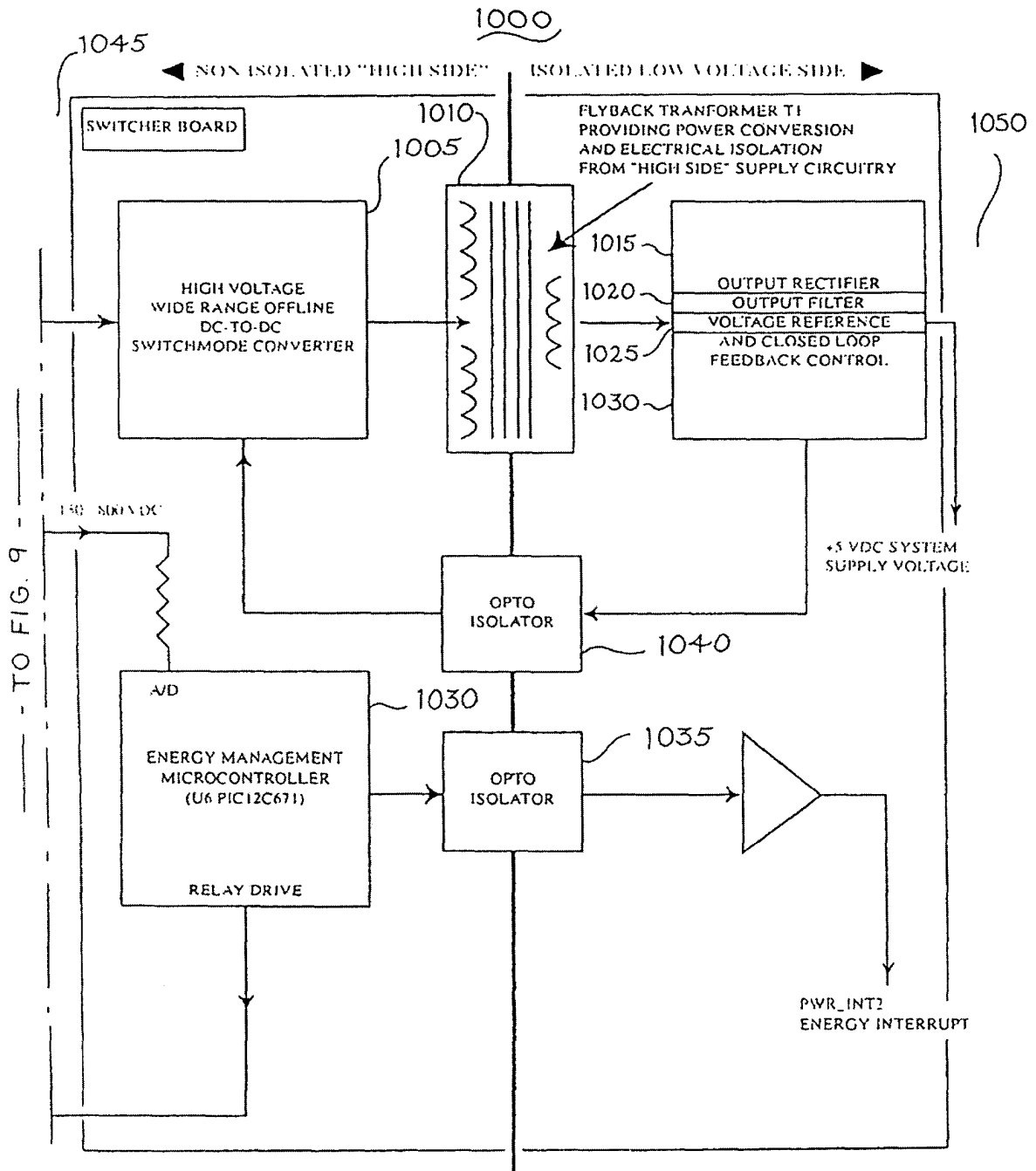


Fig. 10

Fig. 10A(1) (17/58)

Fig. 10A(2) (18/58)

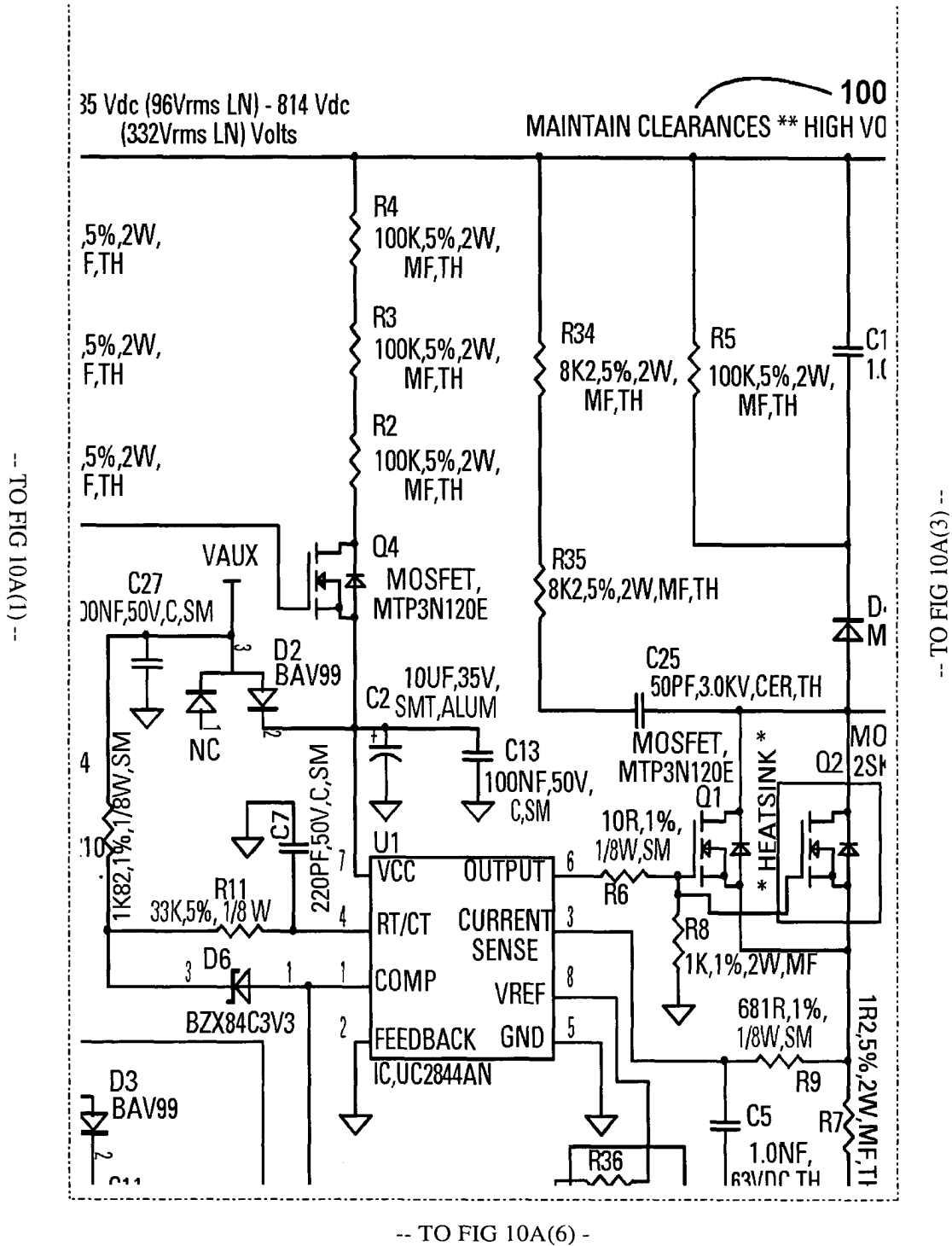


Fig. 10A(3) (19/58)

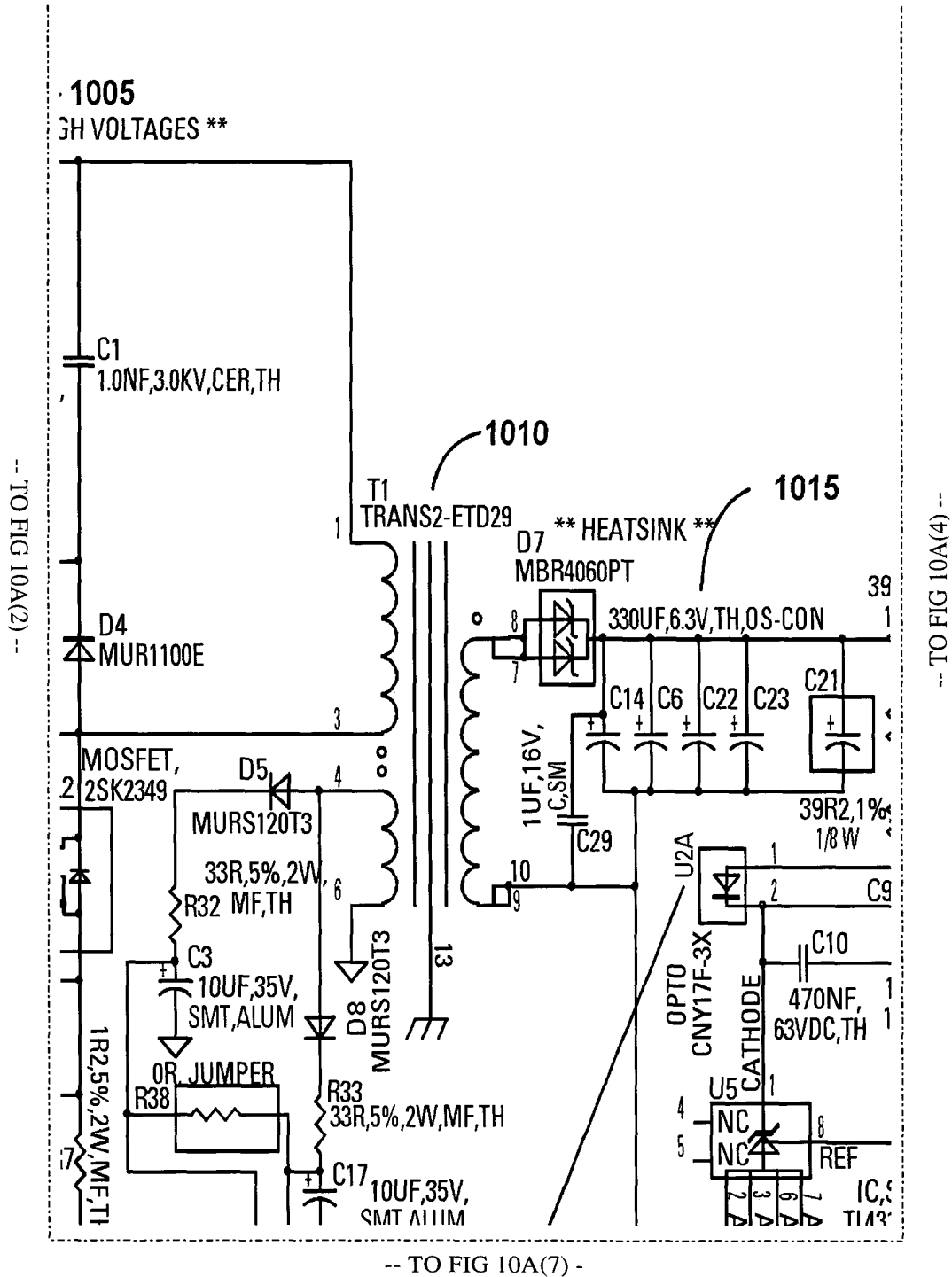
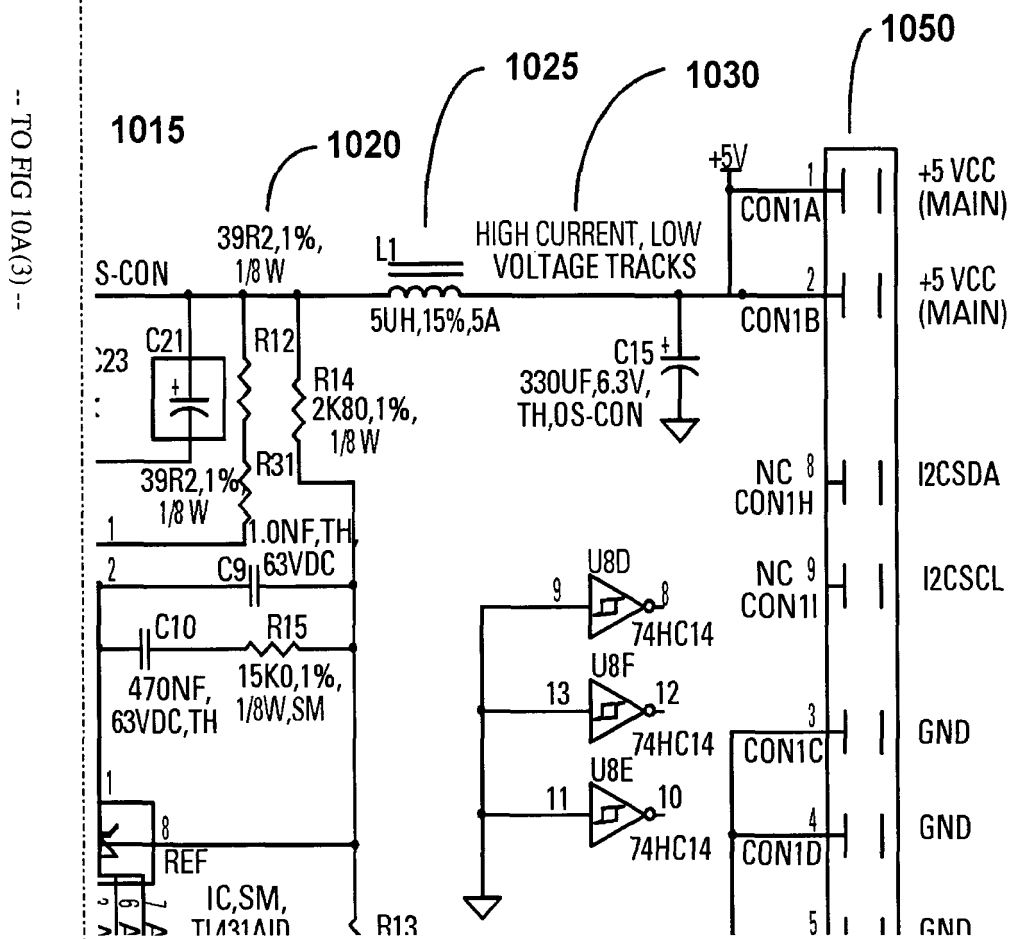


Fig. 10A(4) (20/58)



-- TO FIG 10A(8) -

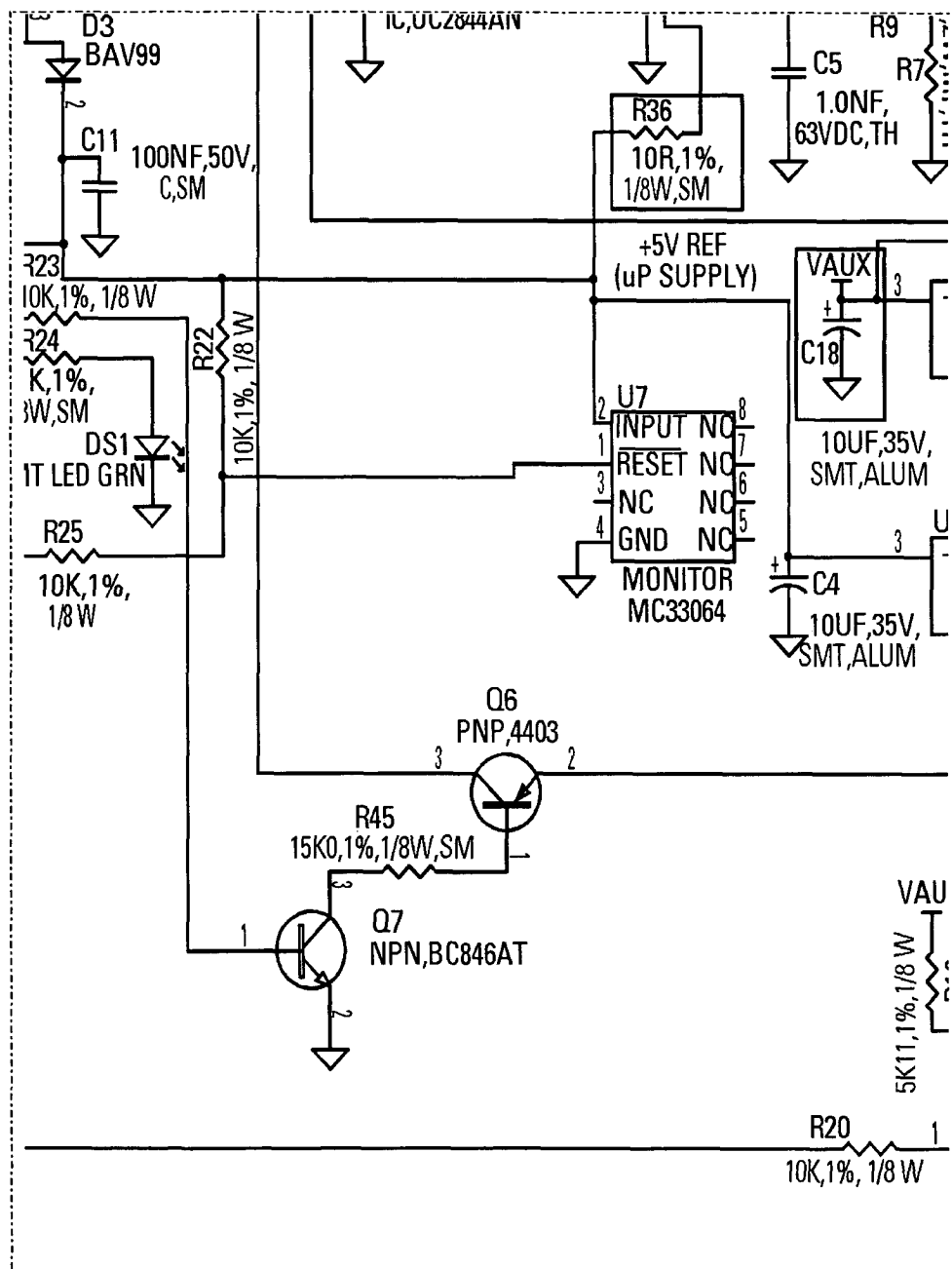
[illegible]

--- TO FIG 10A(6) ---

Fig. 10A(6) (22/58)

-- TO FIG 10A(2) -

-- TO FIG 10A(5) --



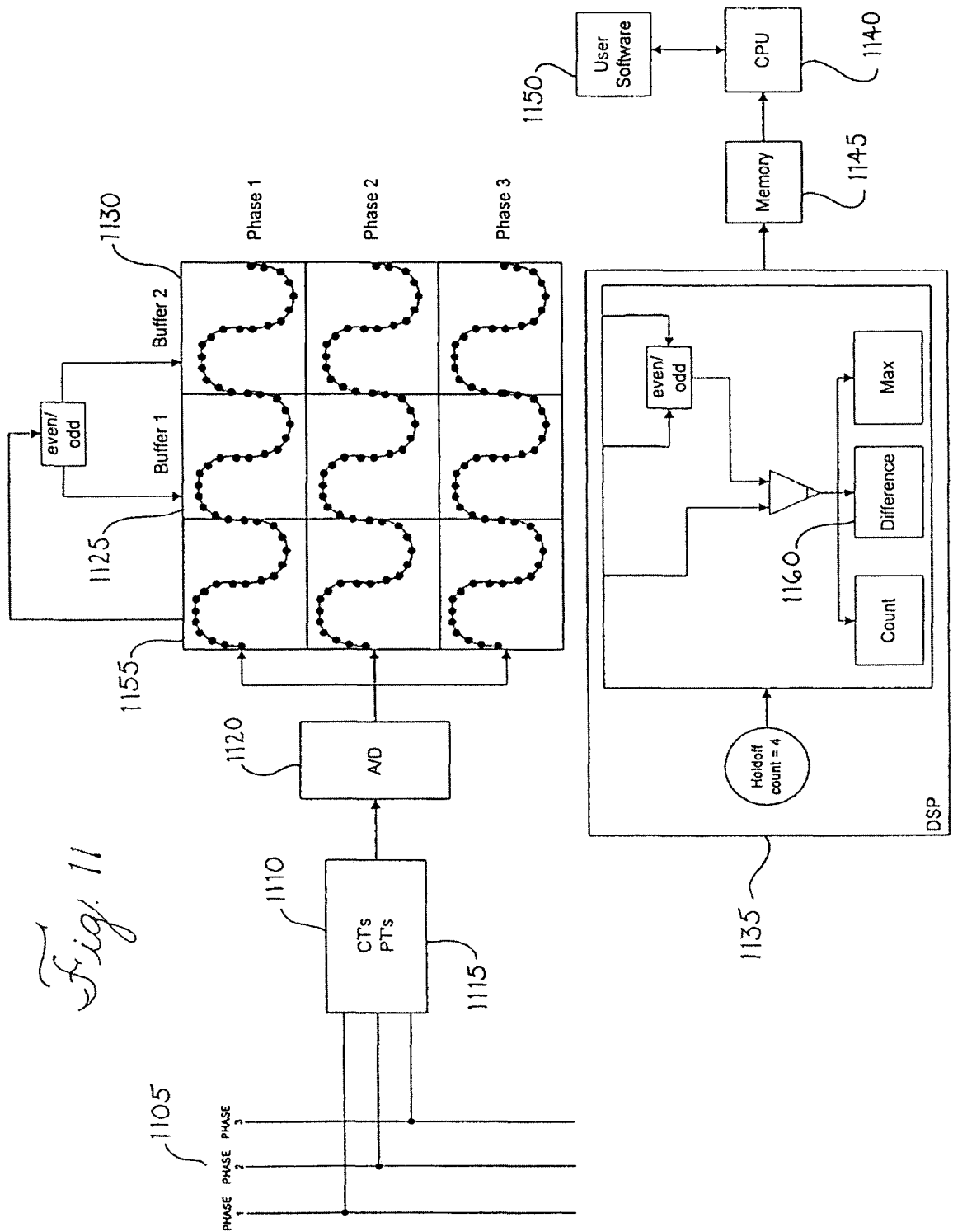
-- TO FIG 10A(7) --

-- TO FIG 10A(3) -

Fig. 10A(8) (24/58)

-- TO FIG 10A(4) -





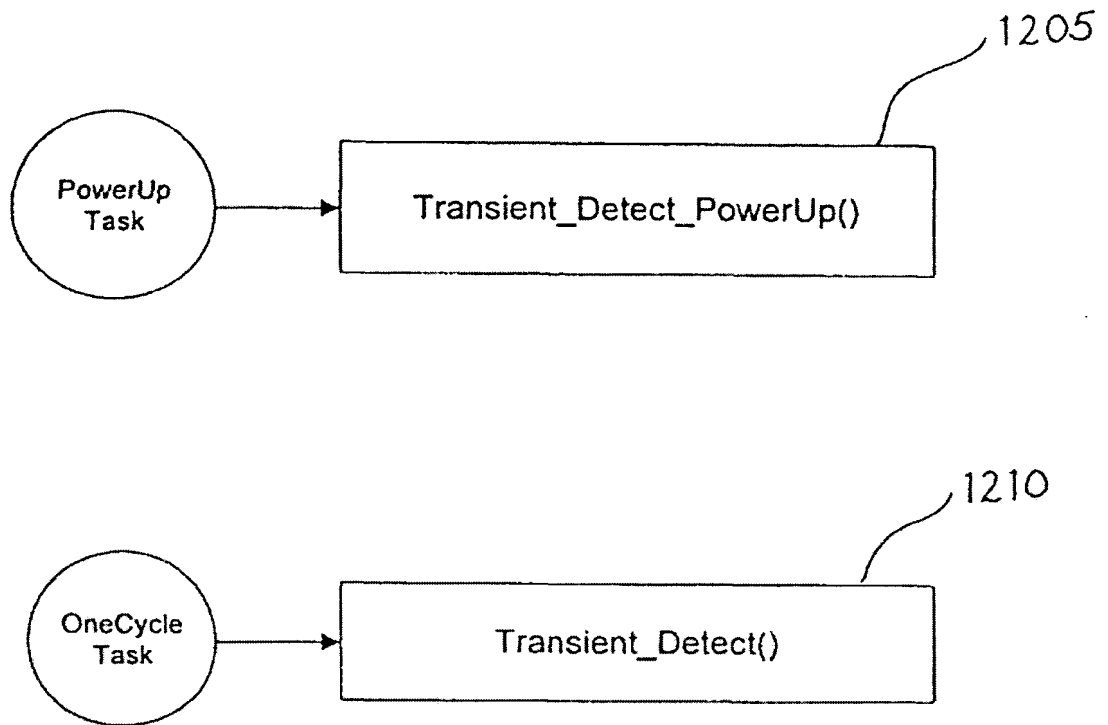


Fig. 12

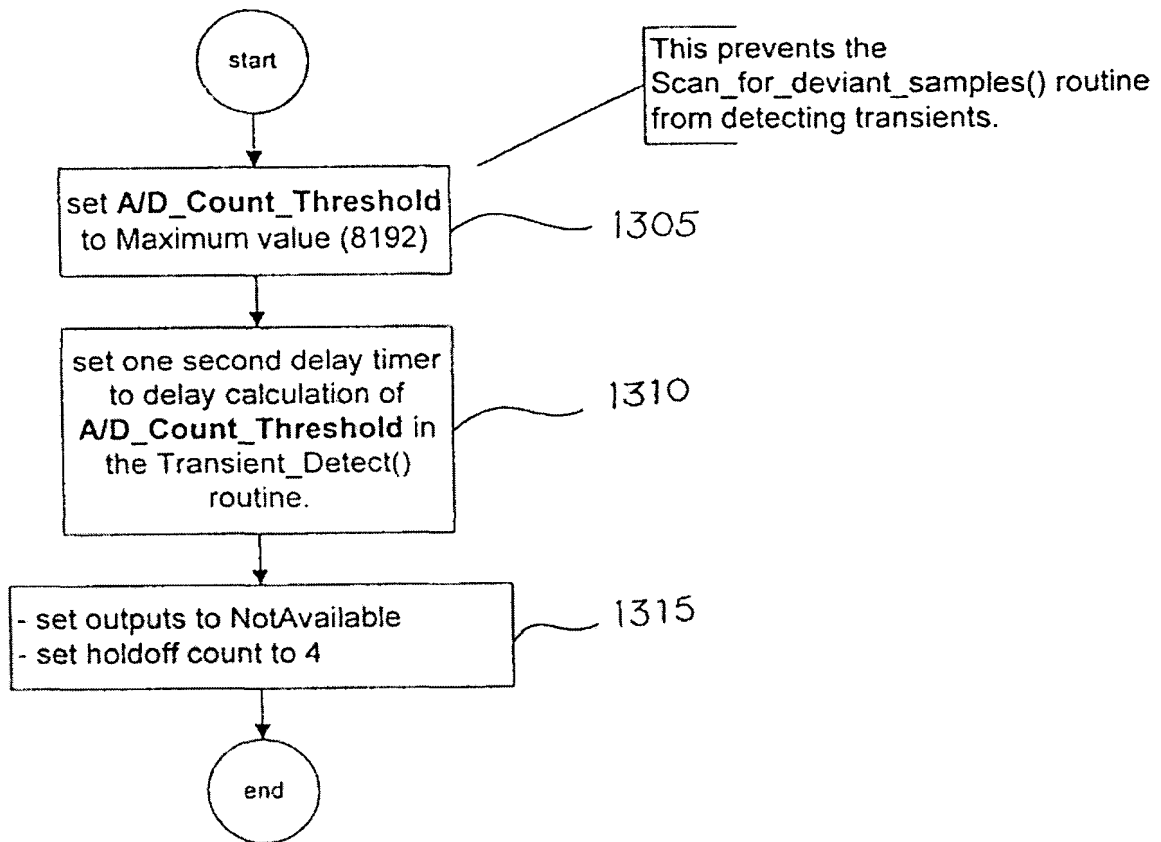
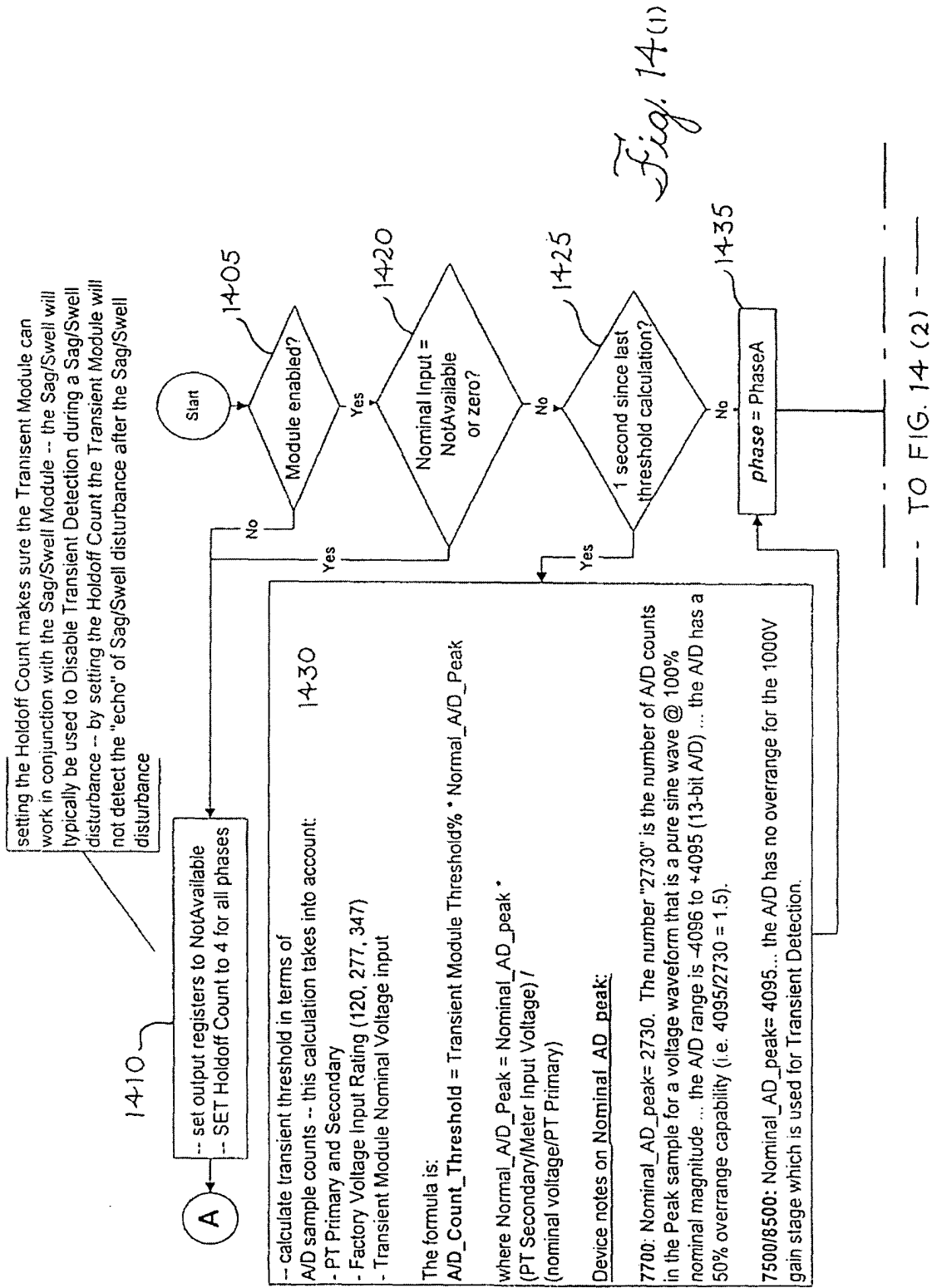


Fig. 13



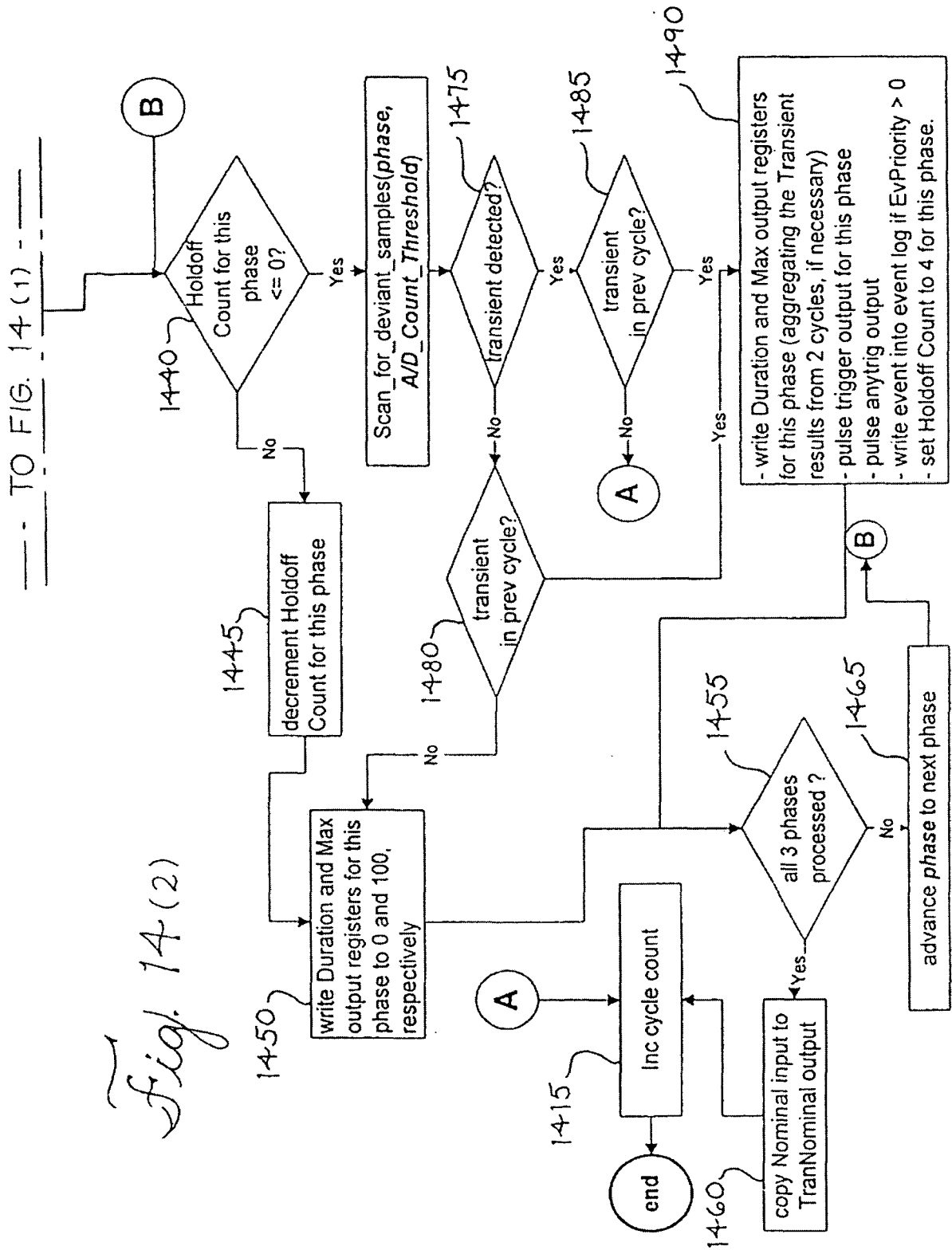
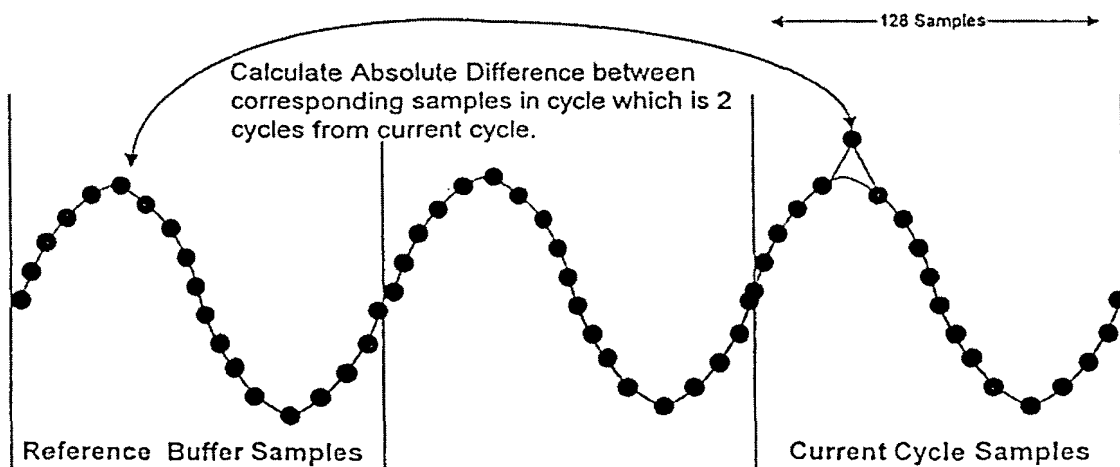
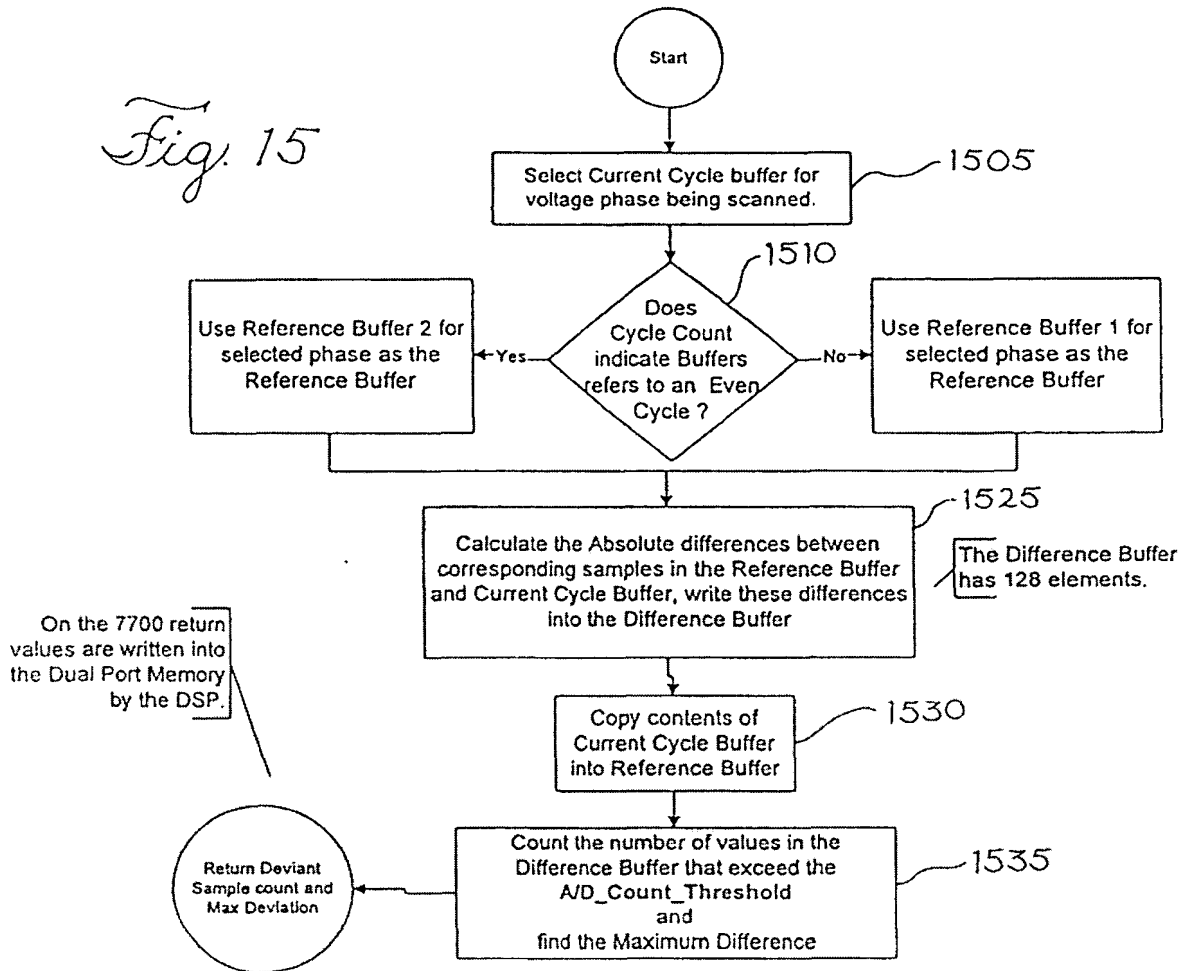


Fig. 15



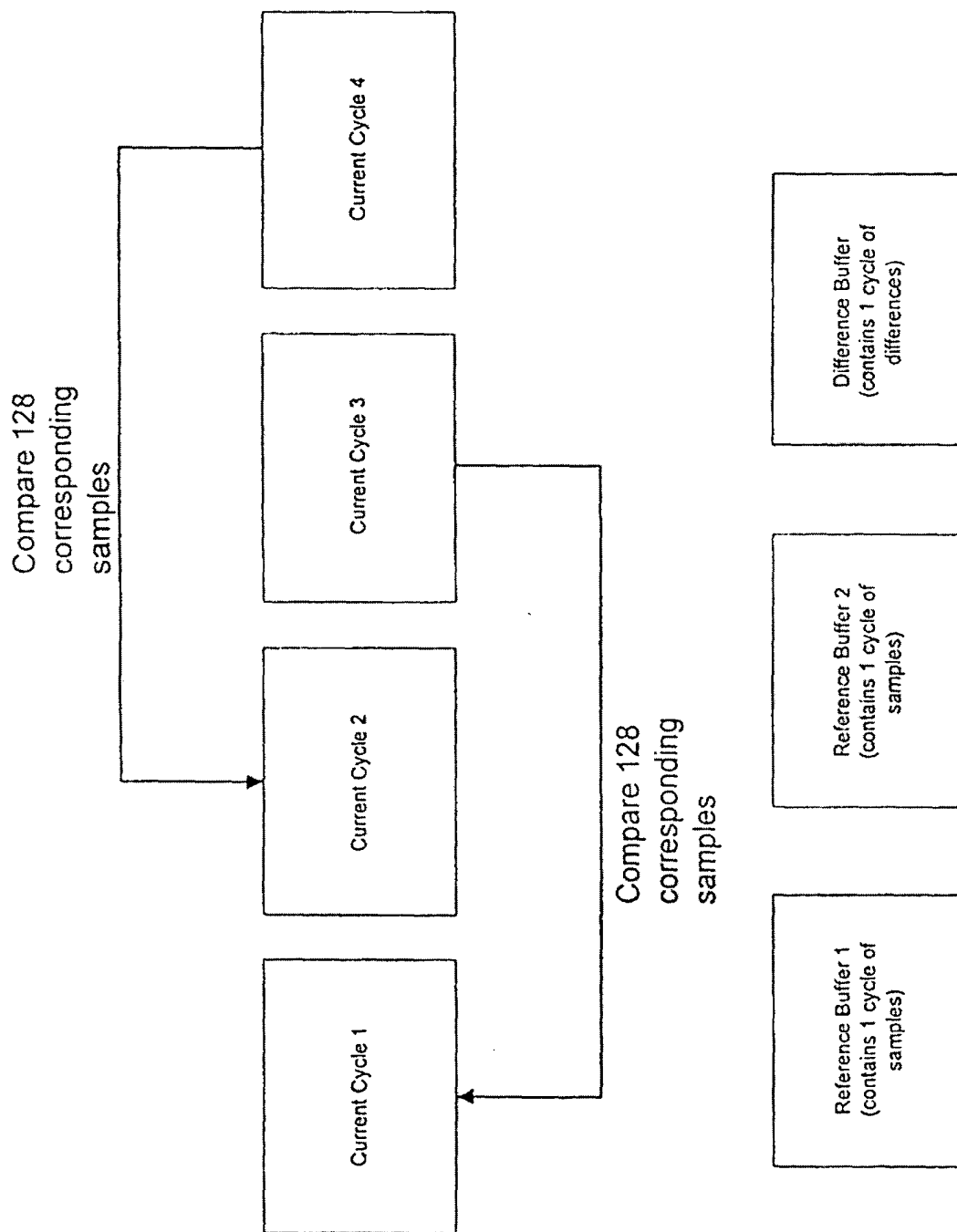


Fig. 16

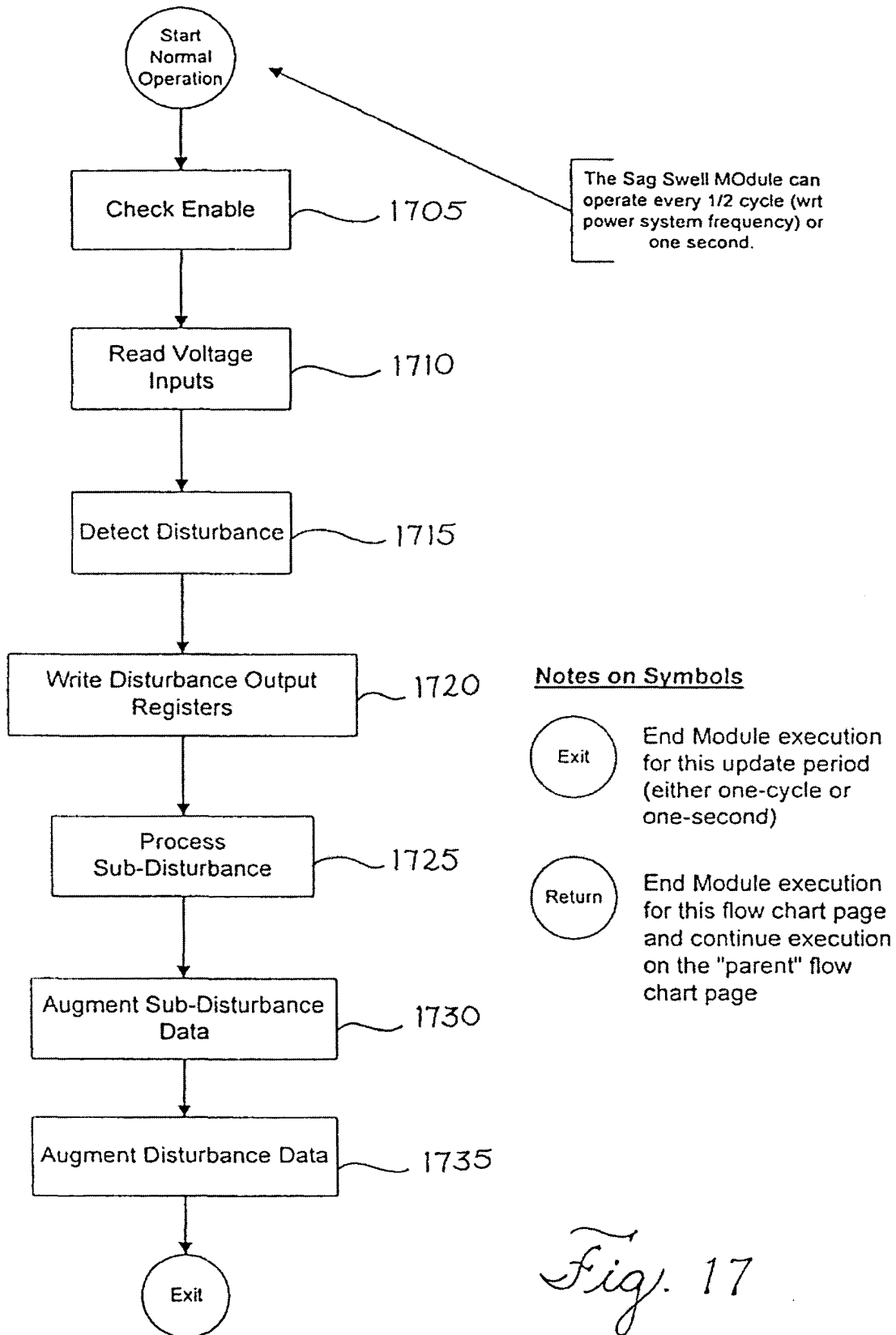


Fig. 17

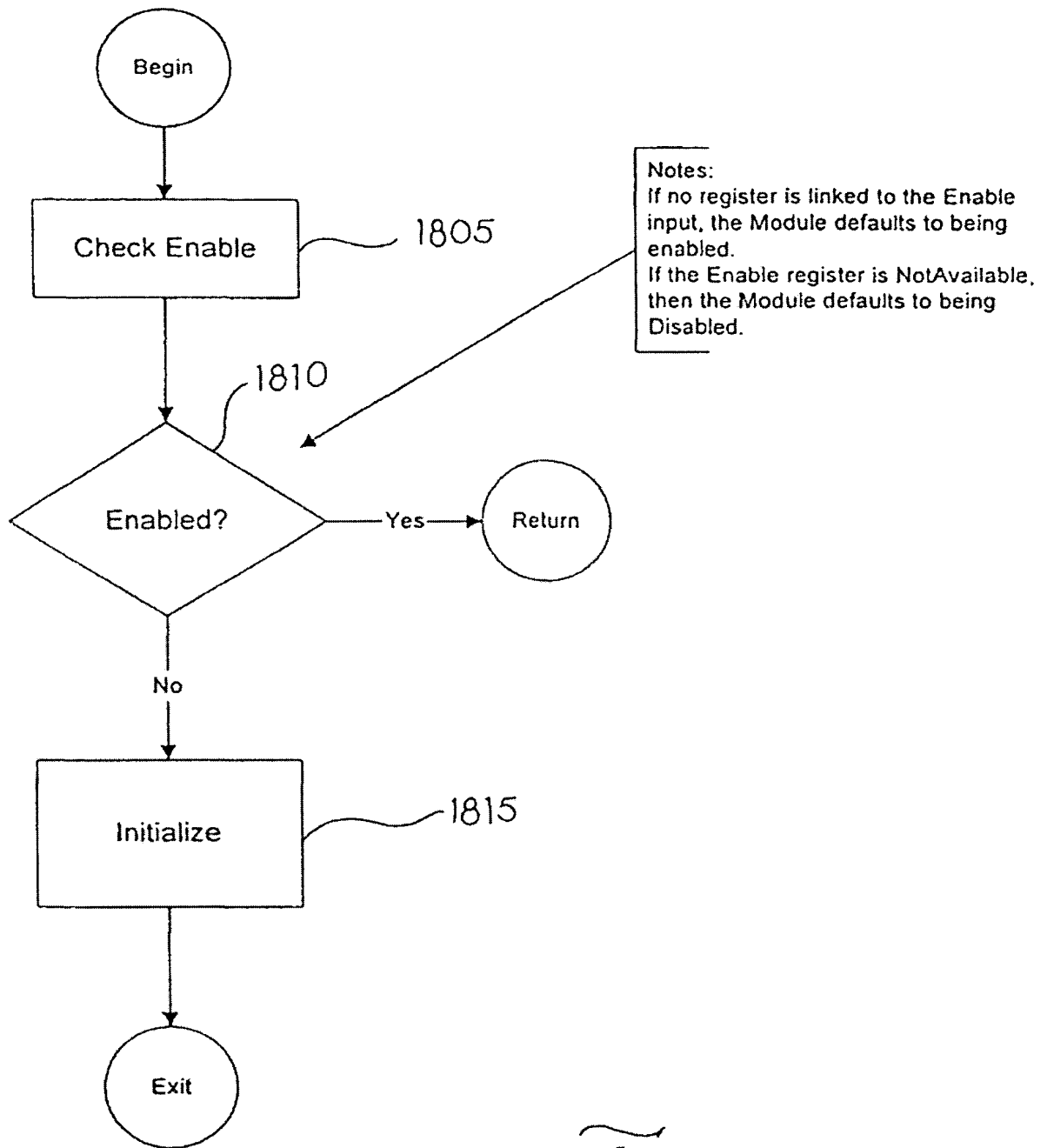


Fig. 18

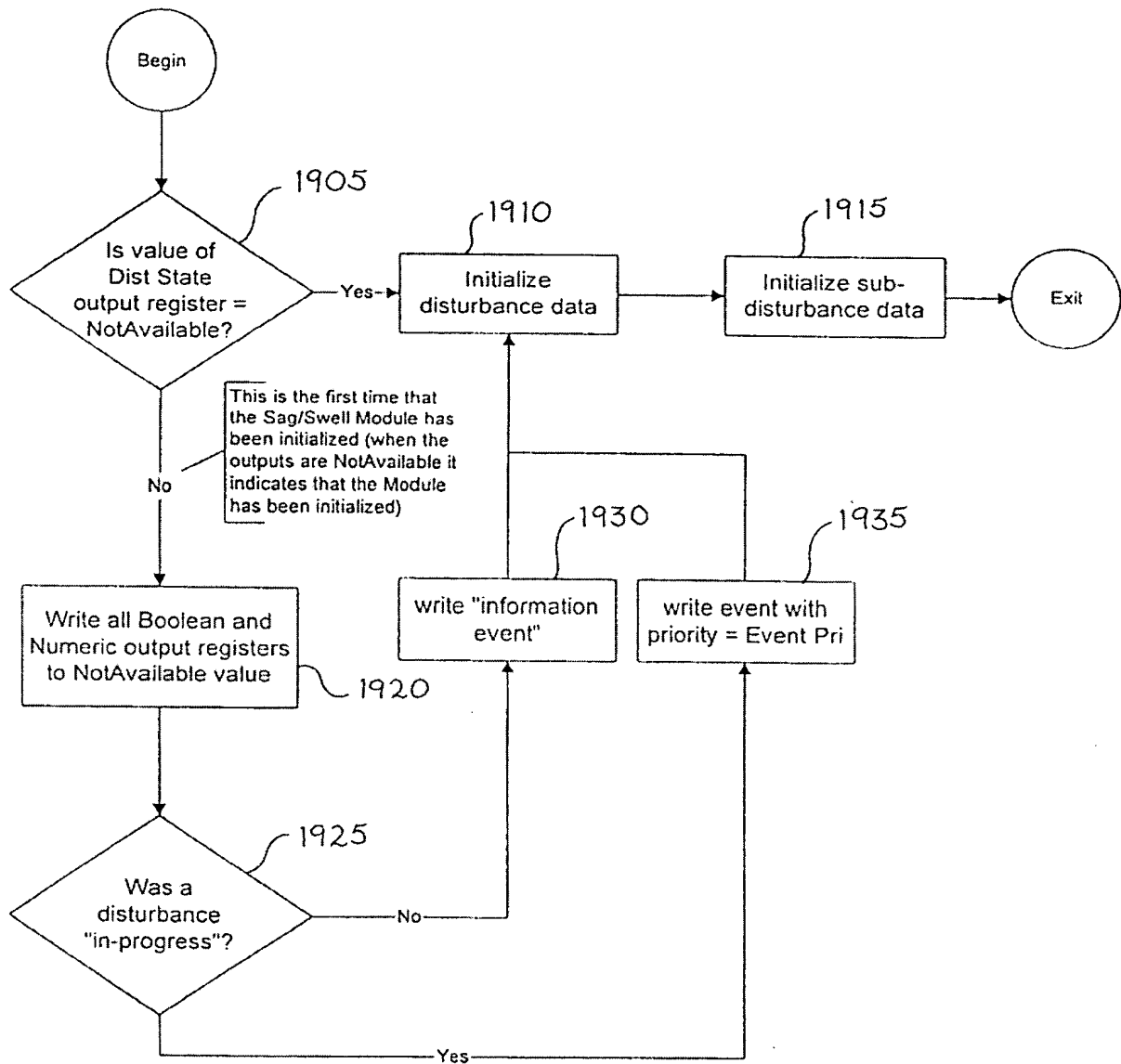


Fig. 19

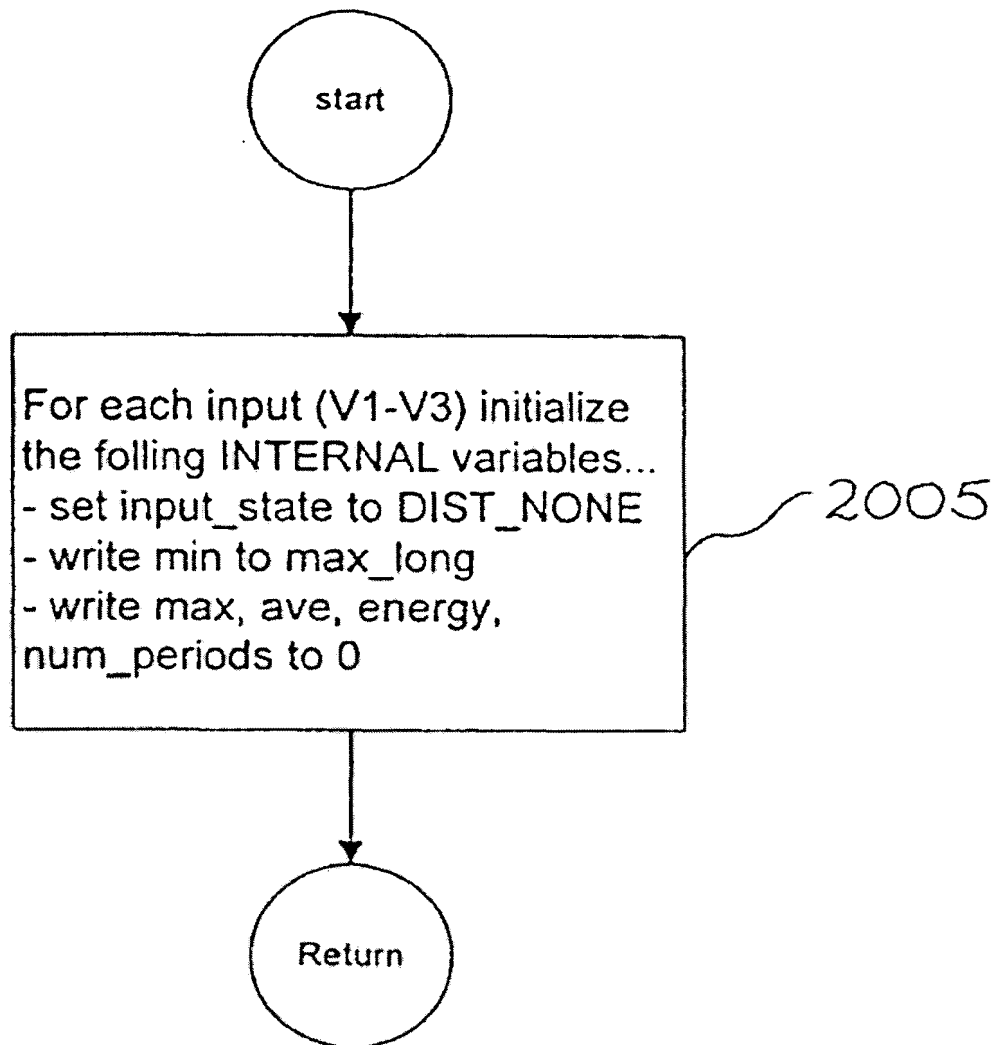


Fig. 20

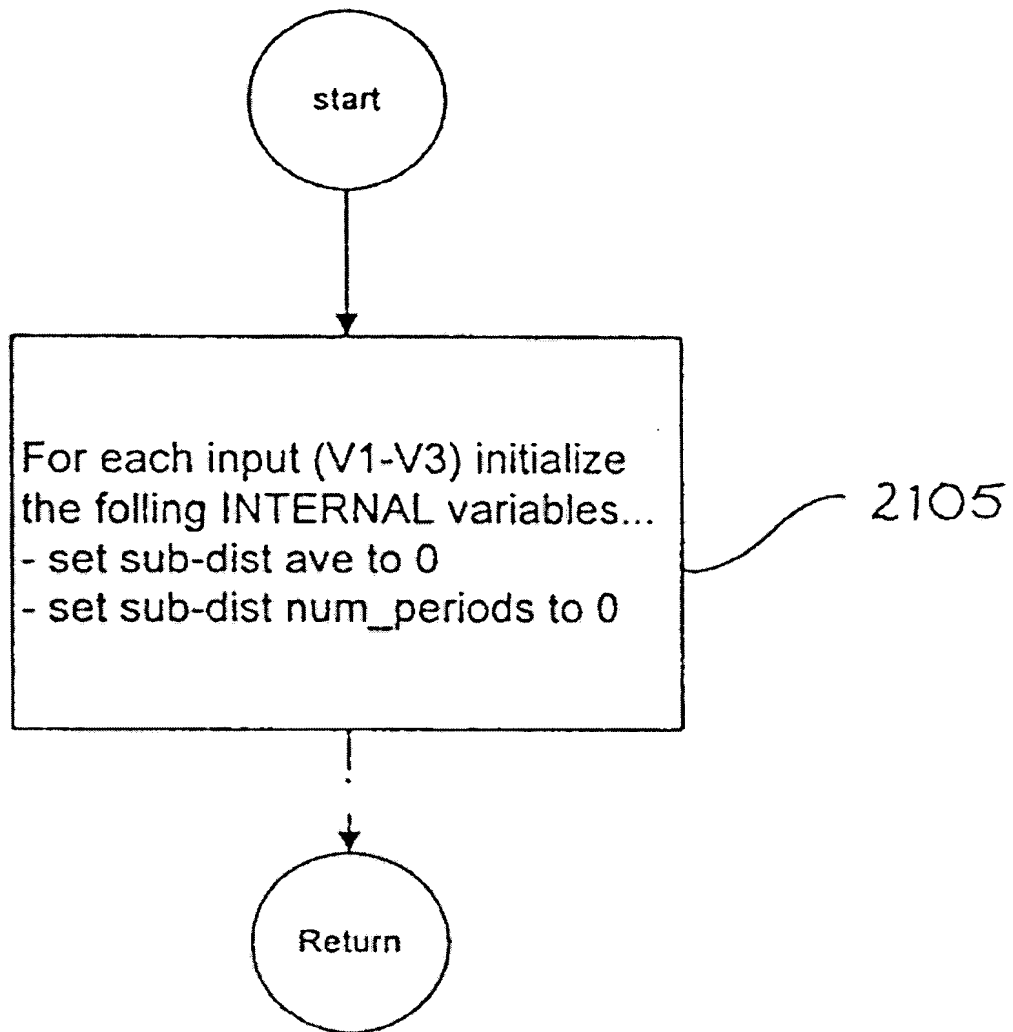
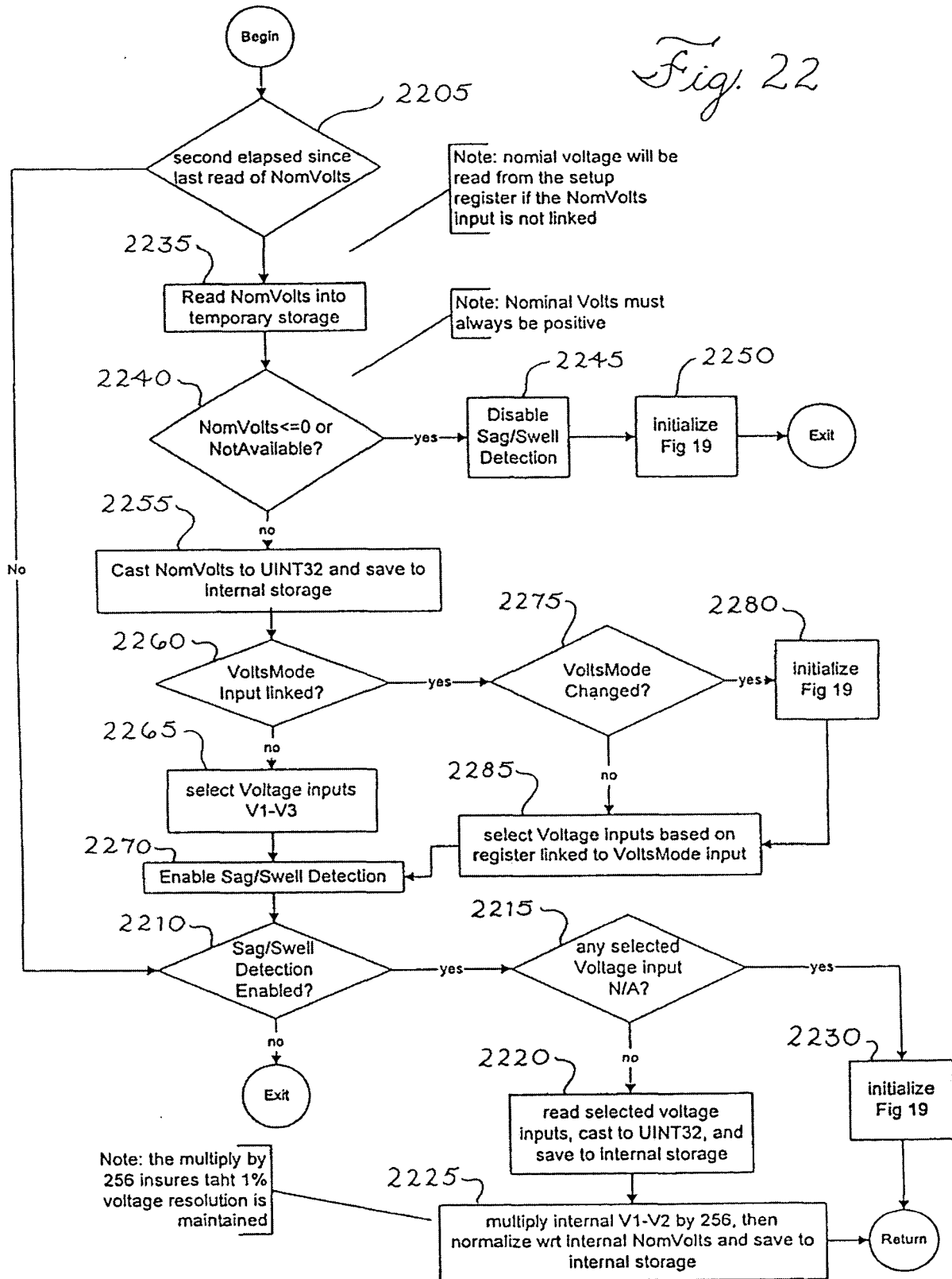
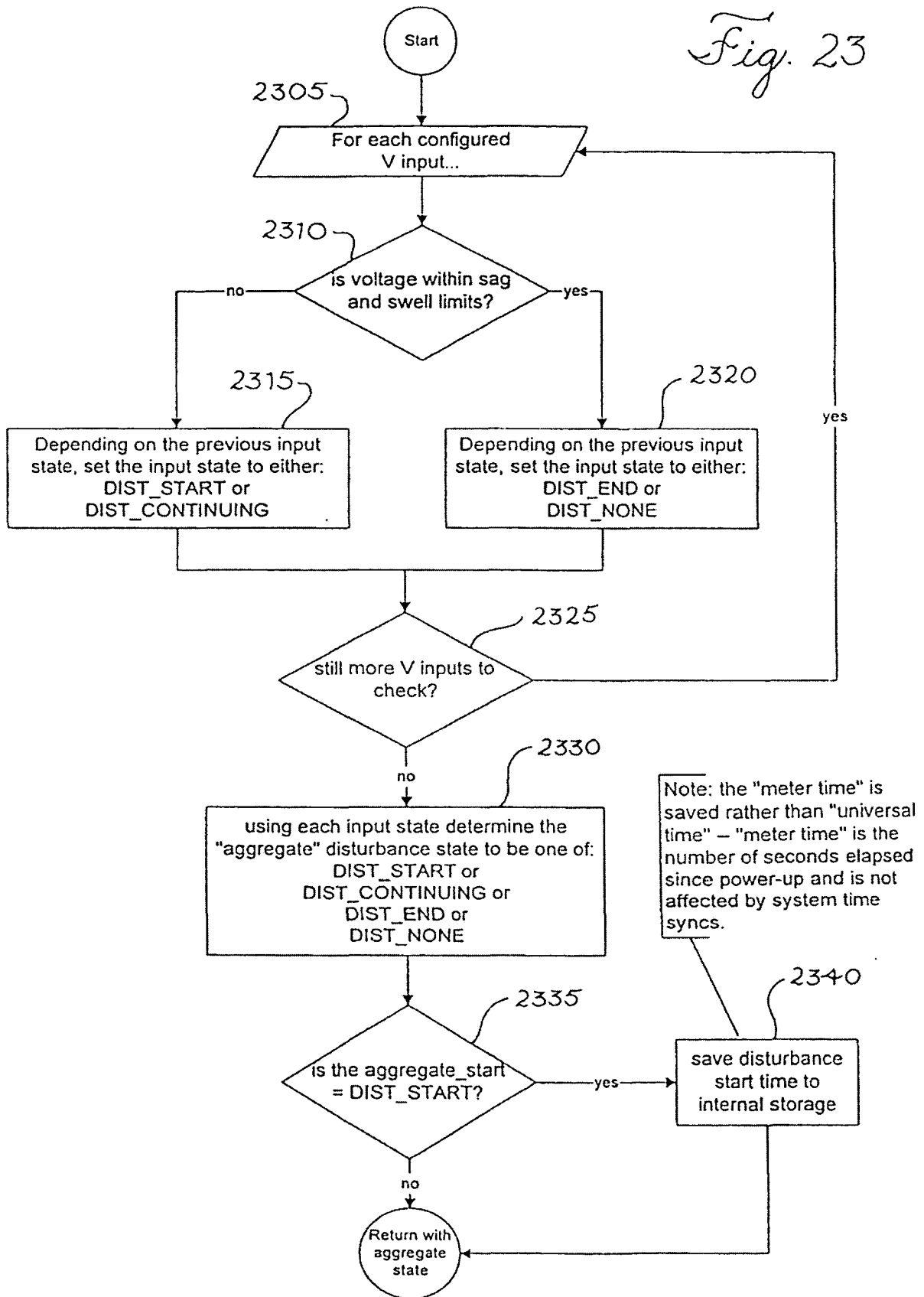


Fig. 21

Fig. 22





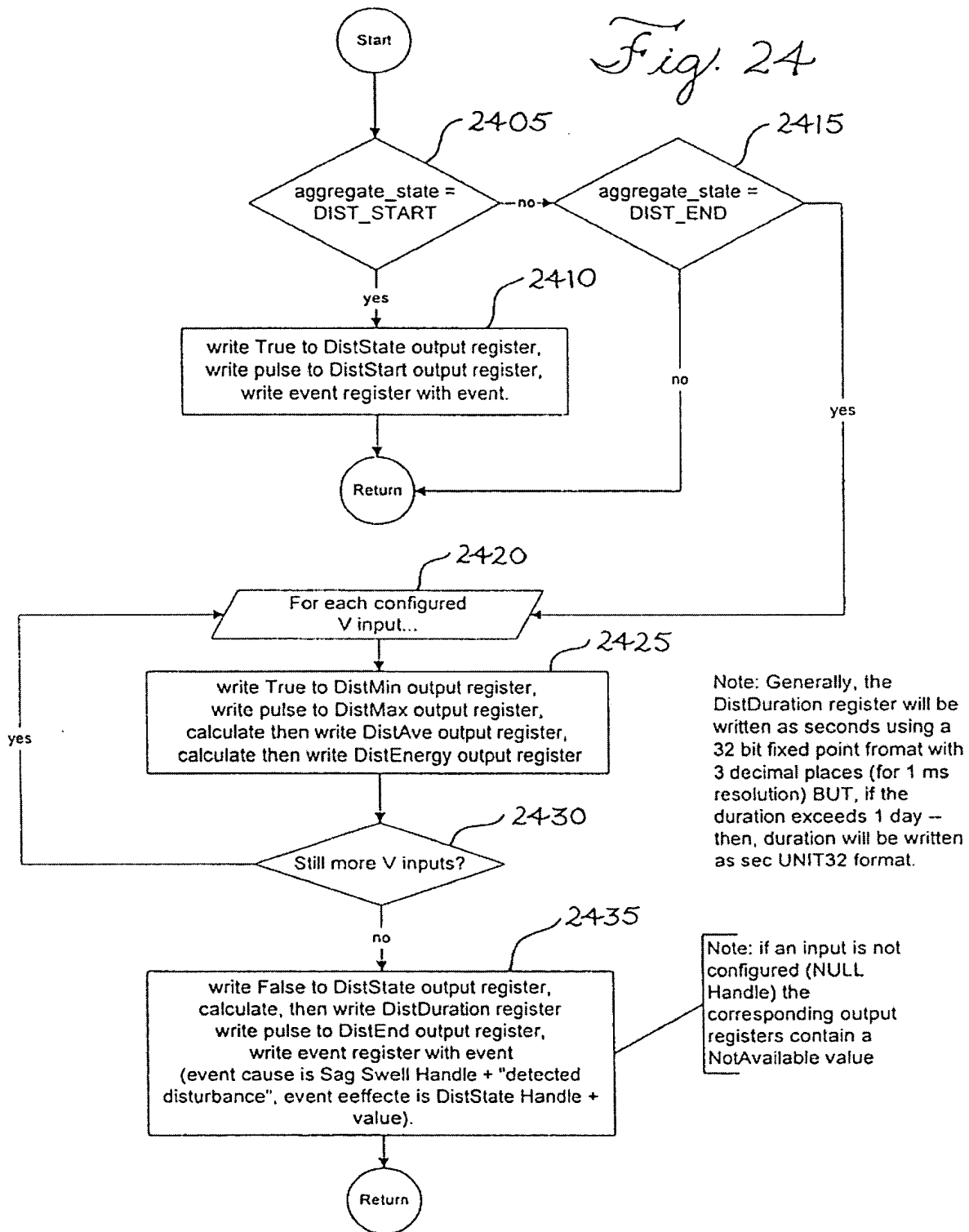
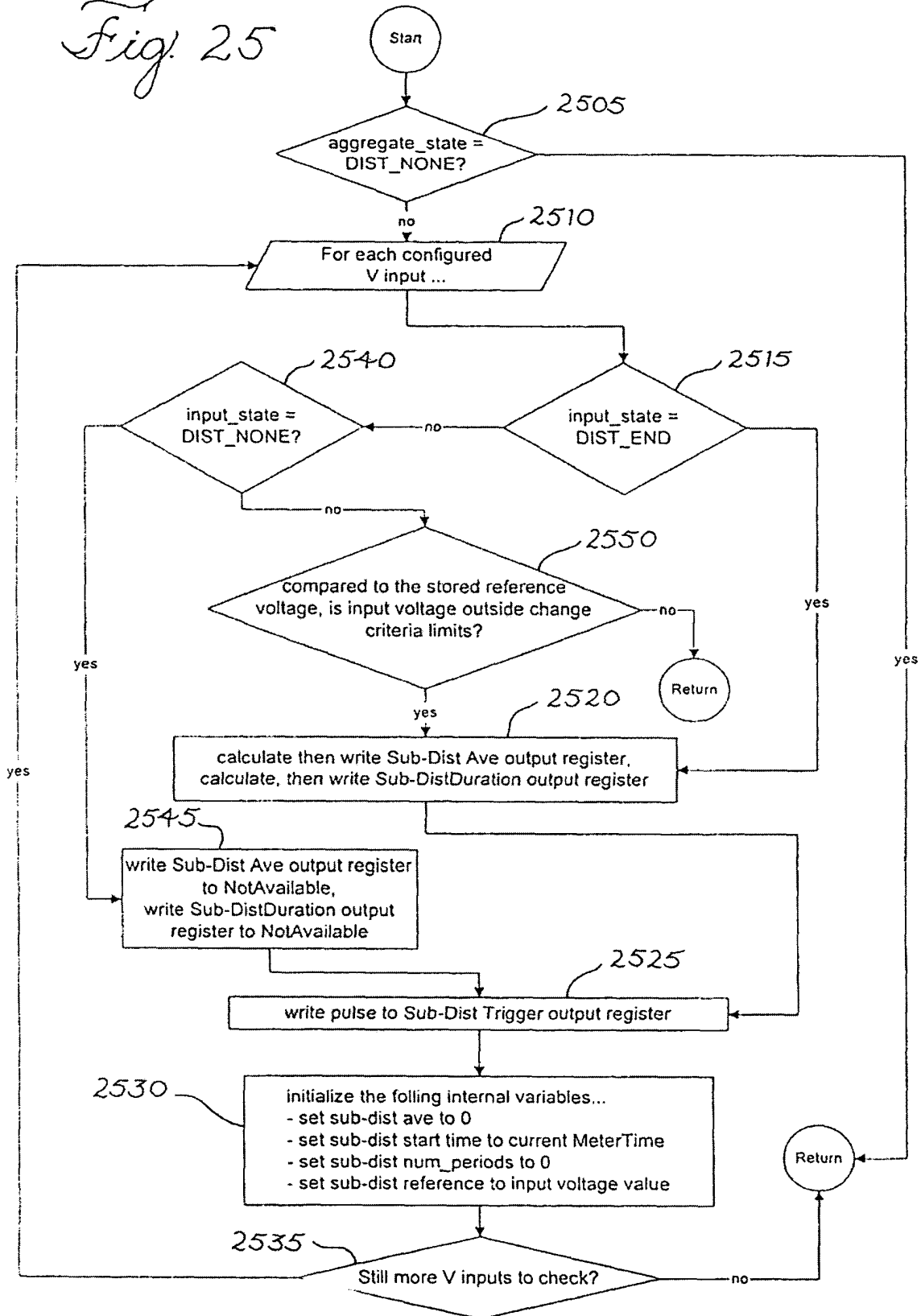


Fig. 25



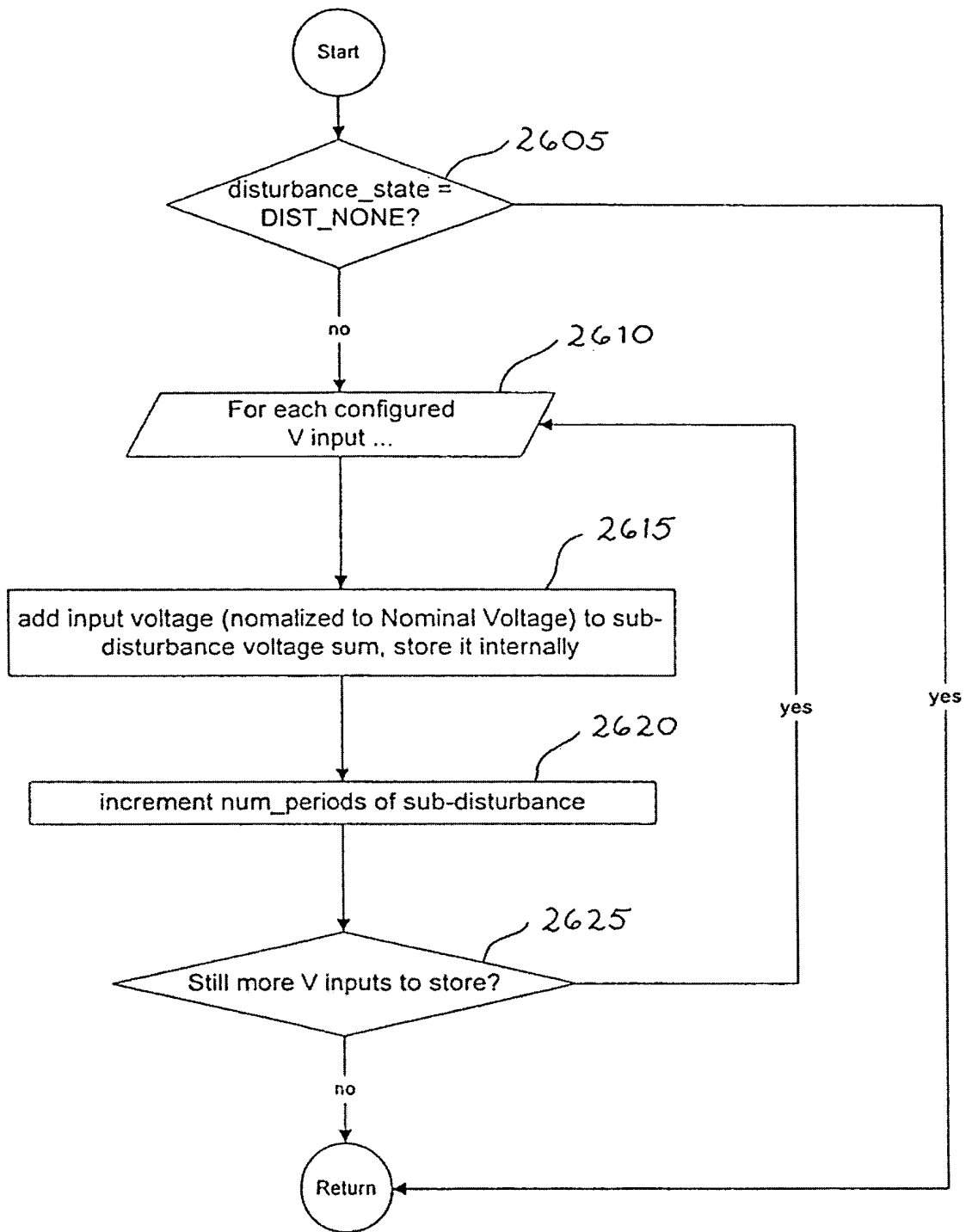
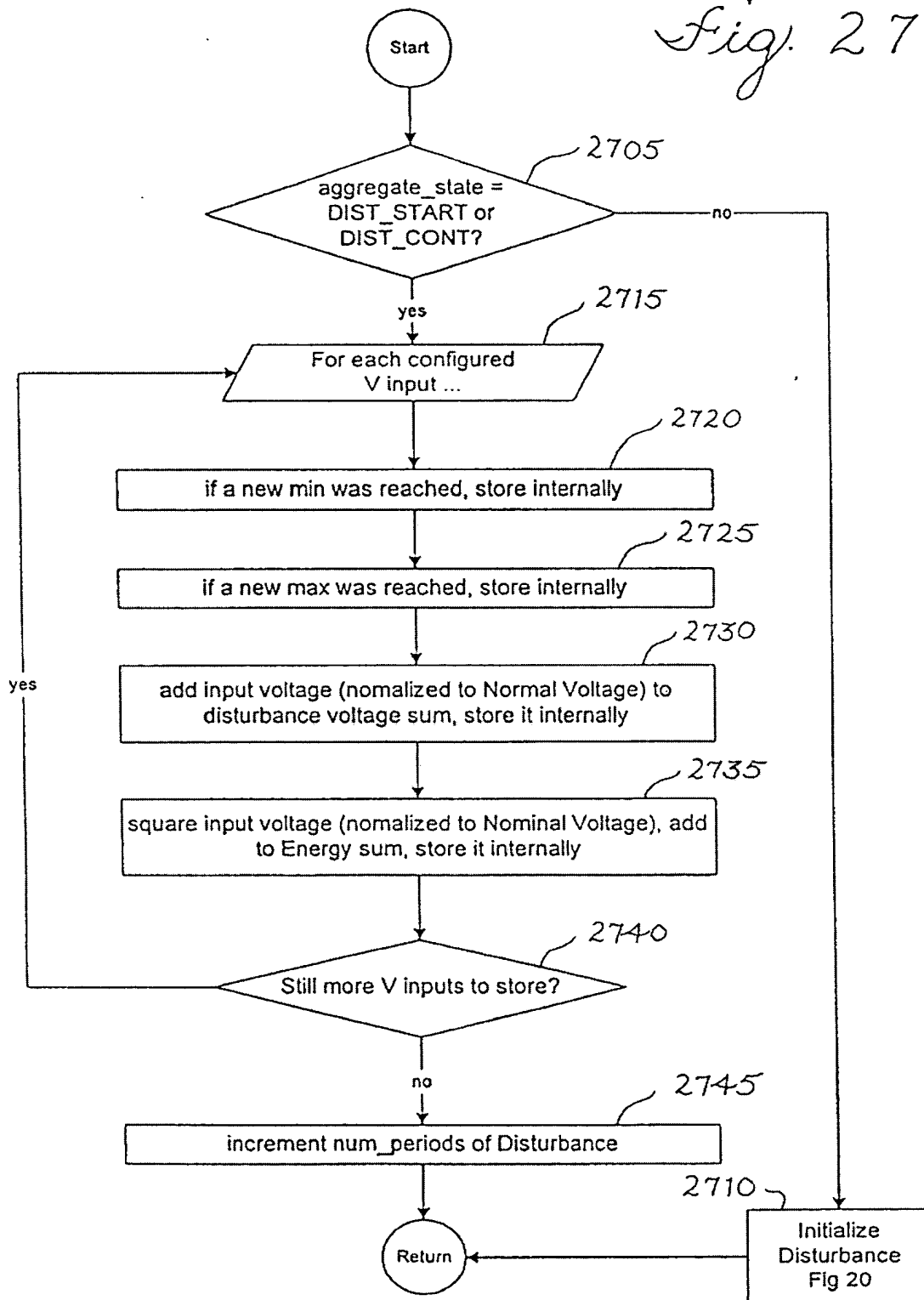


Fig. 26

Fig. 27



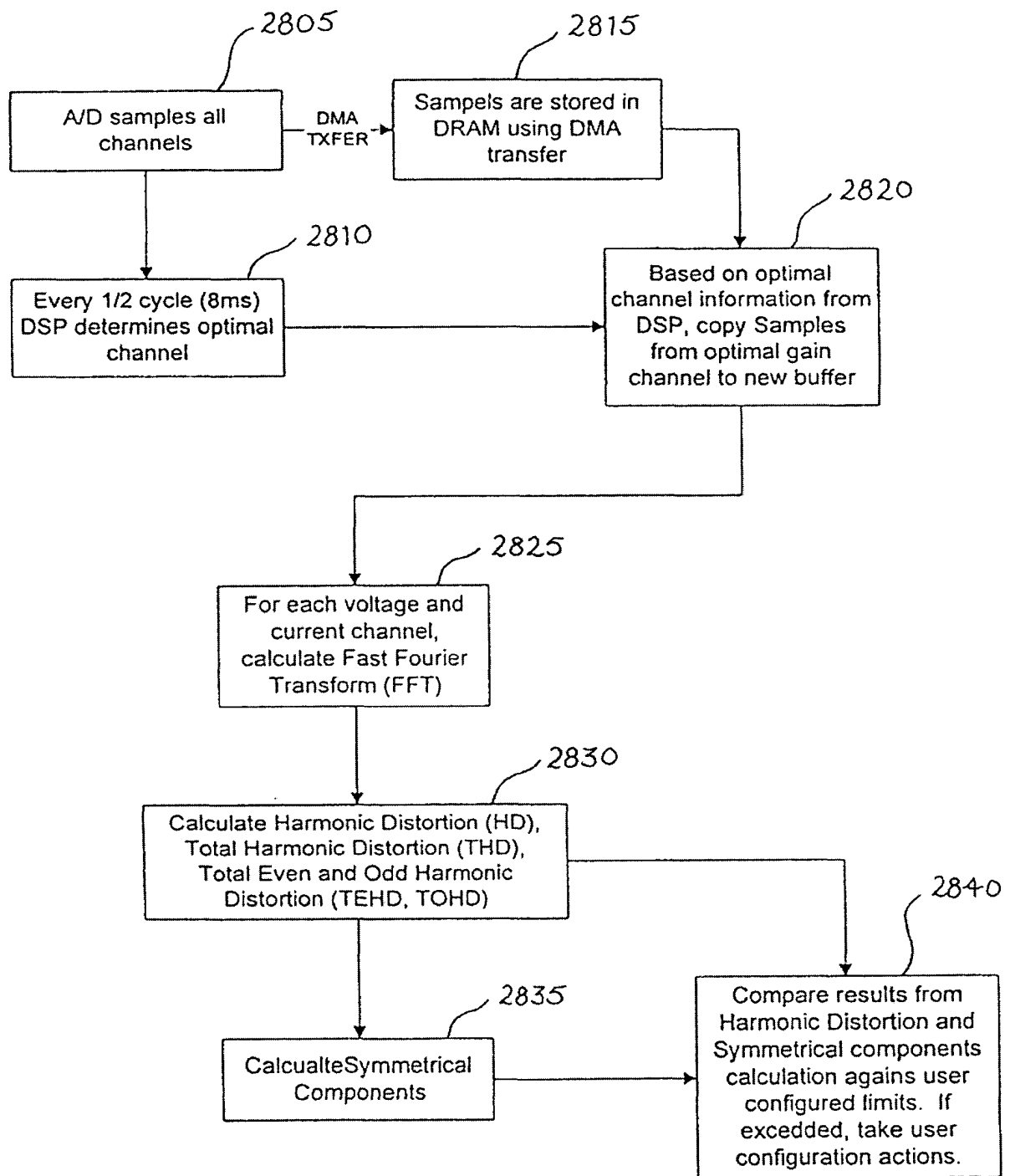


Fig. 28

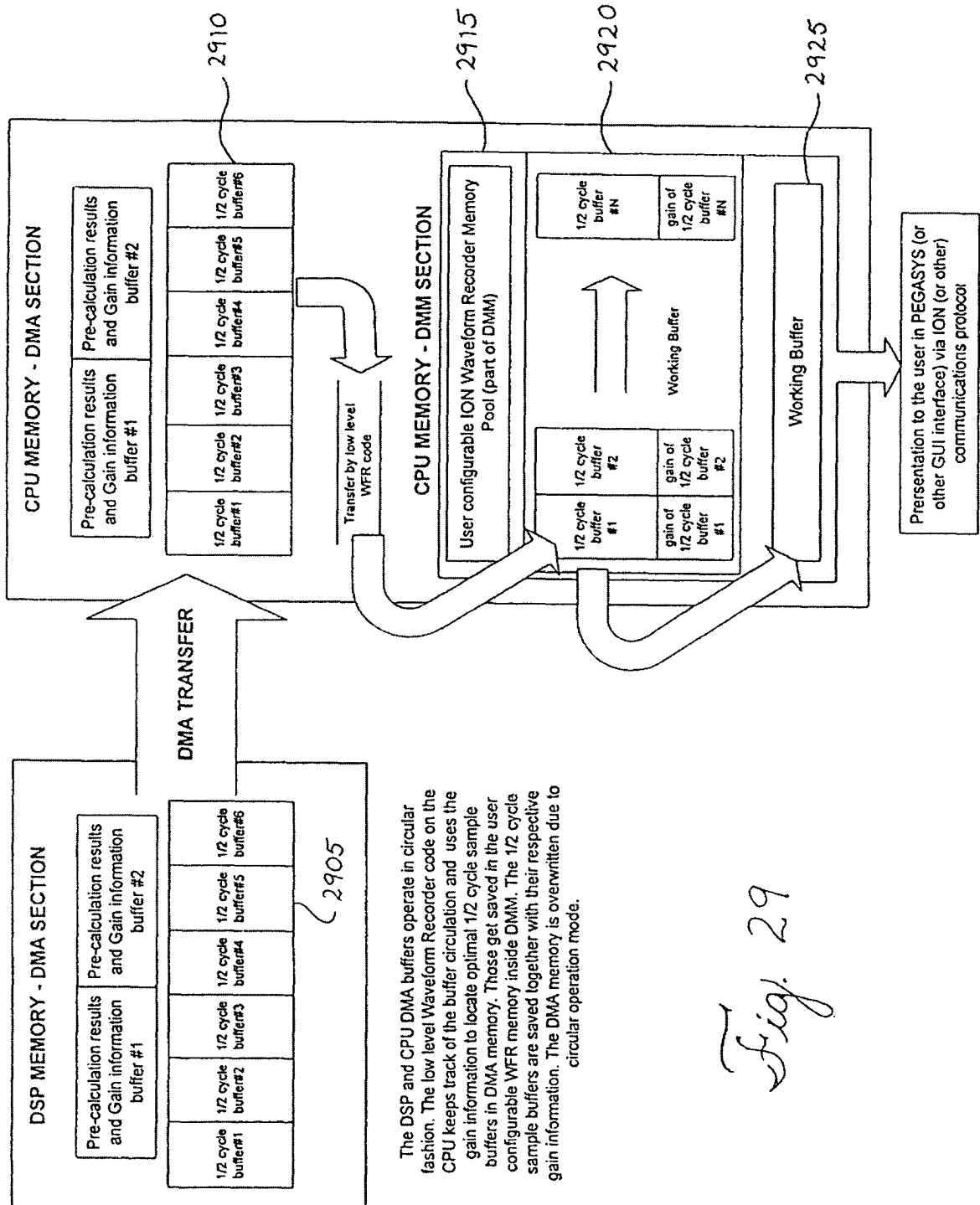


Fig. 29

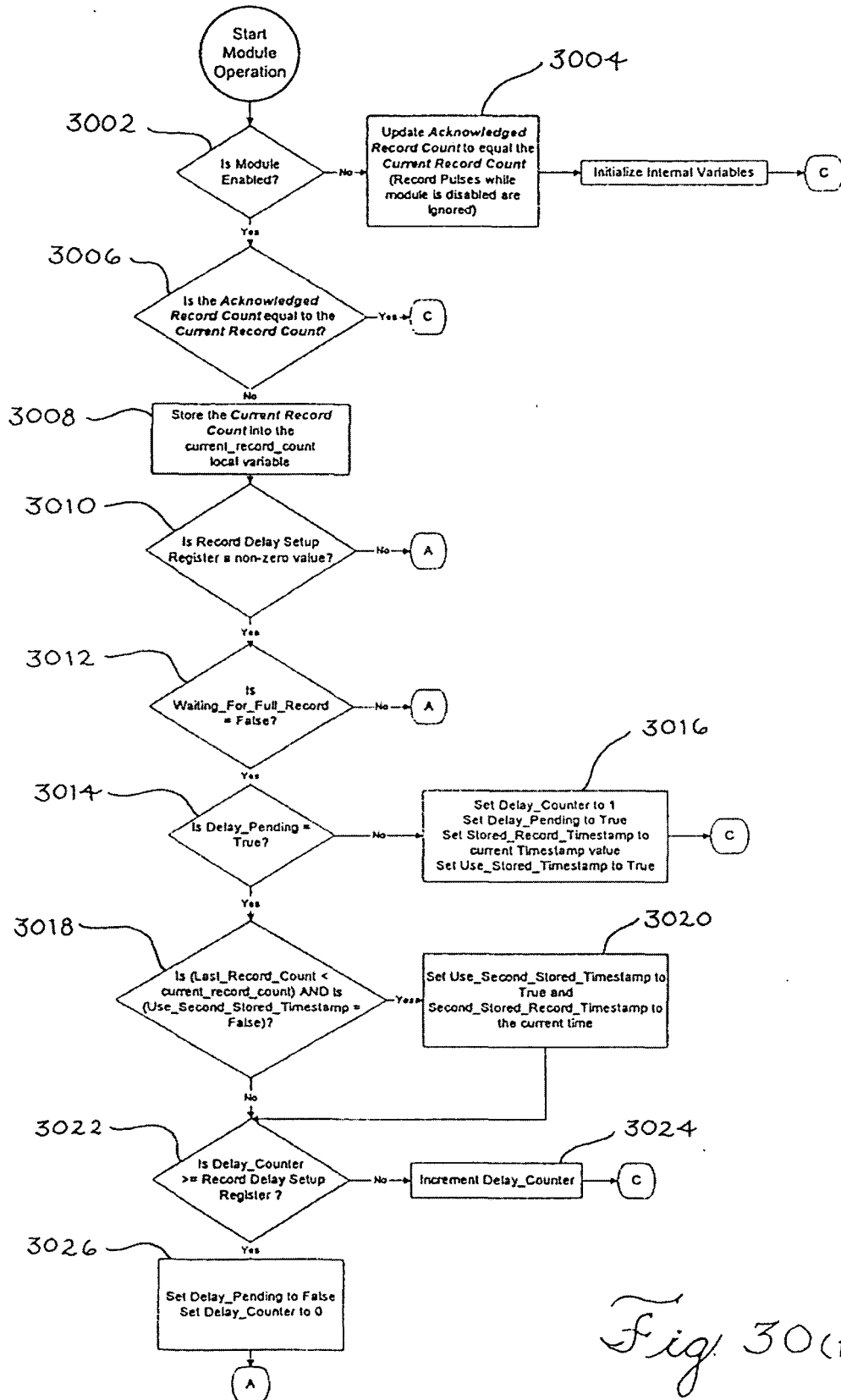


Fig. 30(1)

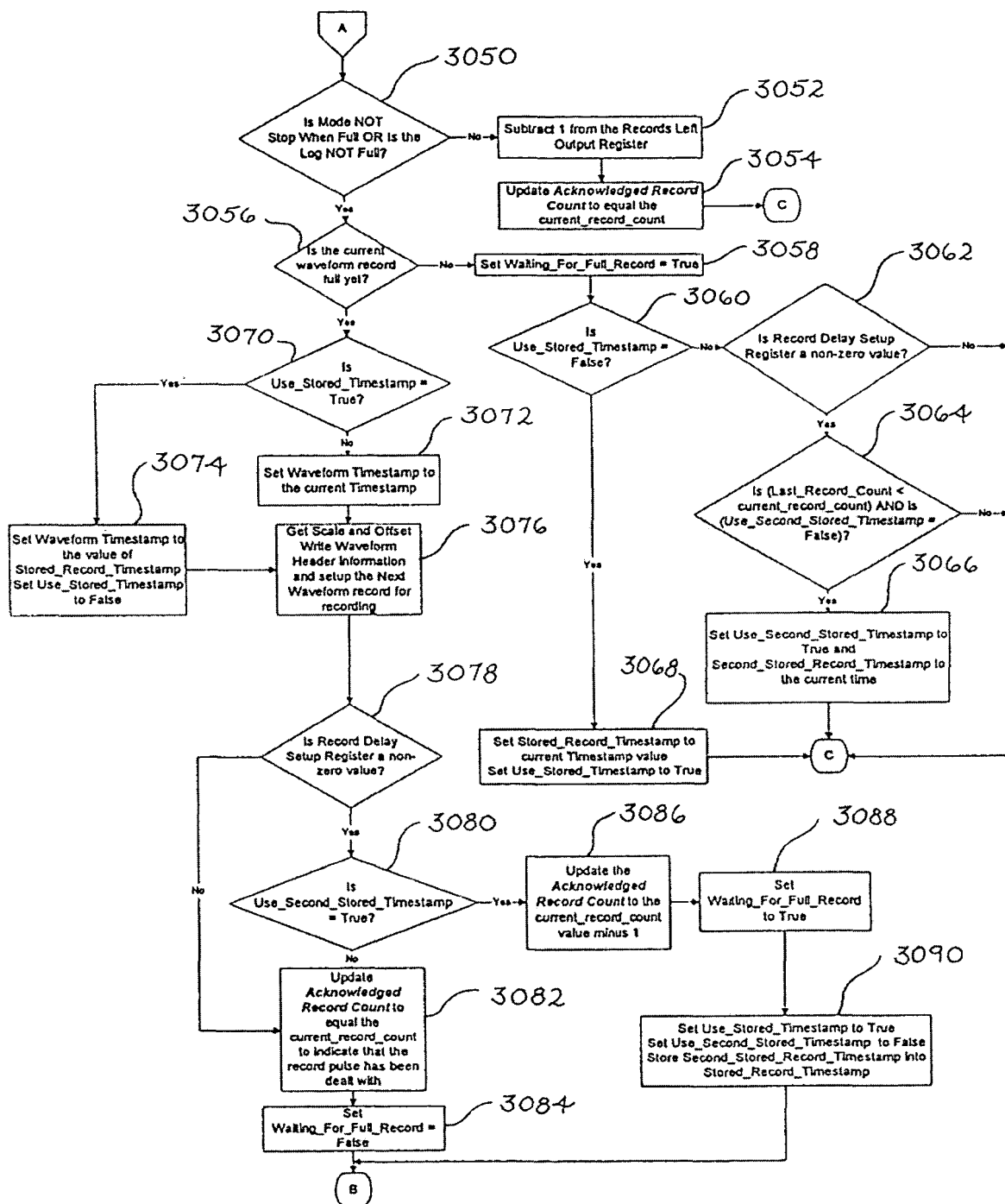


Fig. 30(2)

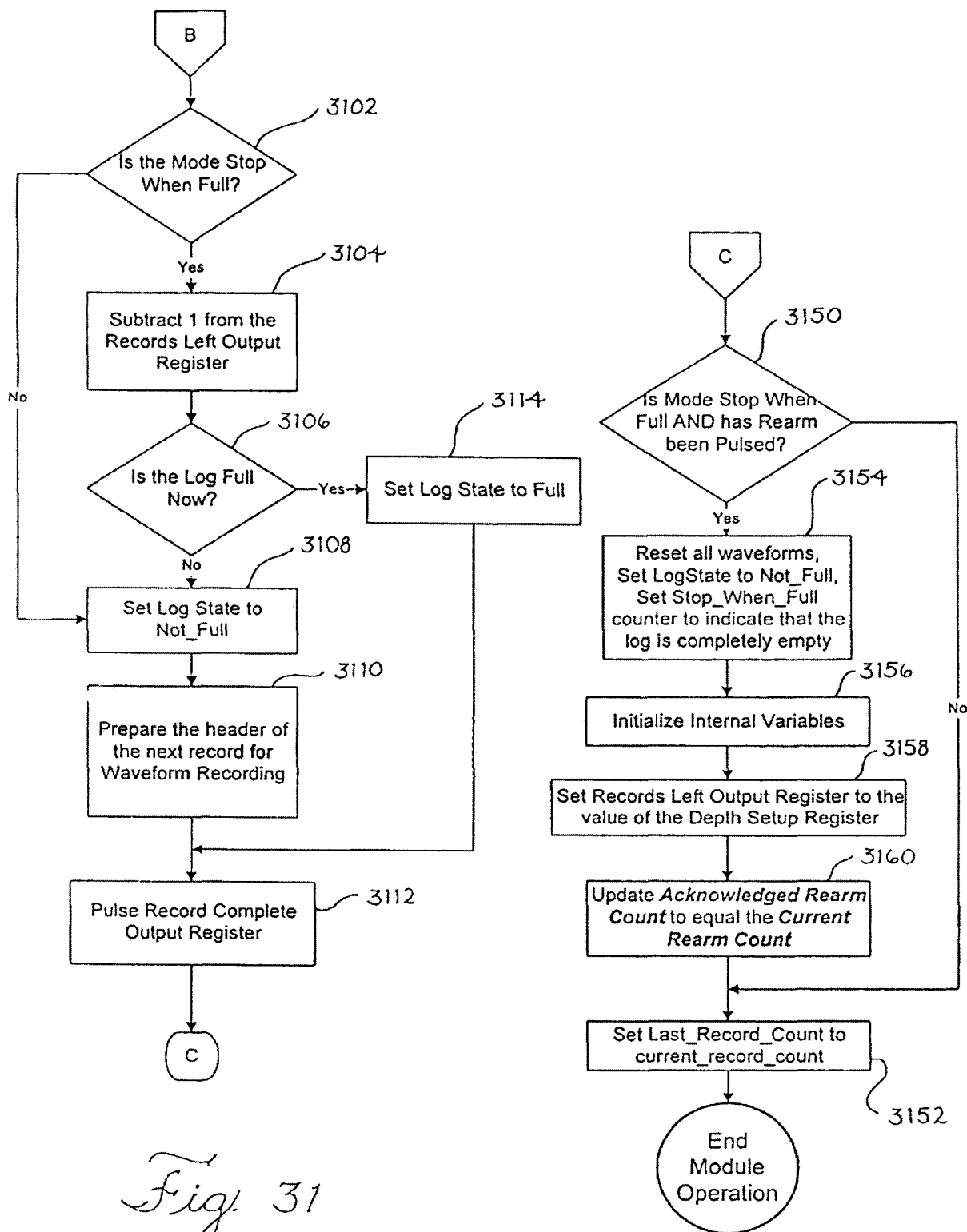


Fig. 31

Fig. 32 (1)

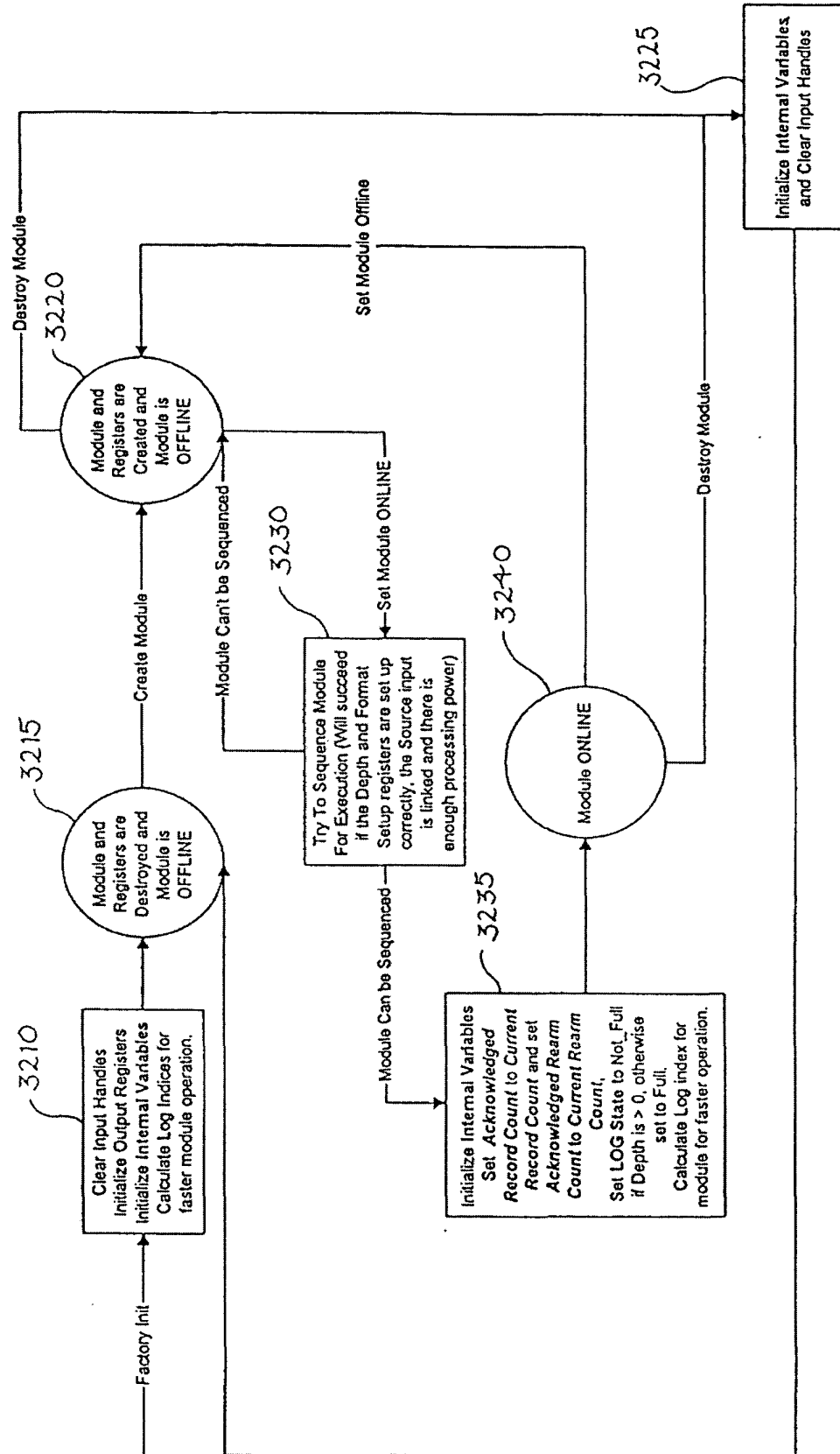


Fig. 32(2) 49/58

Internal Variables

Delay_Pending indicates whether a waveform Record Delay is currently active. Set to False on initialization of internal variables.

Delay_Counter indicates how many cycles the delay has been pending for. Set to 0 on initialization of internal variables.

Waiting_For_Full_Record Indicates a record pulse has been detected, but the current waveform record is not full yet. Set to False on initialization of internal variables.

Use_Stored_Timestamp indicates that the next waveform to be stored should use Stored_Record_Timestamp instead of the current cycle timestamp. Set to False on initialization of internal variables.

Stored_Record_Timestamp indicates the timestamp to use for the next waveform, if Used_Stored_Timestamp is True. Never initialized since it will only be used when Use_Stored_Timestamp is True, which indicates that Stored_Record_Timestamp has been set.

Use_Second_Stored_Timestamp indicates that the next waveform to be stored should use Stored_Record_Timestamp and that the waveform following should use Second_Stored_Record_Timestamp instead of the current cycle timestamp. If it is True, then Use_Stored_Timestamp is also True. Set to False on initialization of internal variables.

Second_Stored_Record_Timestamp indicates the timestamp to use for the waveform following the next waveform, if Used_Second_Stored_Timestamp is True. It will only be set if Stored_Record_Timestamp has also been set. Never initialized since it will only be used when Use_Second_Stored_Timestamp is True, which indicates that Second_Stored_Record_Timestamp has been set.

Last_Record_Count indicates the Record count on last module execution. It is set to the current Record input count on initialization of internal variables. **Acknowledged Record Count** indicates the Record pulse count that has been acknowledged already. If this value is equal to the number of pulses on the Record input, then the module does not need to store any new waveforms. This value is actually stored in the Input Handle structure for the Record input handle.

Acknowledged Rearm Count indicates the Rearm pulse count that has been acknowledged already. If this value is equal to the number of pulses on the Rearm input, then the Rearm input has not been pulsed. This value is actually stored in the Input Handle structure for the Rearm input handle.

Local Variables

Current Record Count indicates the pulse count in the register connected to the Record input link. If this value is greater than the Acknowledged Record Count then the module must store a new waveform. This value is copied into the current_record_count local variable at the start of the operate function.

Current Rearm Count indicates the pulse count in the register connected to the Rearm input link. If this value is greater than the Acknowledged Rearm Count then the module must rearm itself.

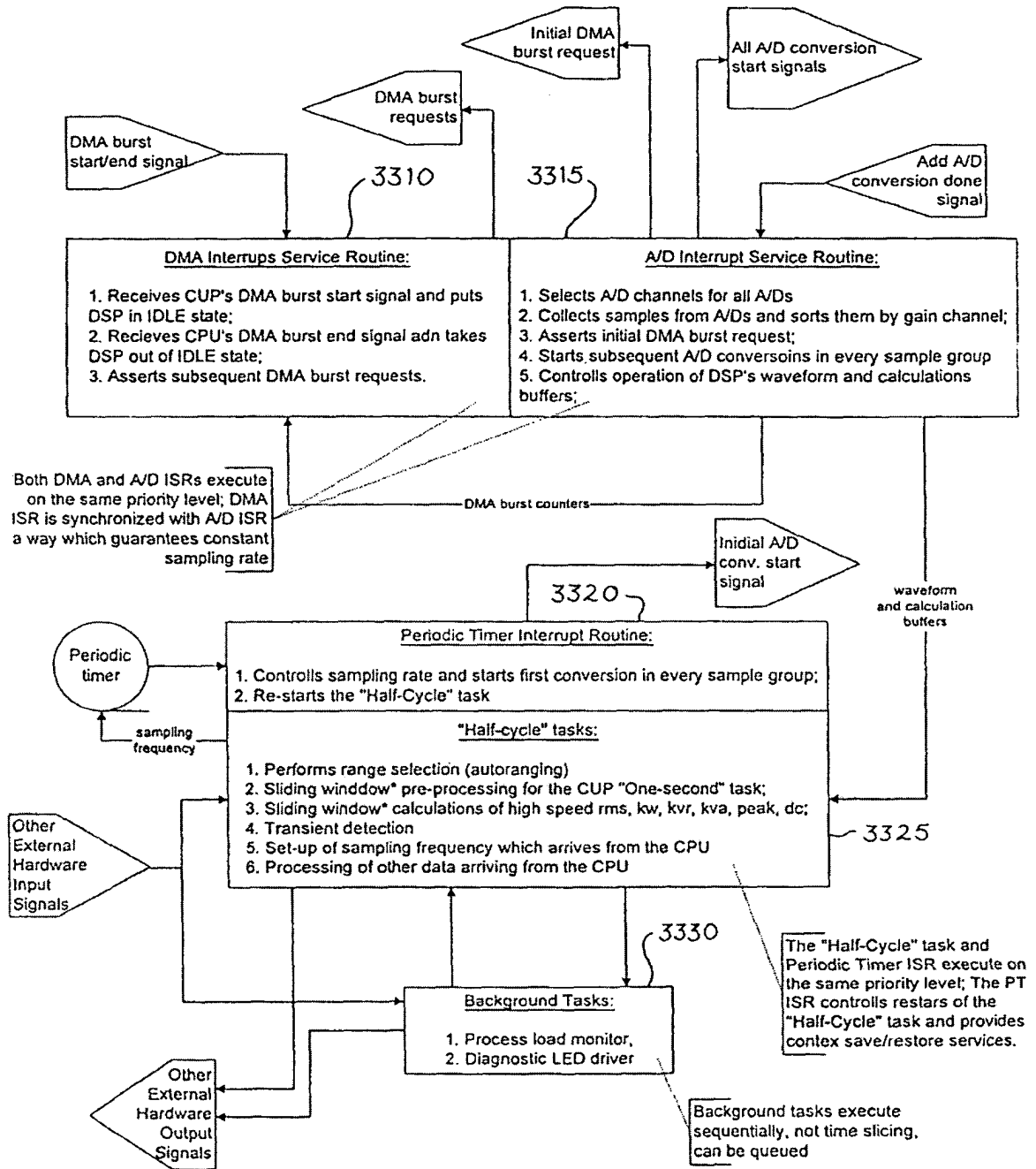




Fig. 33

Fig. 34

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DMA Half-Cycle Activity Timeline

line half cycles	n-1	n	n+1	n+2	n+3	n+4	n+5
DSP ACTIVITY	AD sample(n-1) & pre-process(n-3)(n-2)	AD sample(n) & pre-process(n-2)(n-1)	AD sample(n+1) & pre-process(n-1)(n)	AD sample(n+2) & pre-process(n)(n+1)	AD sample(n+3) & pre-process(n+1)(n+2)	AD sample(n+4) & pre-process(n+2)(n+3)	AD sample(n+5) & pre-process(n+3)(n+4)
DMA ACTIVITY	DMA transfer. samples(n-2) & pre-results(n-4)(n-3)	DMA transfer. samples(n-1) & pre-results(n-3)(n-2)	DMA transfer. samples(n) & pre-results(n-2)(n-1)	DMA transfer. samples(n+1) & pre-results(n-1)(n)	DMA transfer. samples(n+2) & pre-results(n)(n+1)	DMA transfer. samples(n+3) & pre-results(n+1)(n+2)	DMA transfer. samples(n+4) & pre-results(n+2)(n+3)
CPU ACTIVITY	process pre-results(n-5)(n-4) record waveform(n-5)	process pre-results(n-4)(n-3) record waveform(n-4)	process pre-results(n-3)(n-2) record waveform(n-3)	process pre-results(n-2)(n-1) record waveform(n-2)	process pre-results(n-1)(n) record waveform(n-1)	process pre-results(n)(n+1) record waveform(n)	process pre-results(n+1)(n+2) record waveform(n+1)

 Waveform Recording is autoranged and delayed by 3 to 4 half cycles with respect to any real-time line event
 Half Cycle calculation Results are delayed by 3 half cycles with respect to any real-time line event

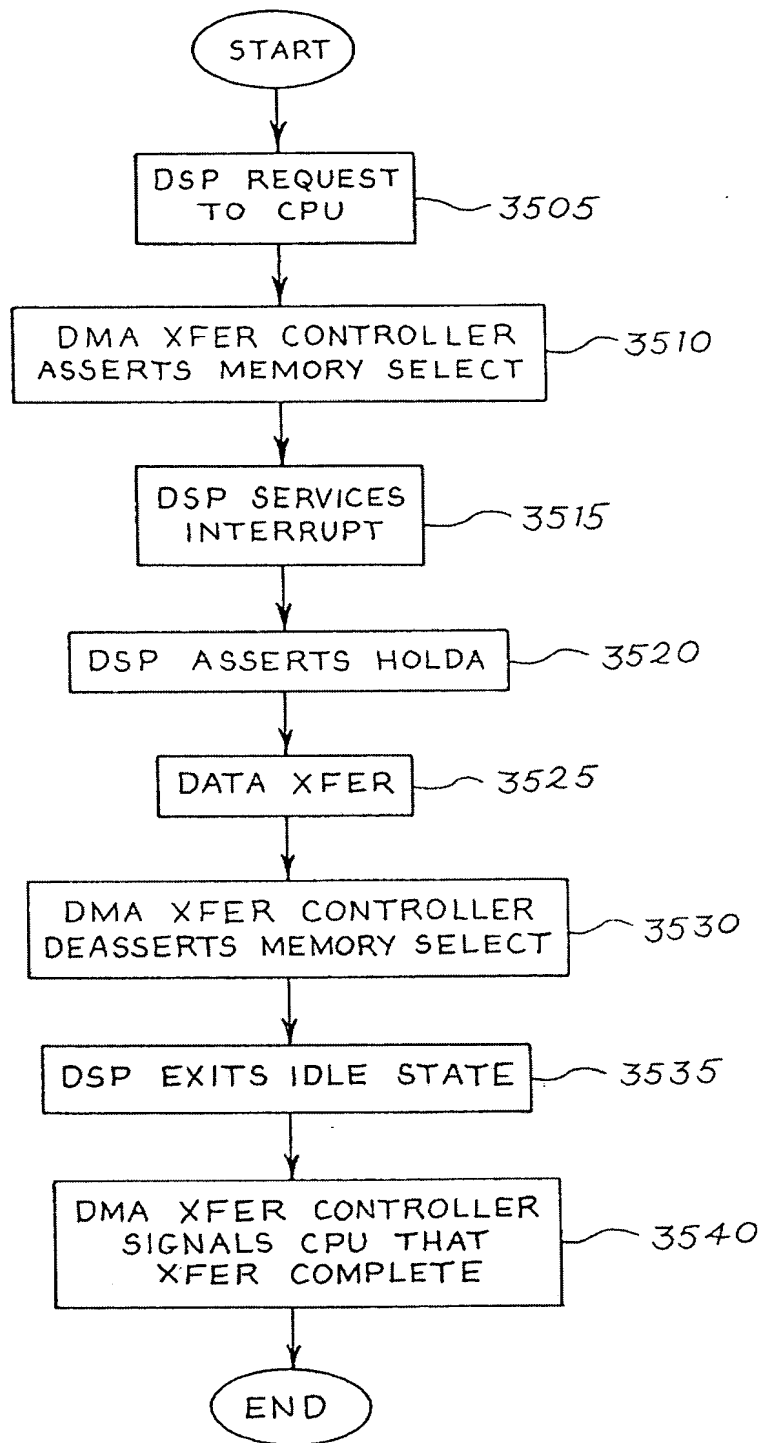
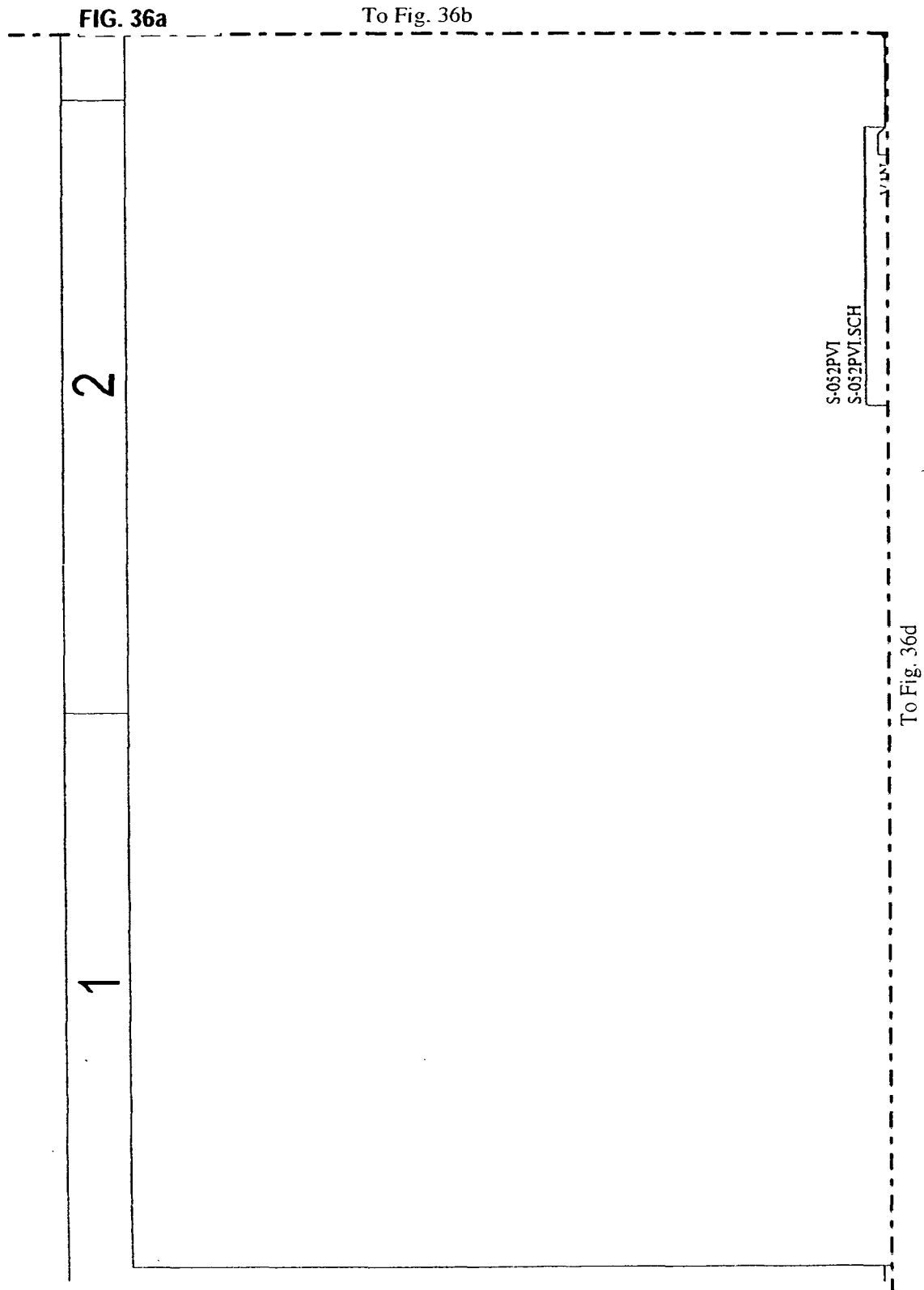


Fig. 35



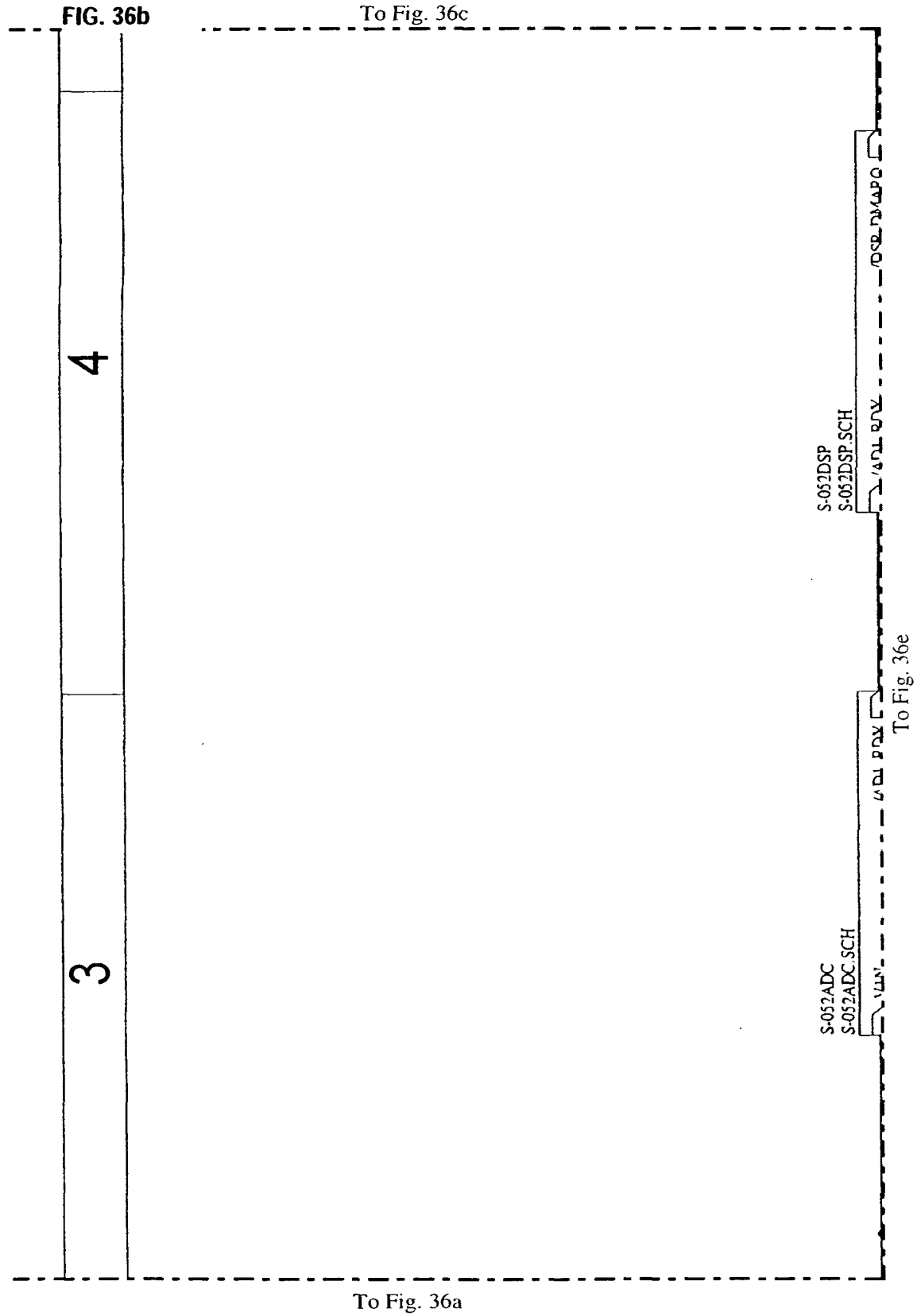
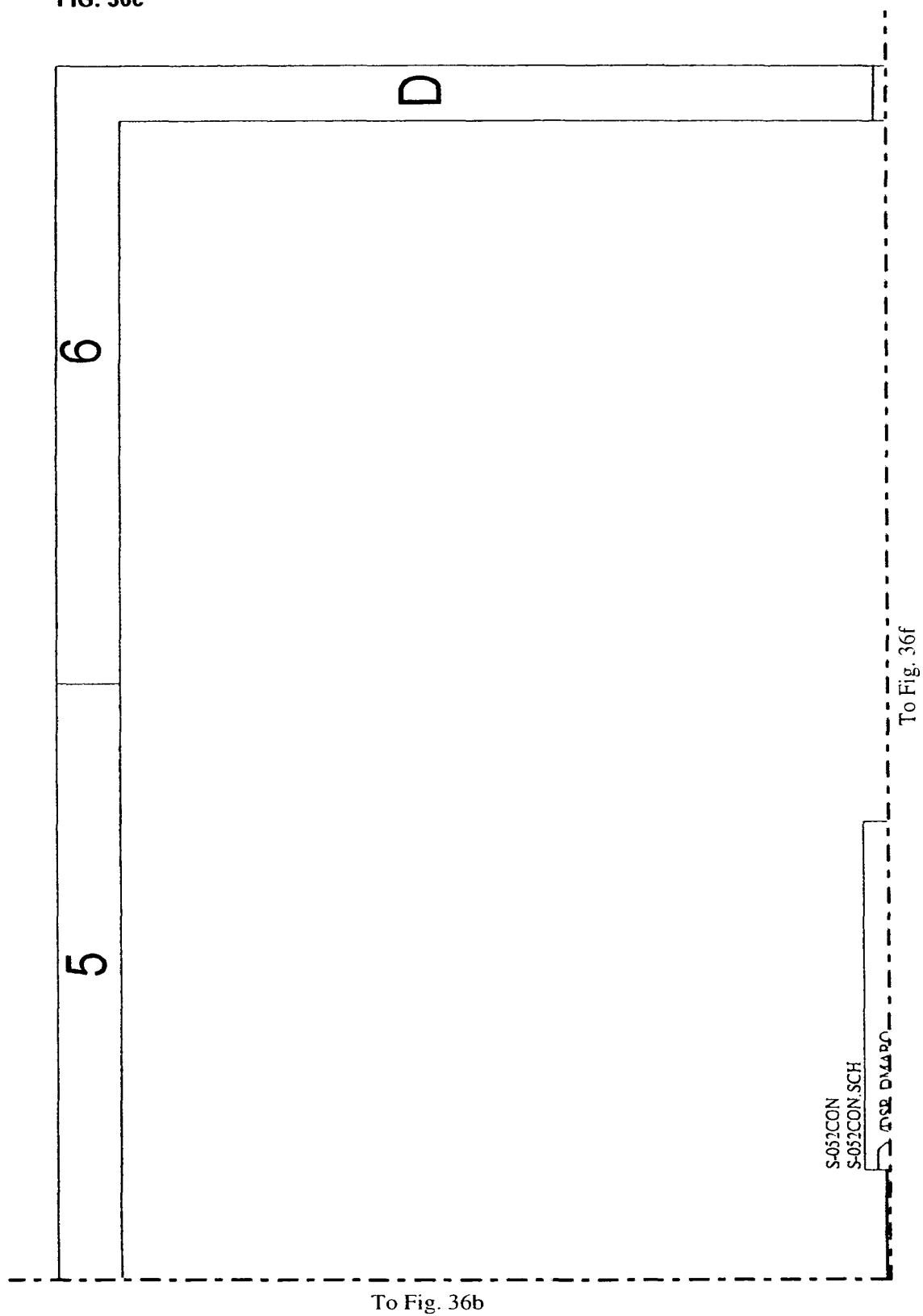
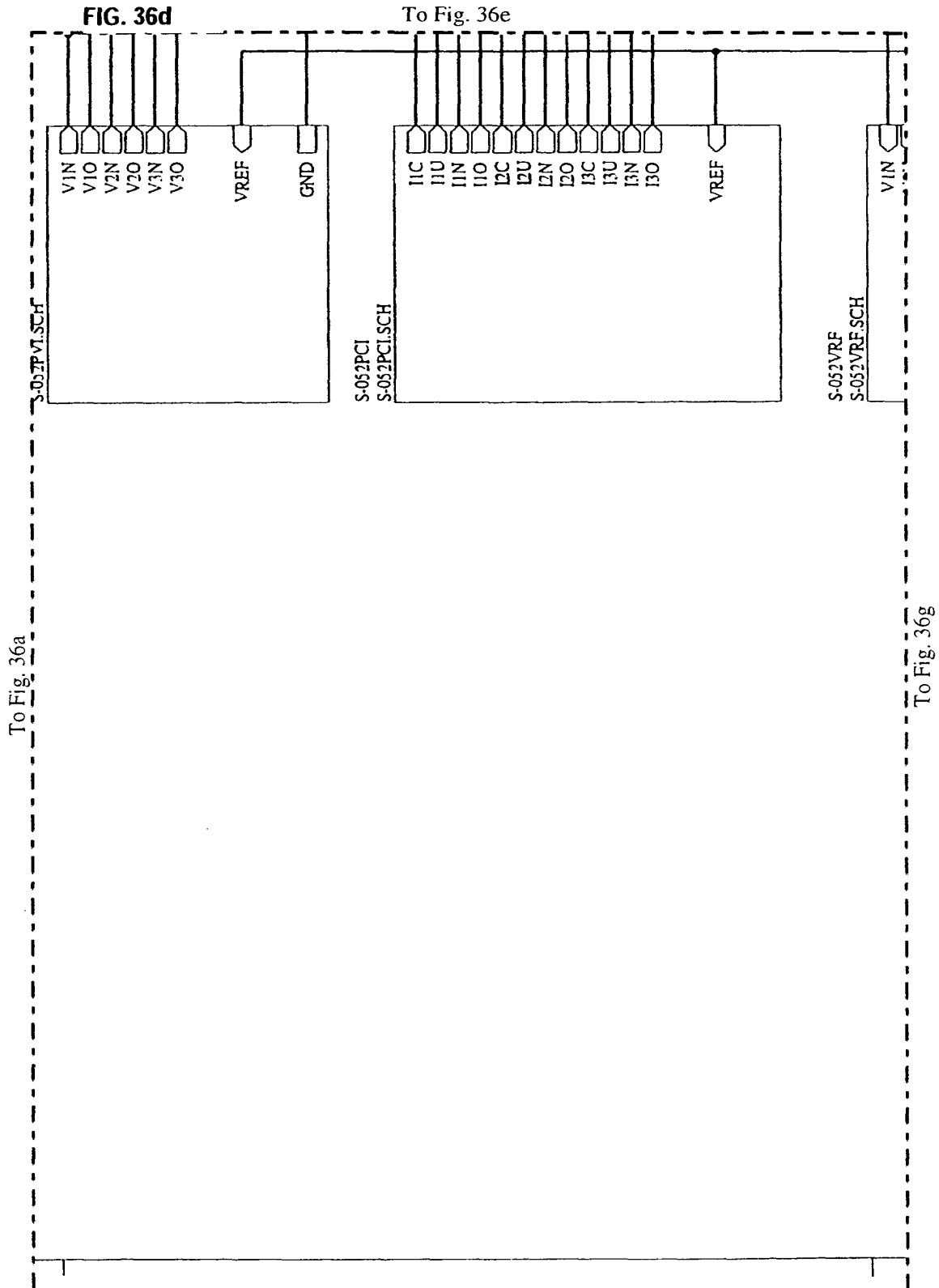


FIG. 36c





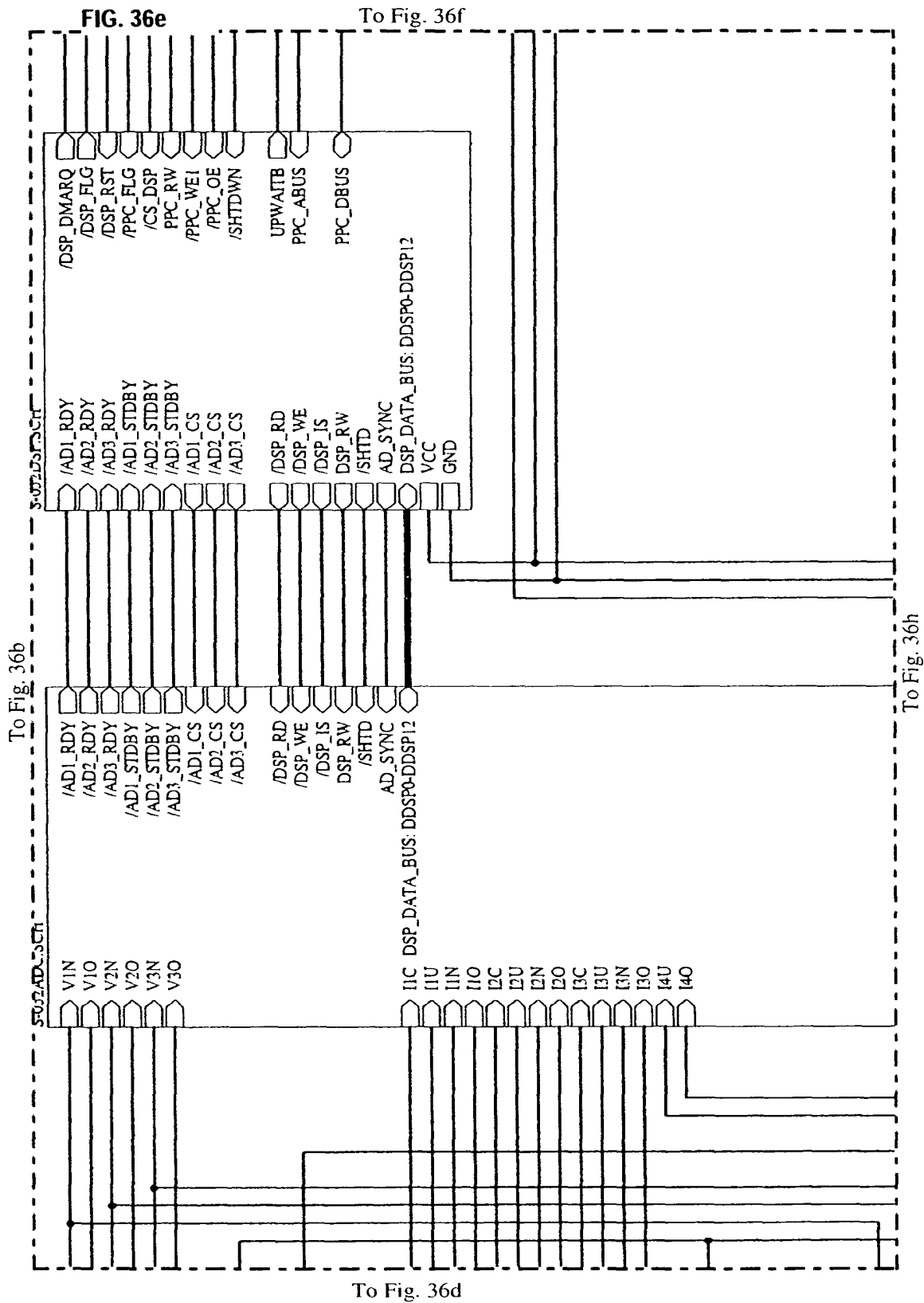
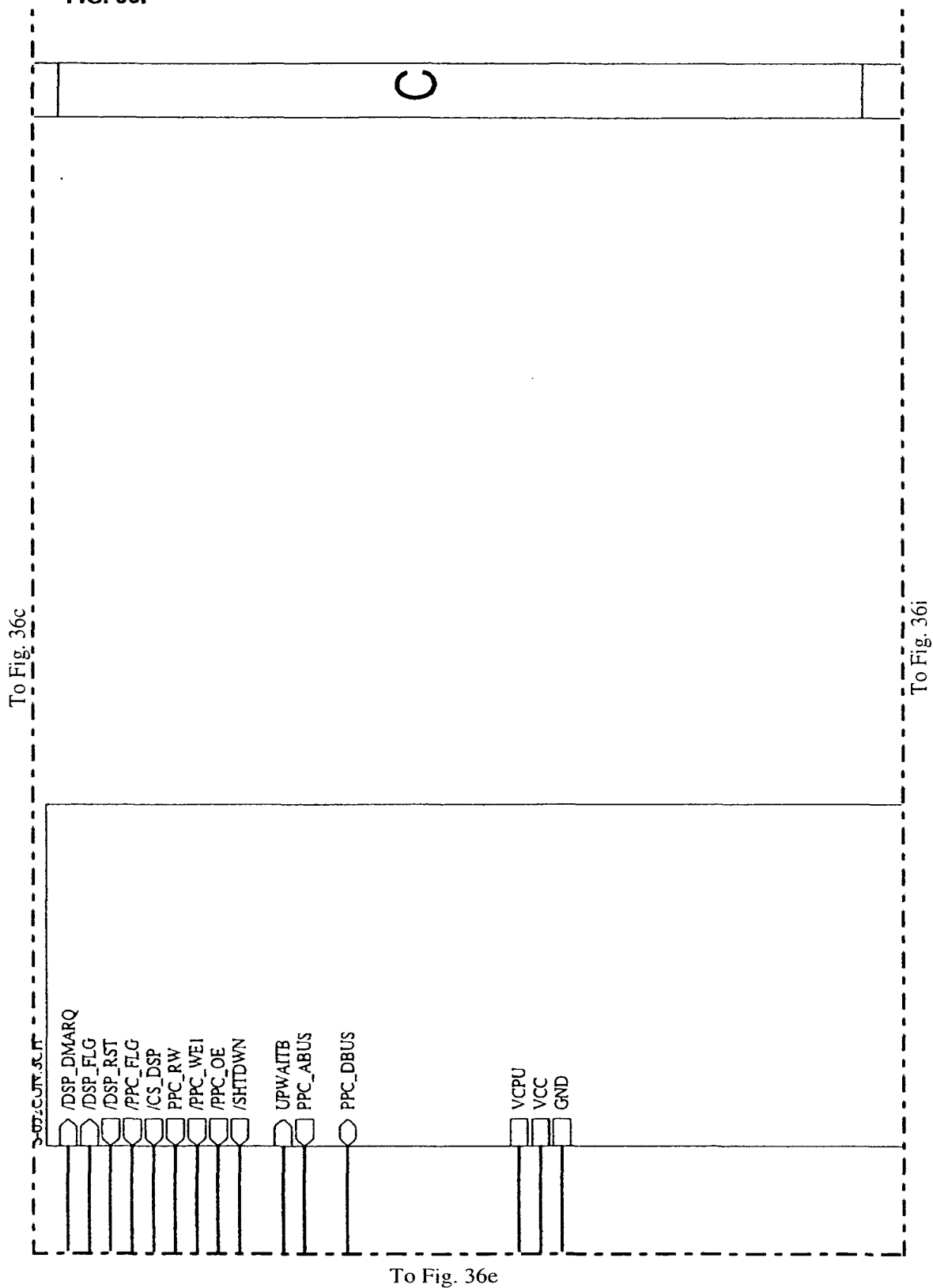
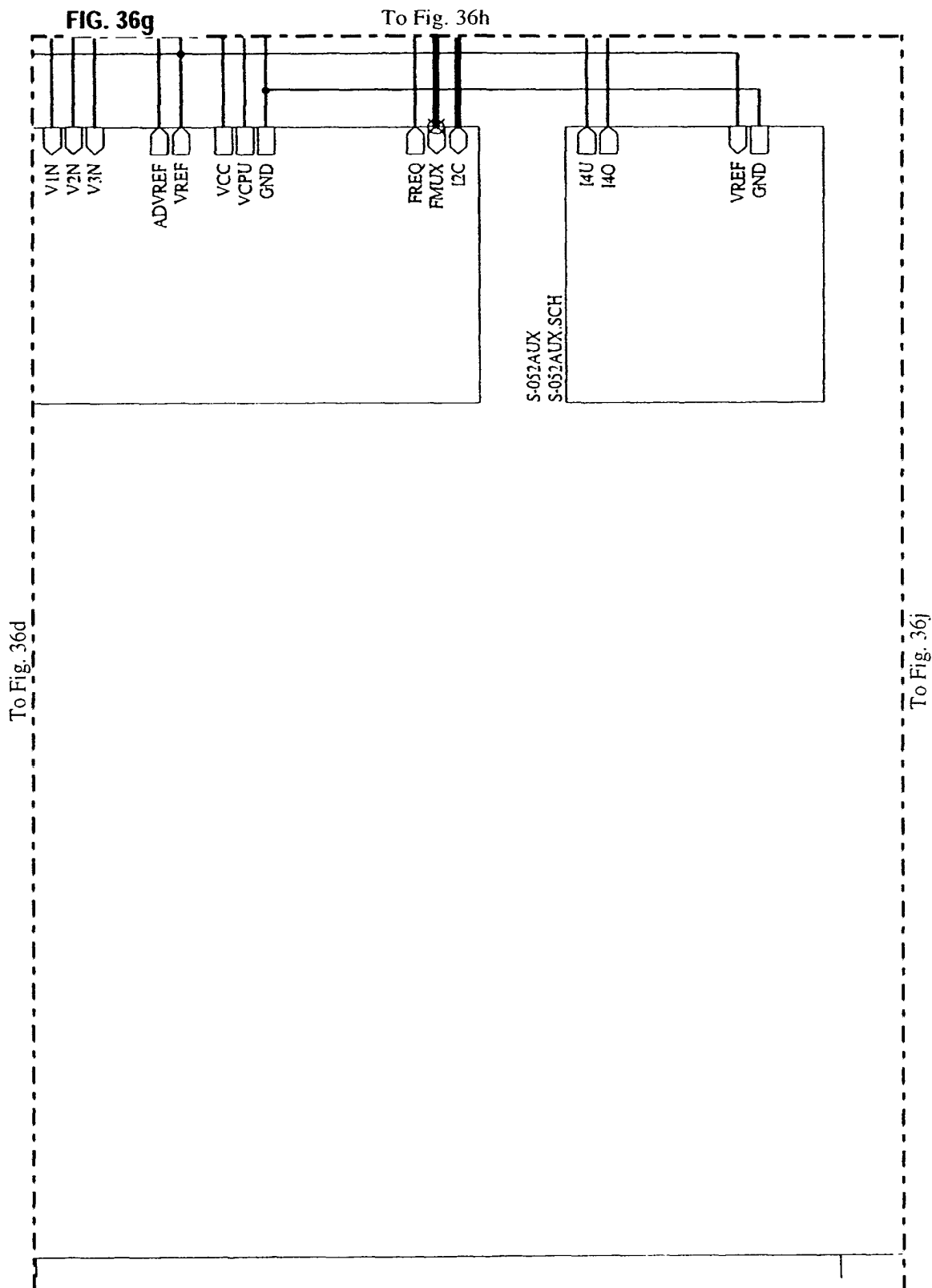


FIG. 36f





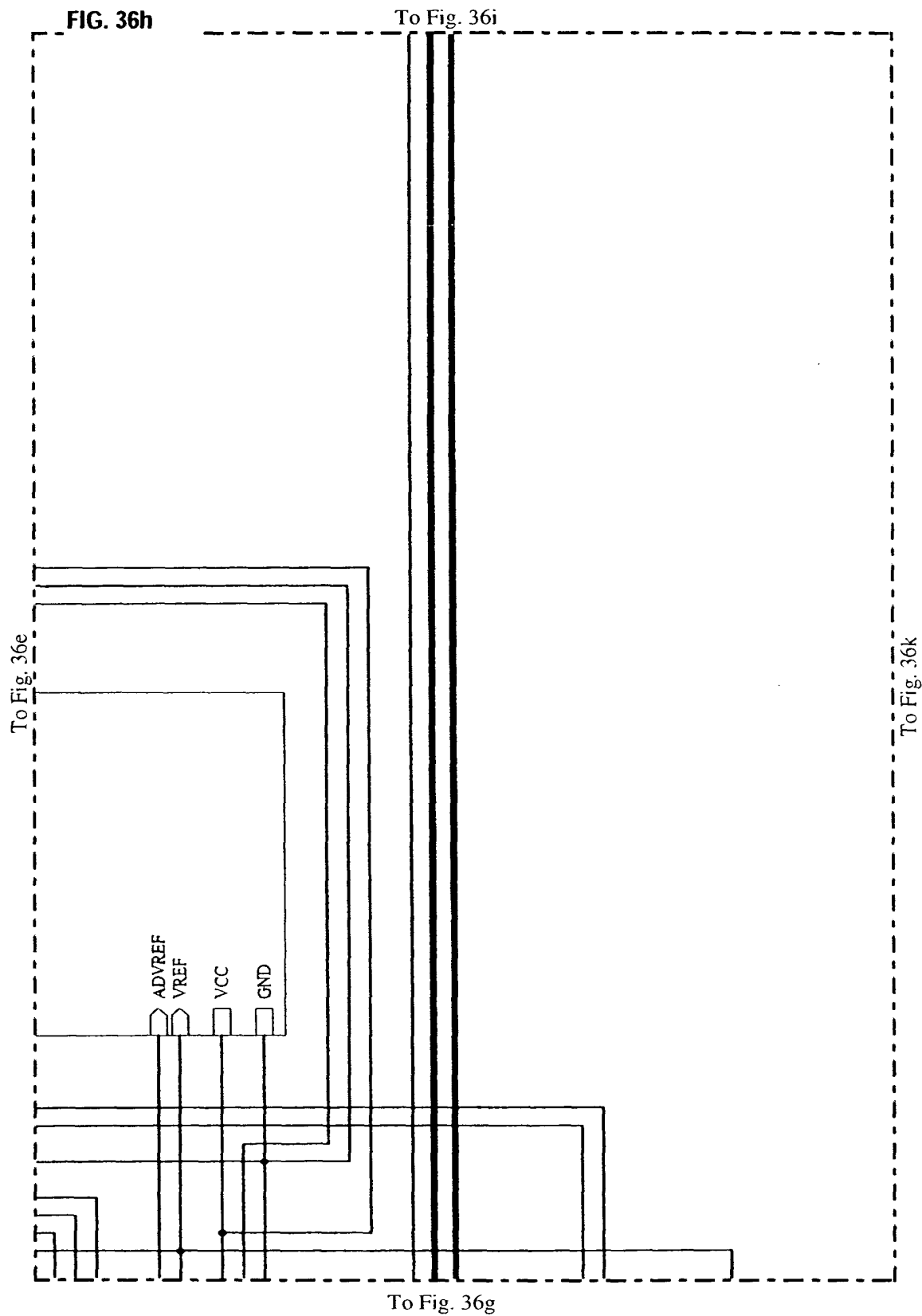


FIG. 36i

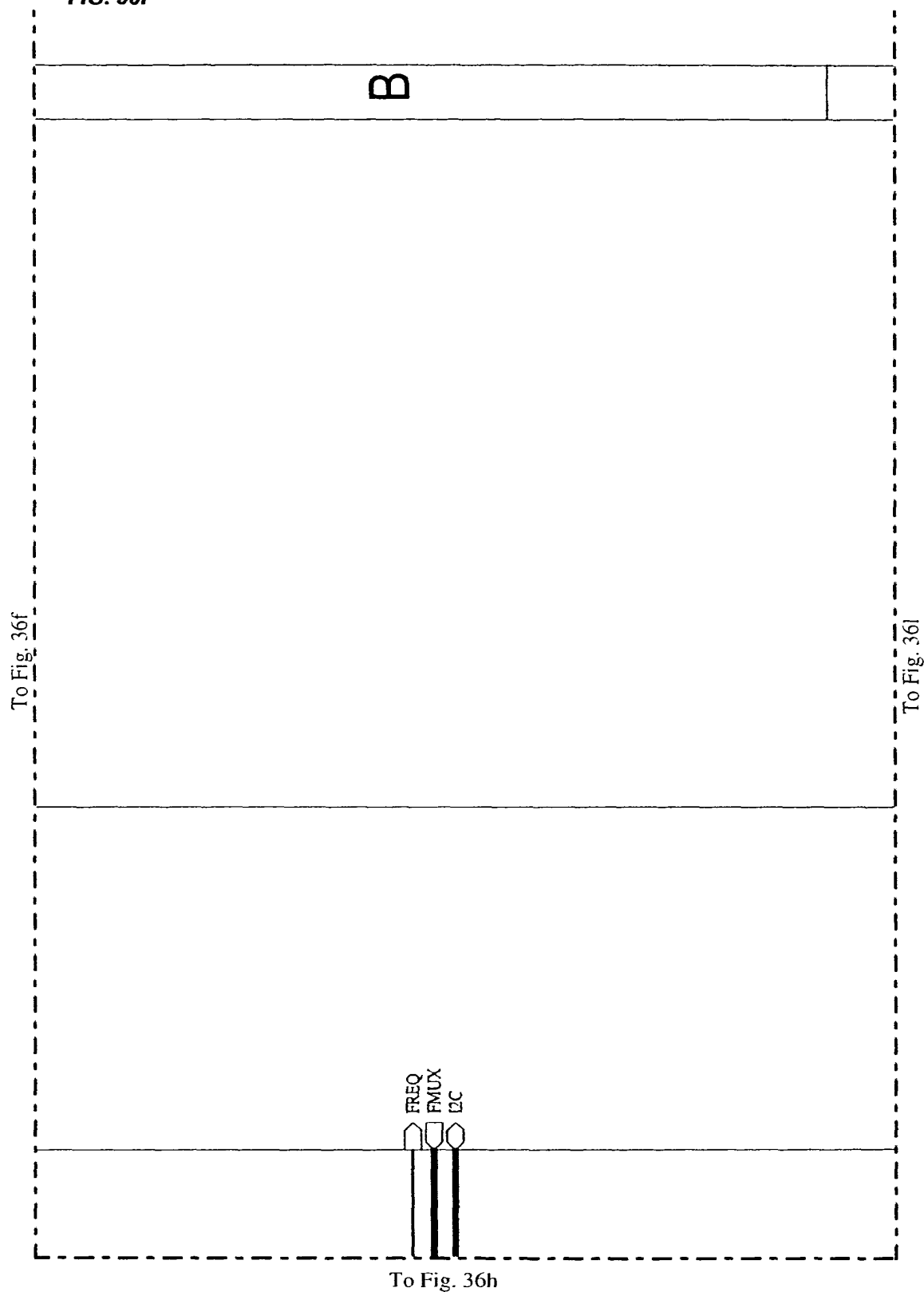


FIG. 36j

To Fig. 36k

To Fig. 36g

2

1

FIG. 36k

To Fig. 36l

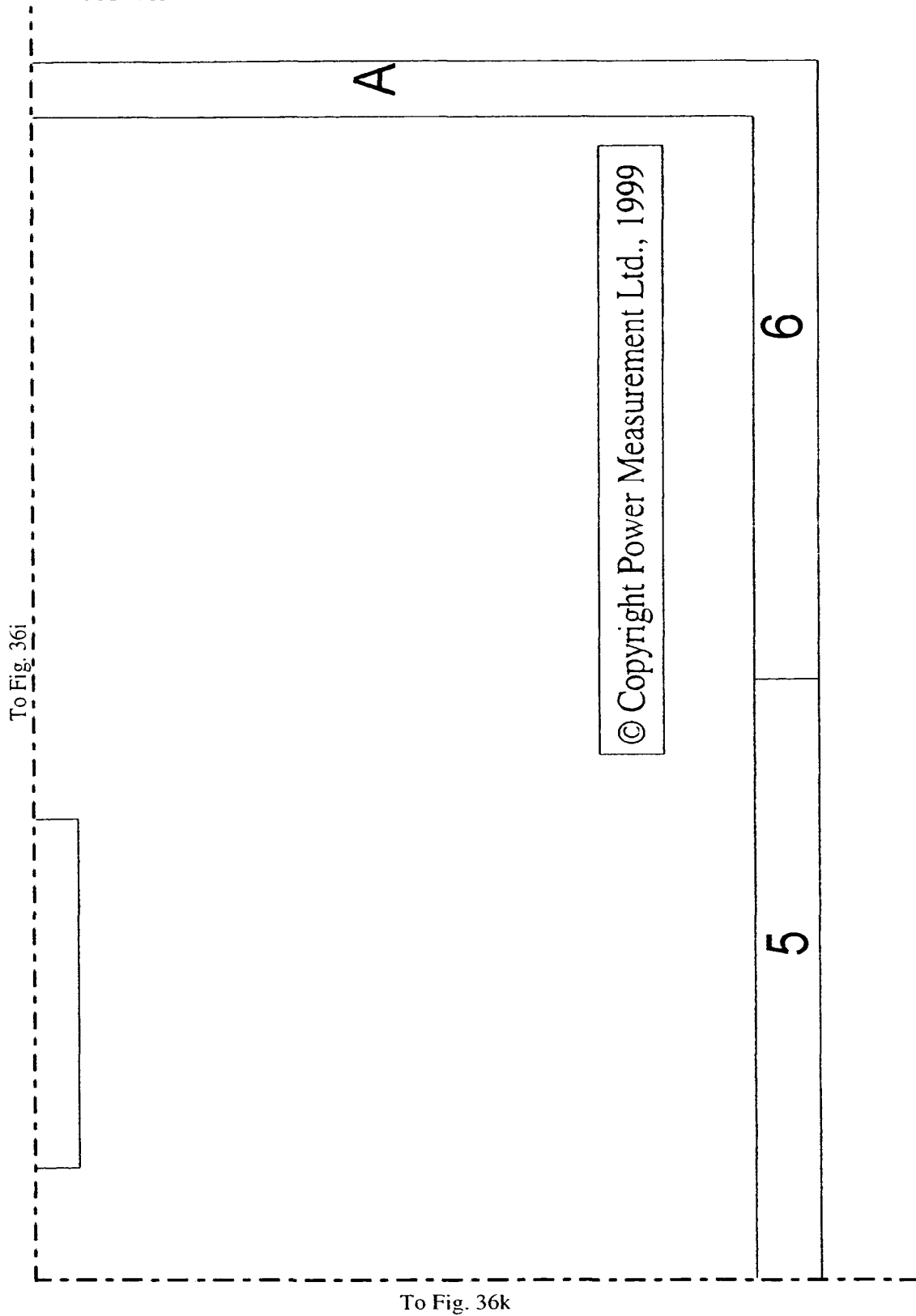
To Fig. 36h

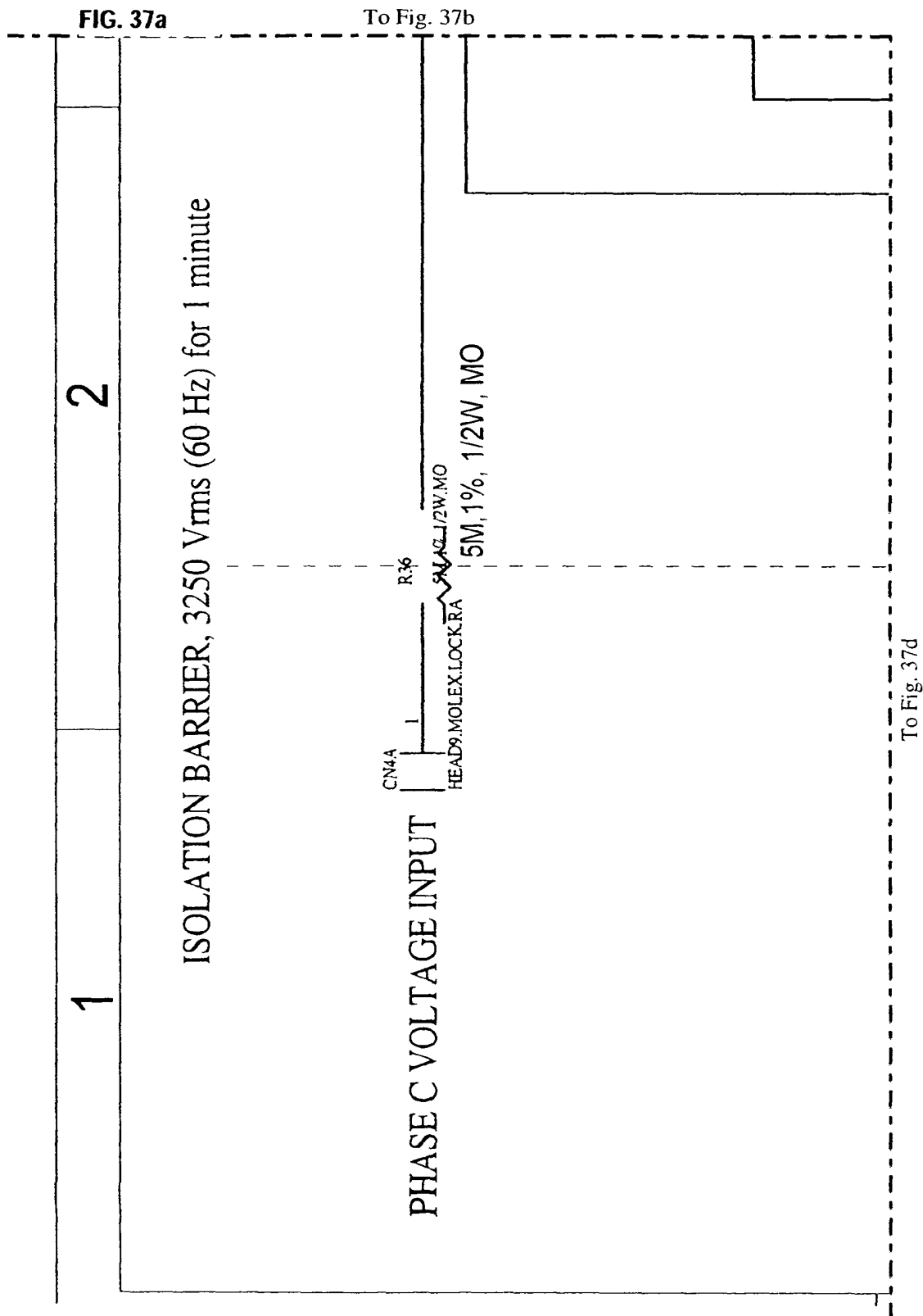
4

3

To Fig. 36j

FIG. 36l





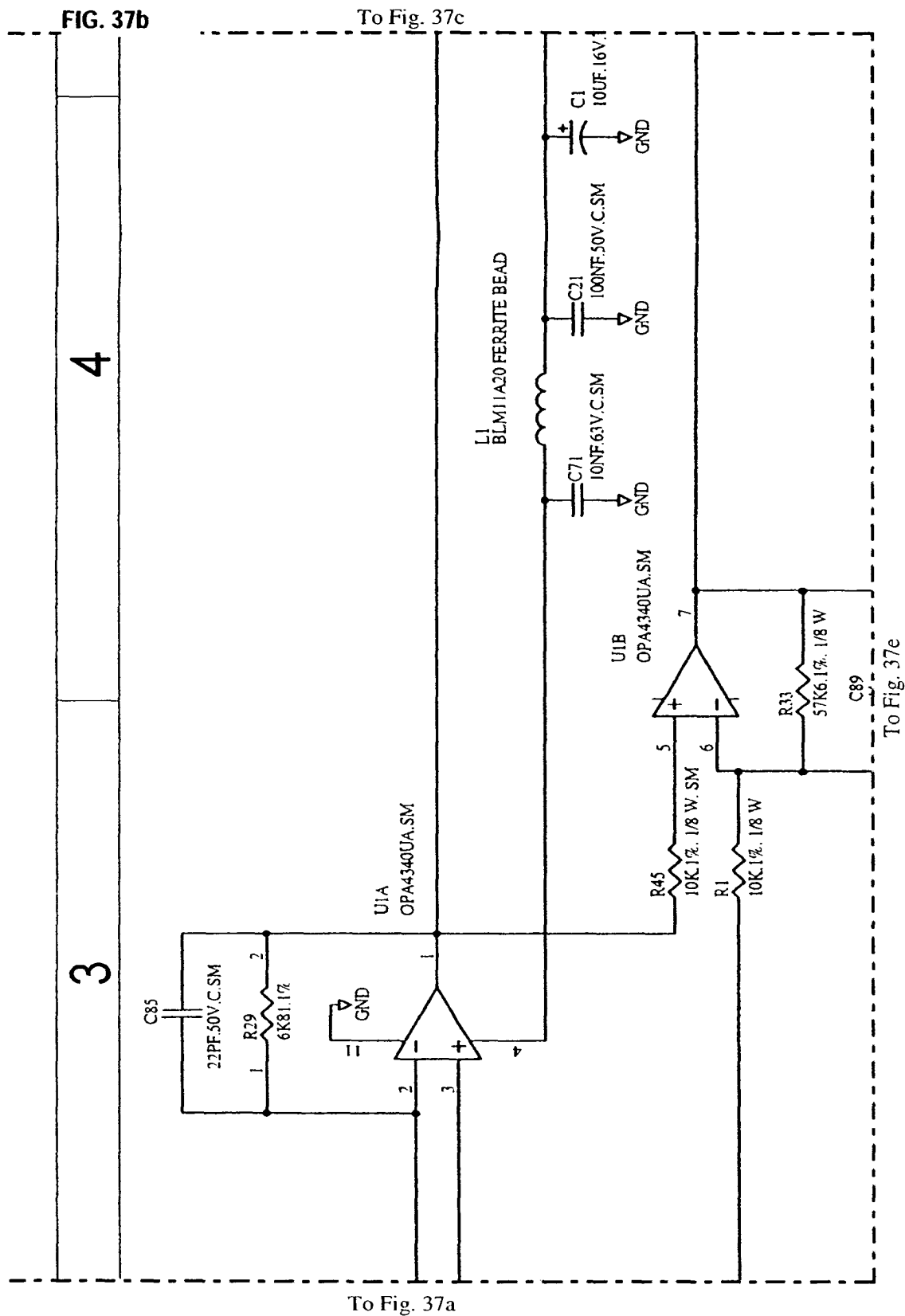
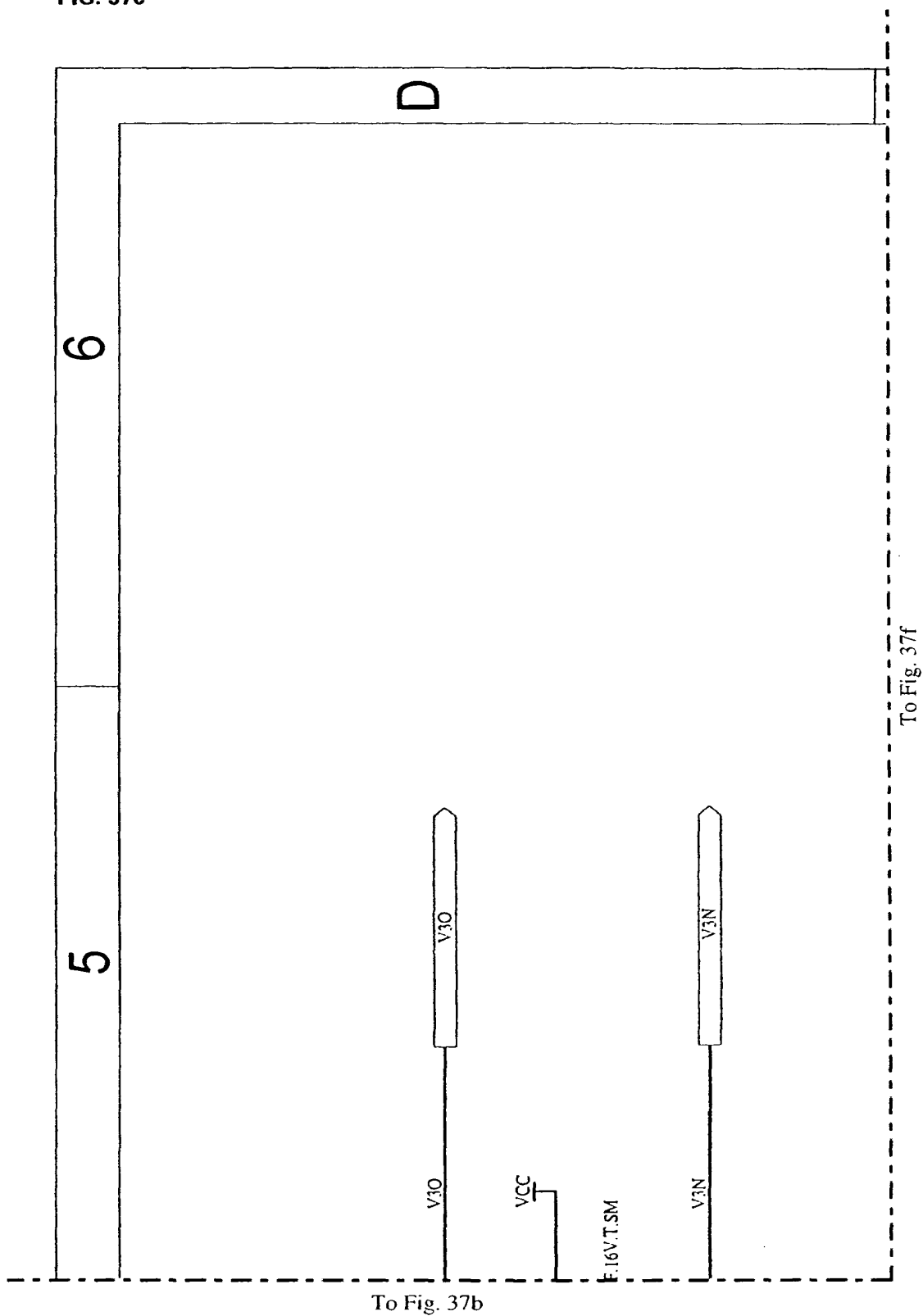
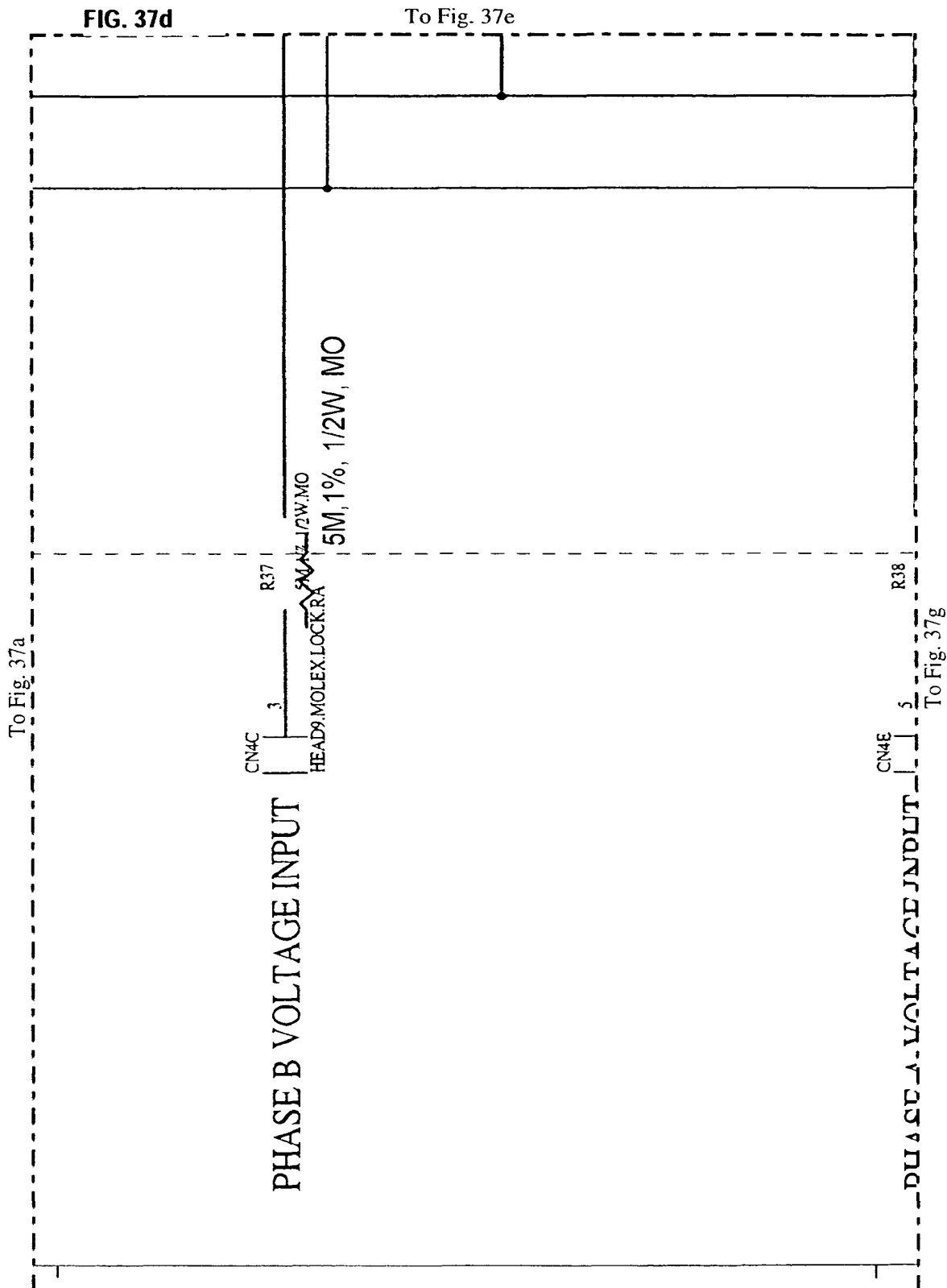


FIG. 37c





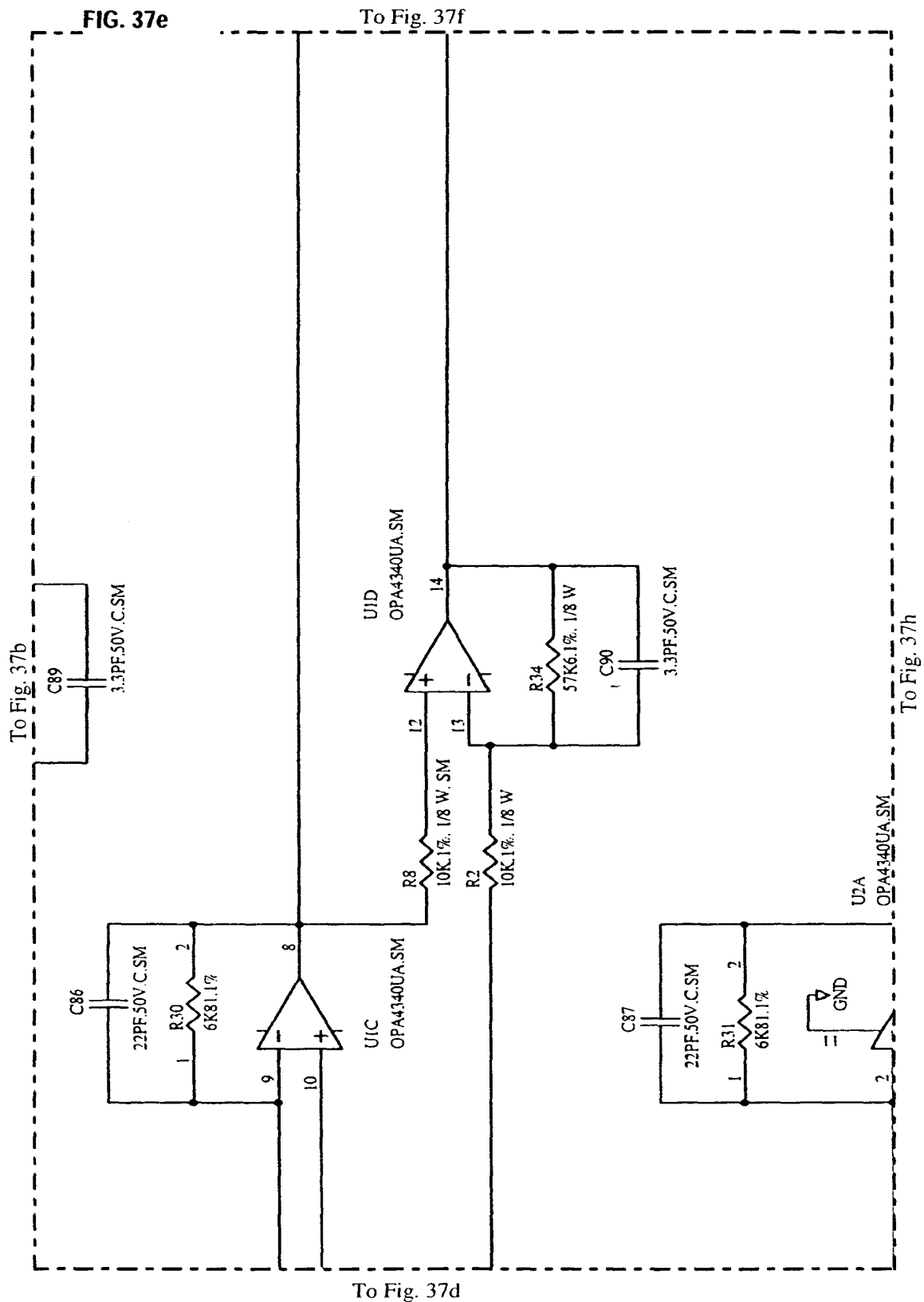
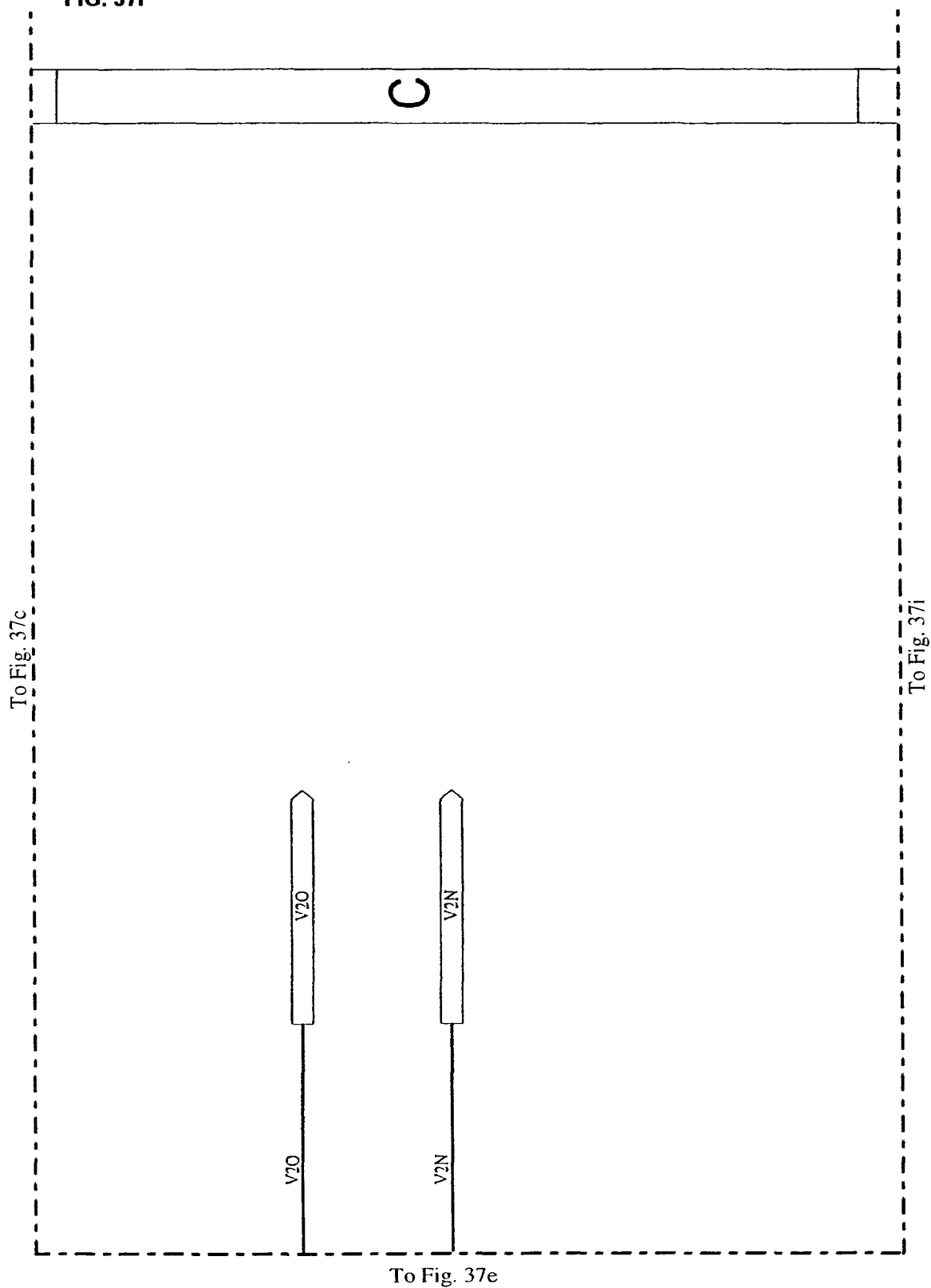
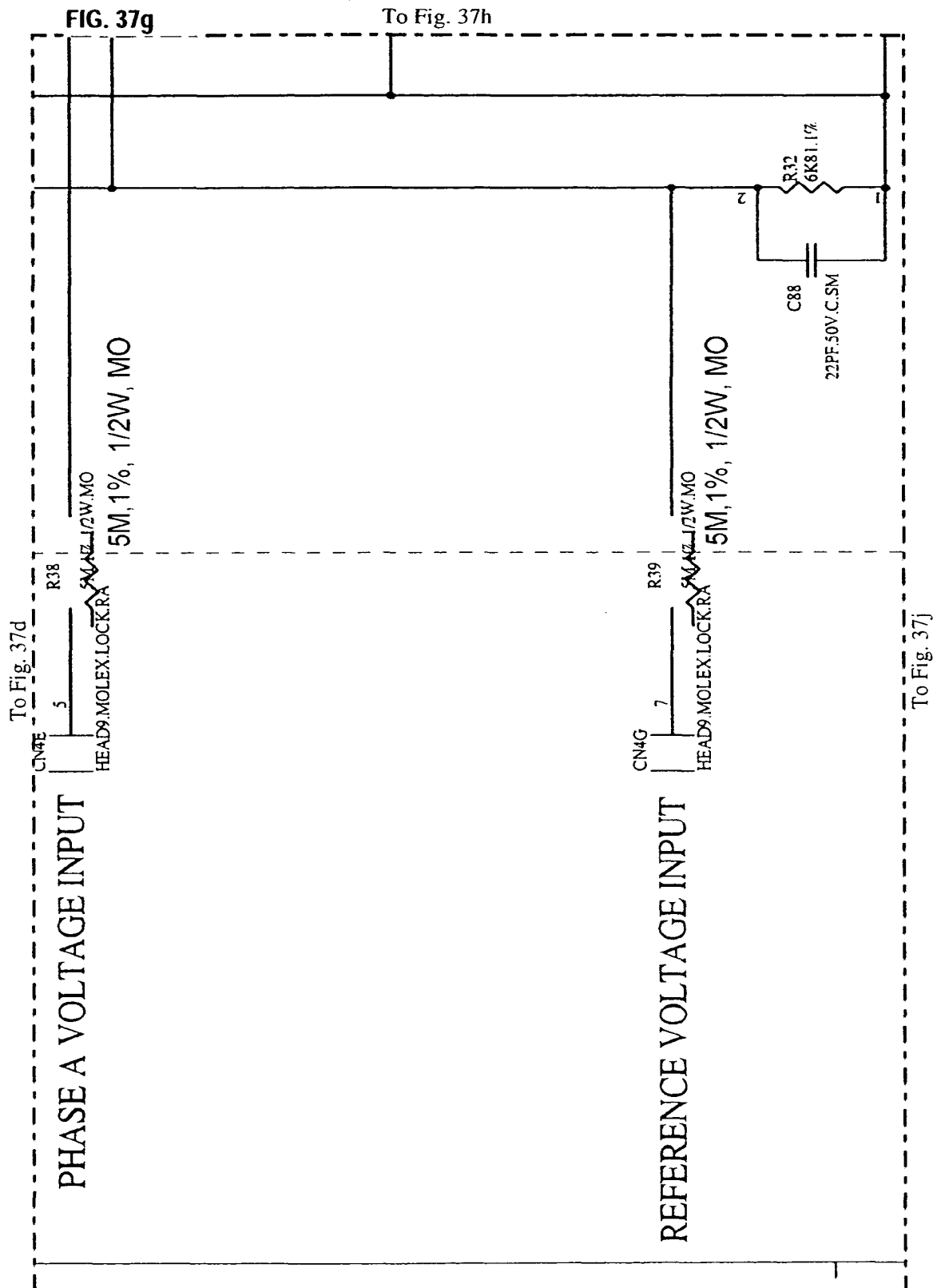


FIG. 37f





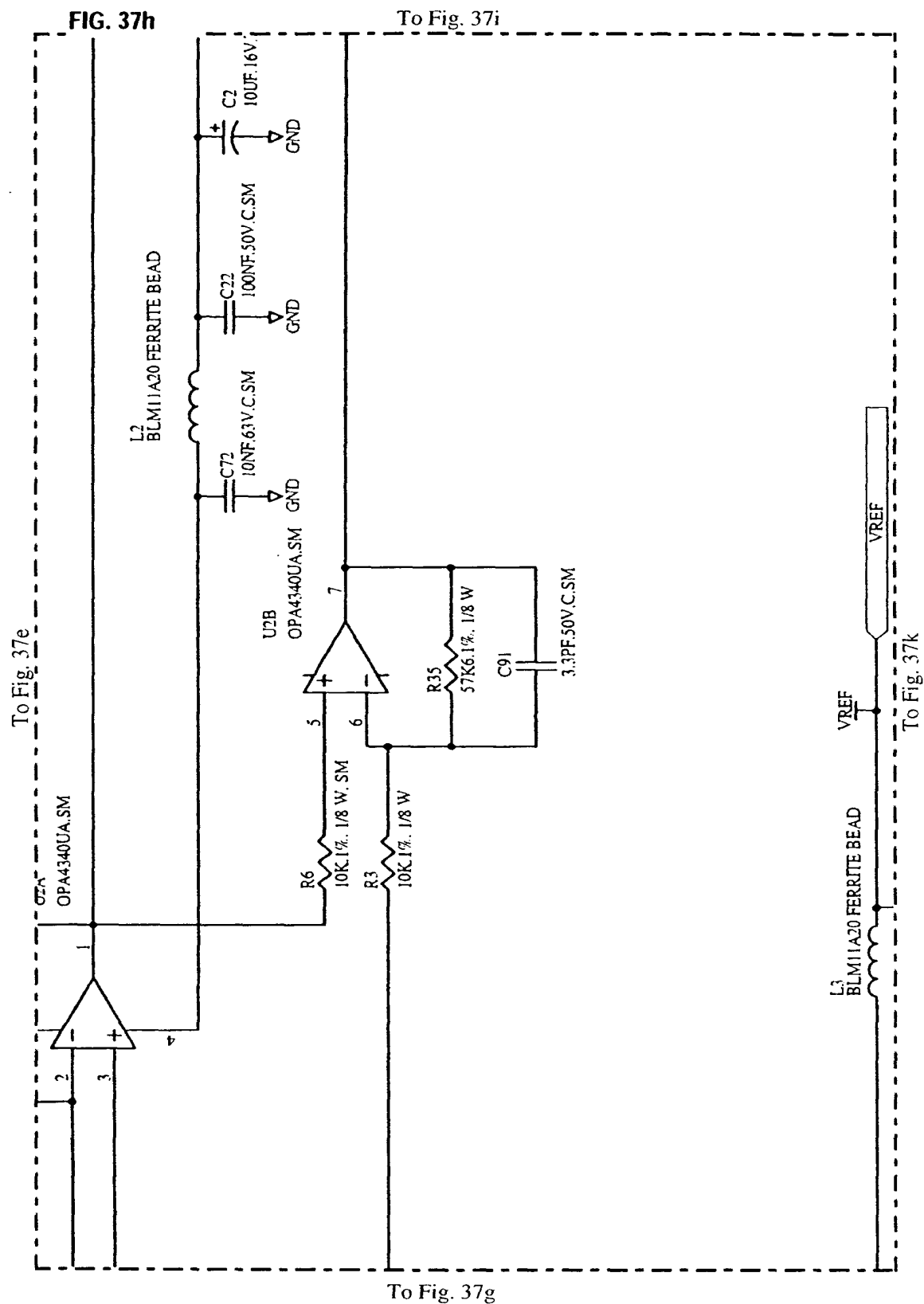
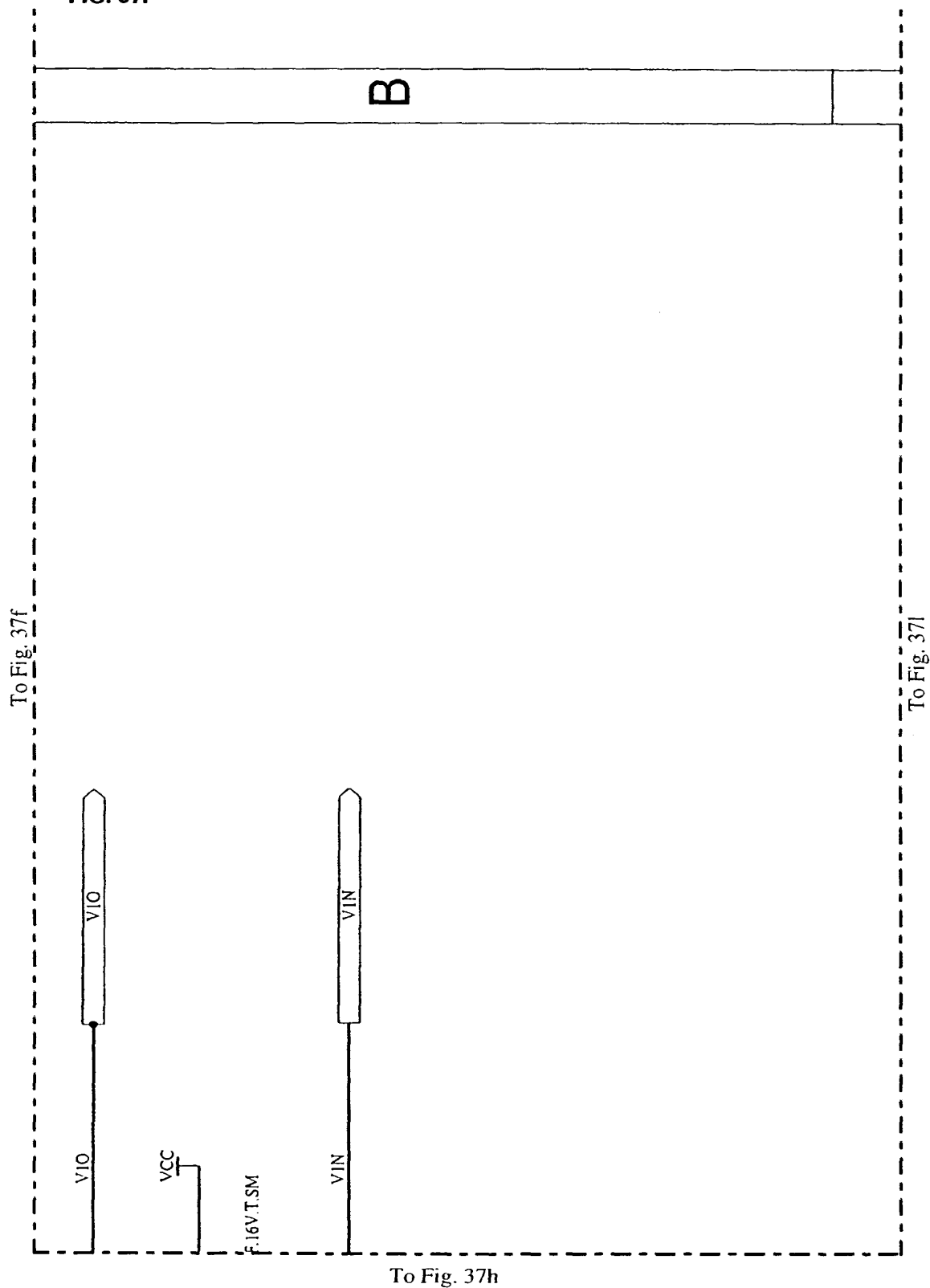
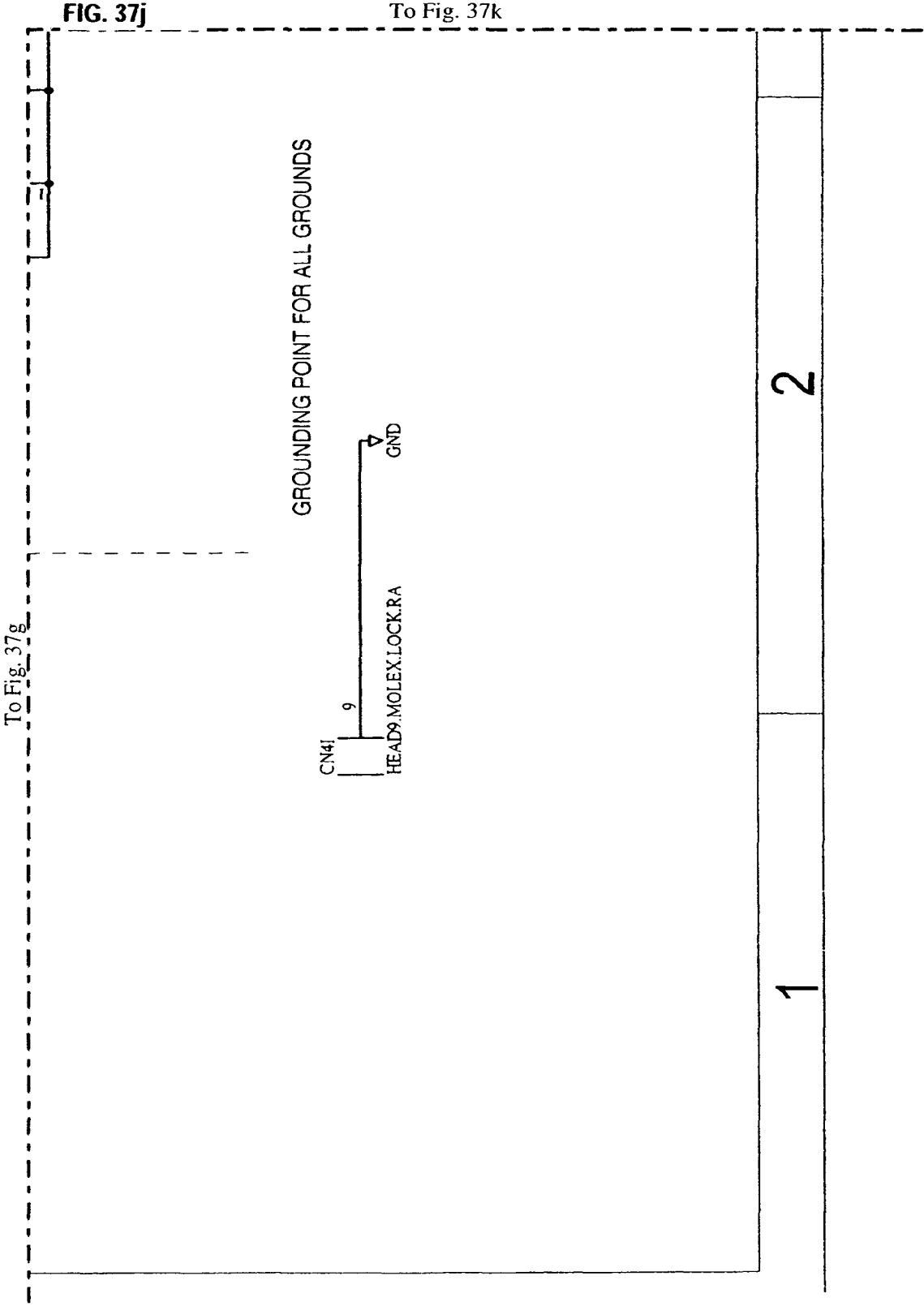


FIG. 37i





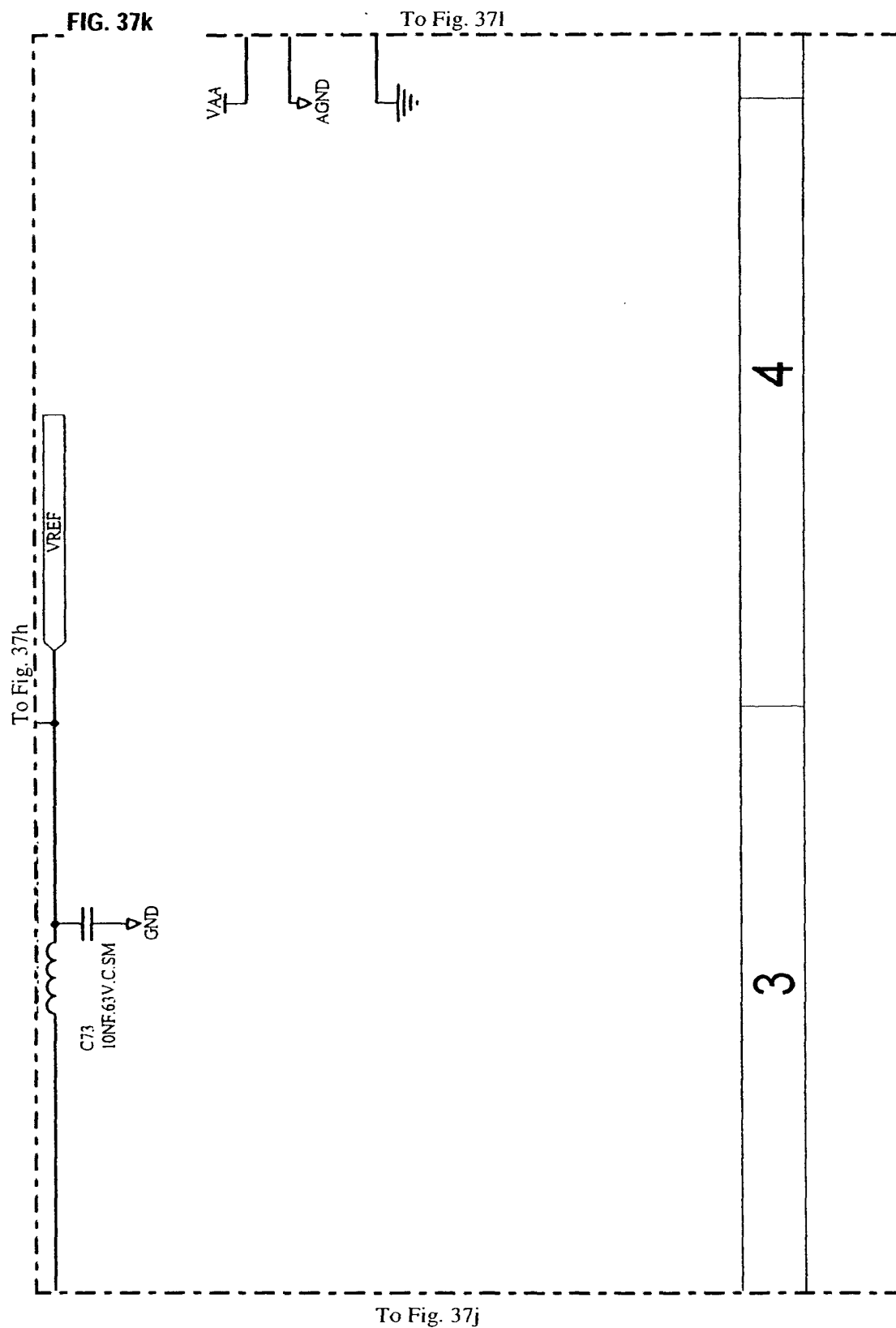


FIG. 37l

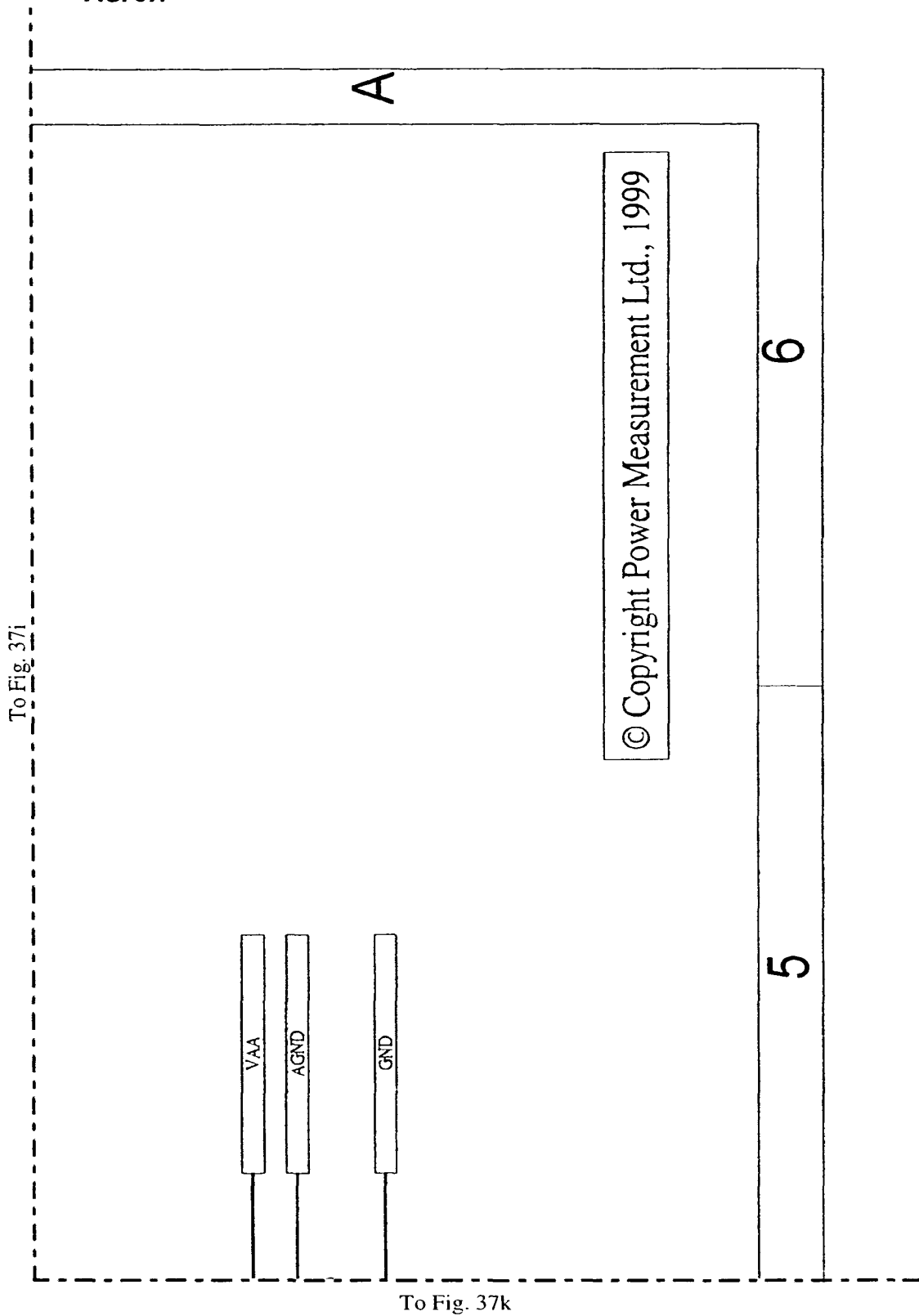
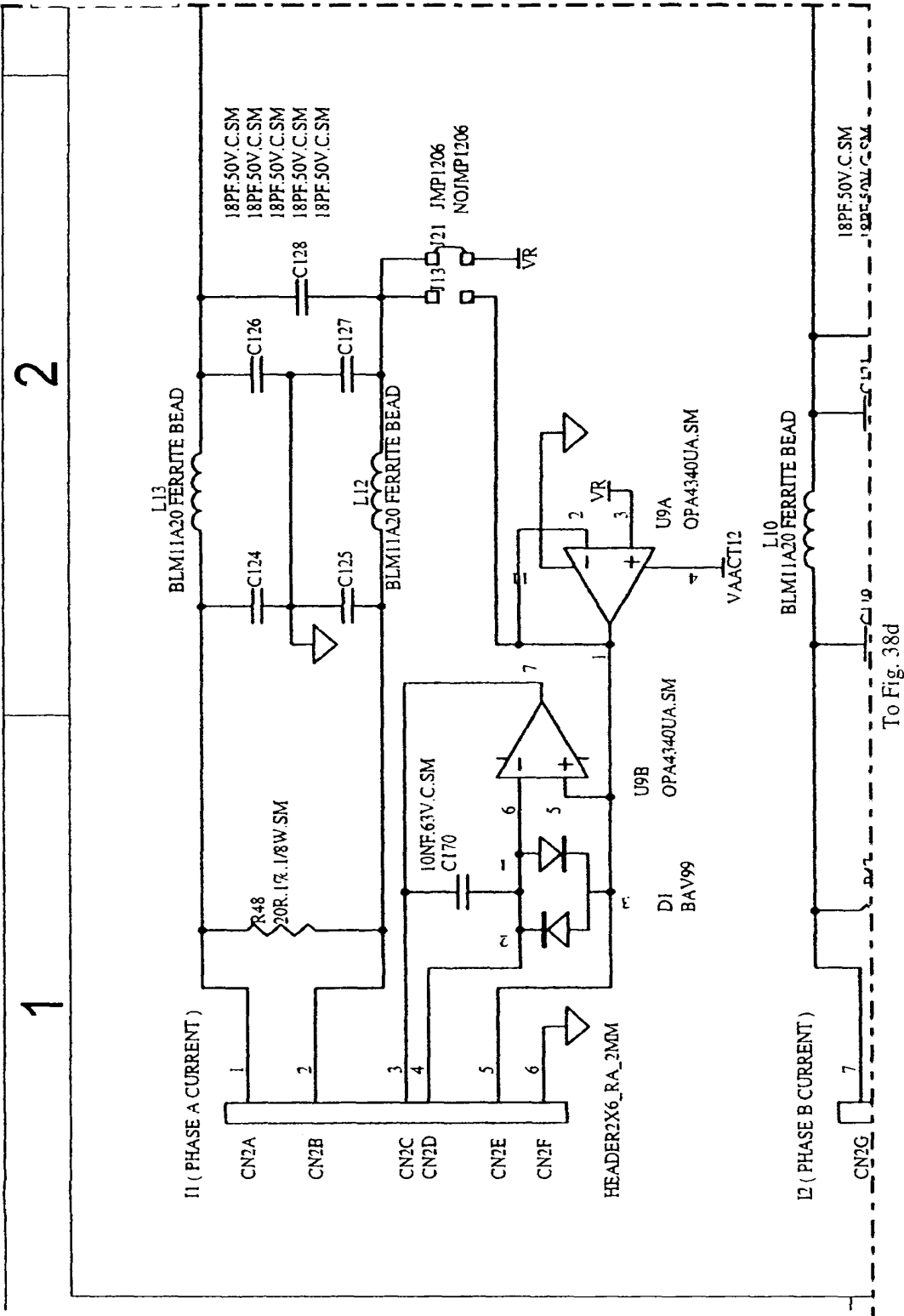


FIG. 38a

To Fig. 38b



To Fig. 38d

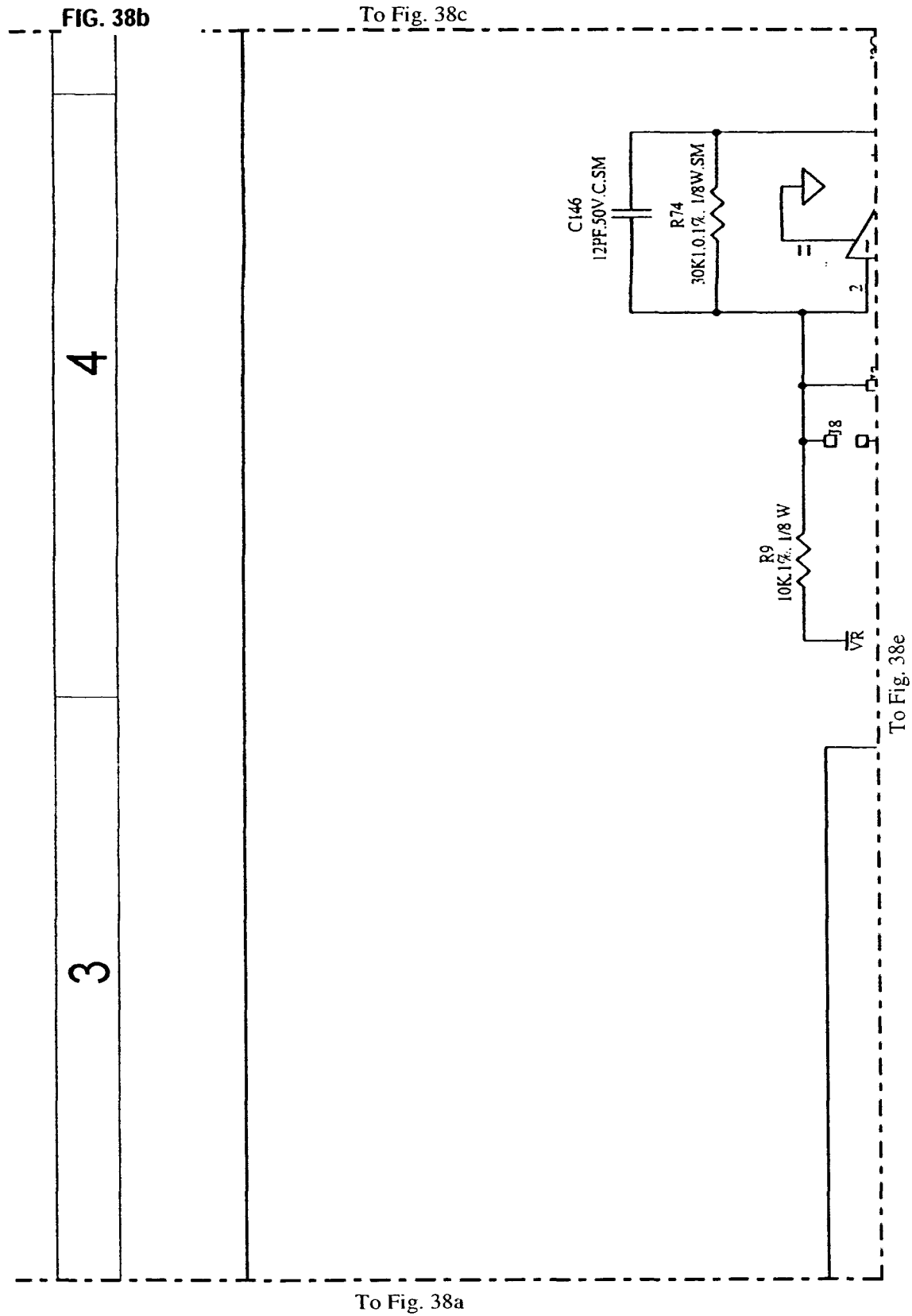
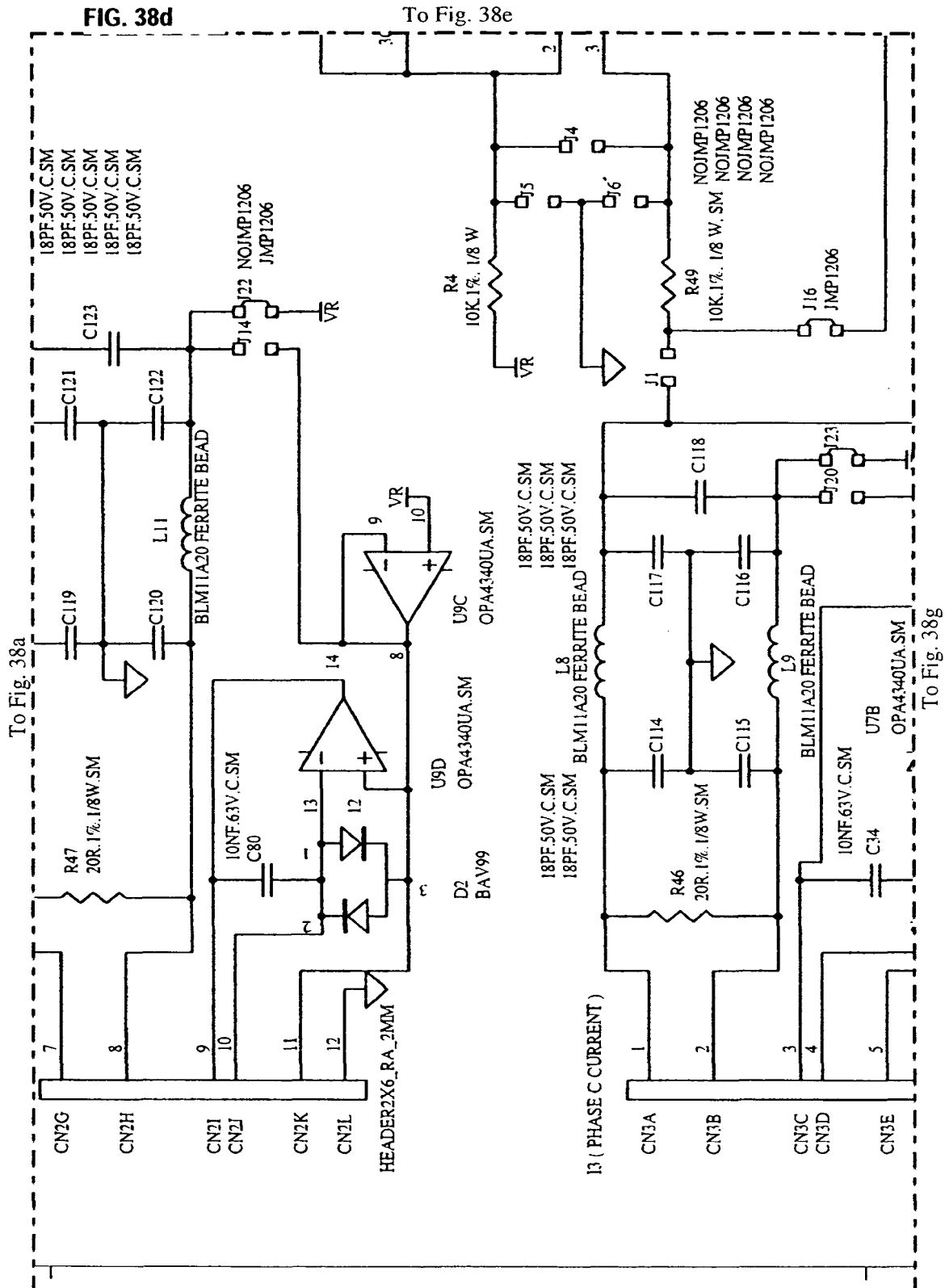
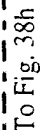


FIG. 38c

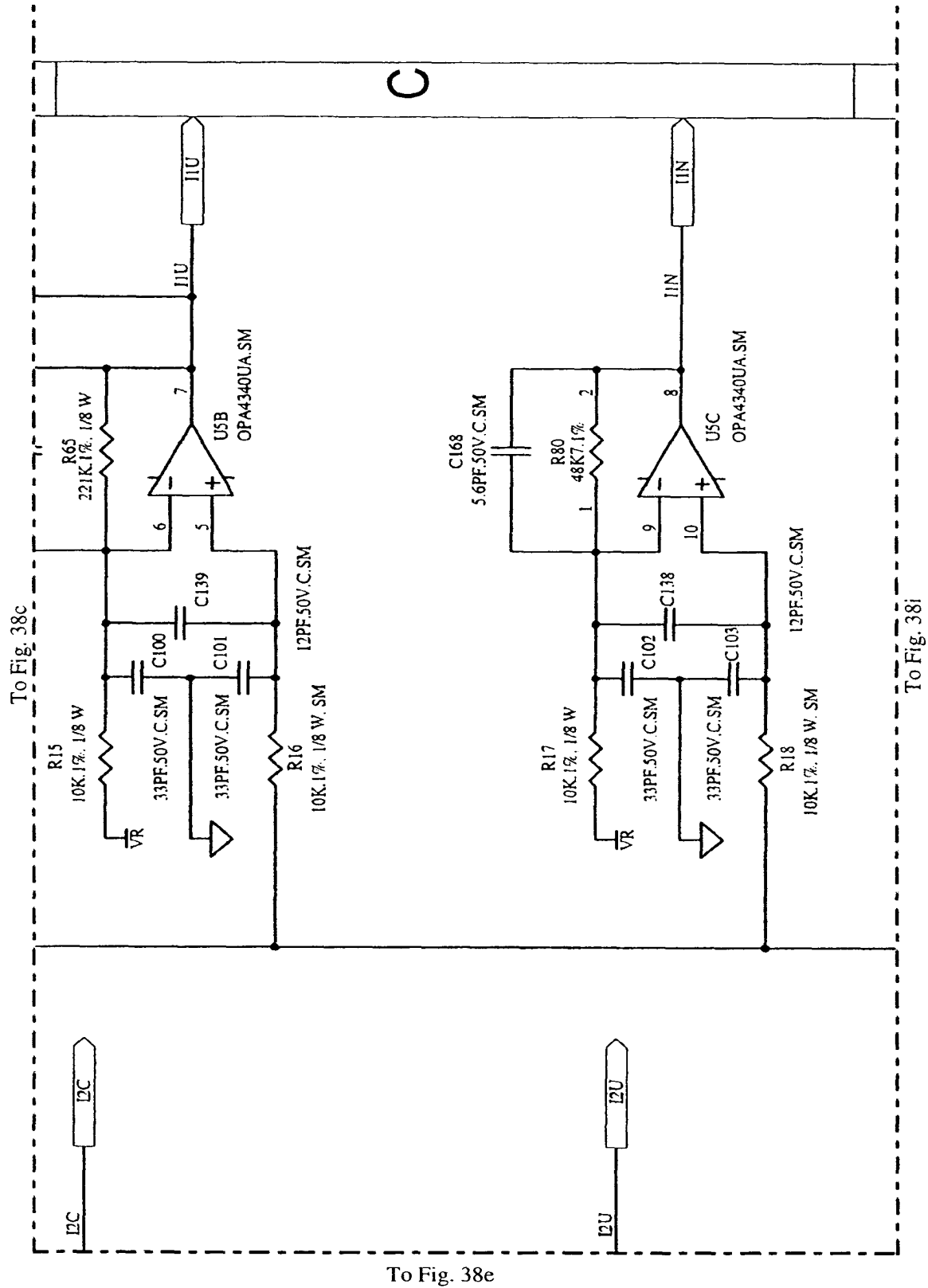


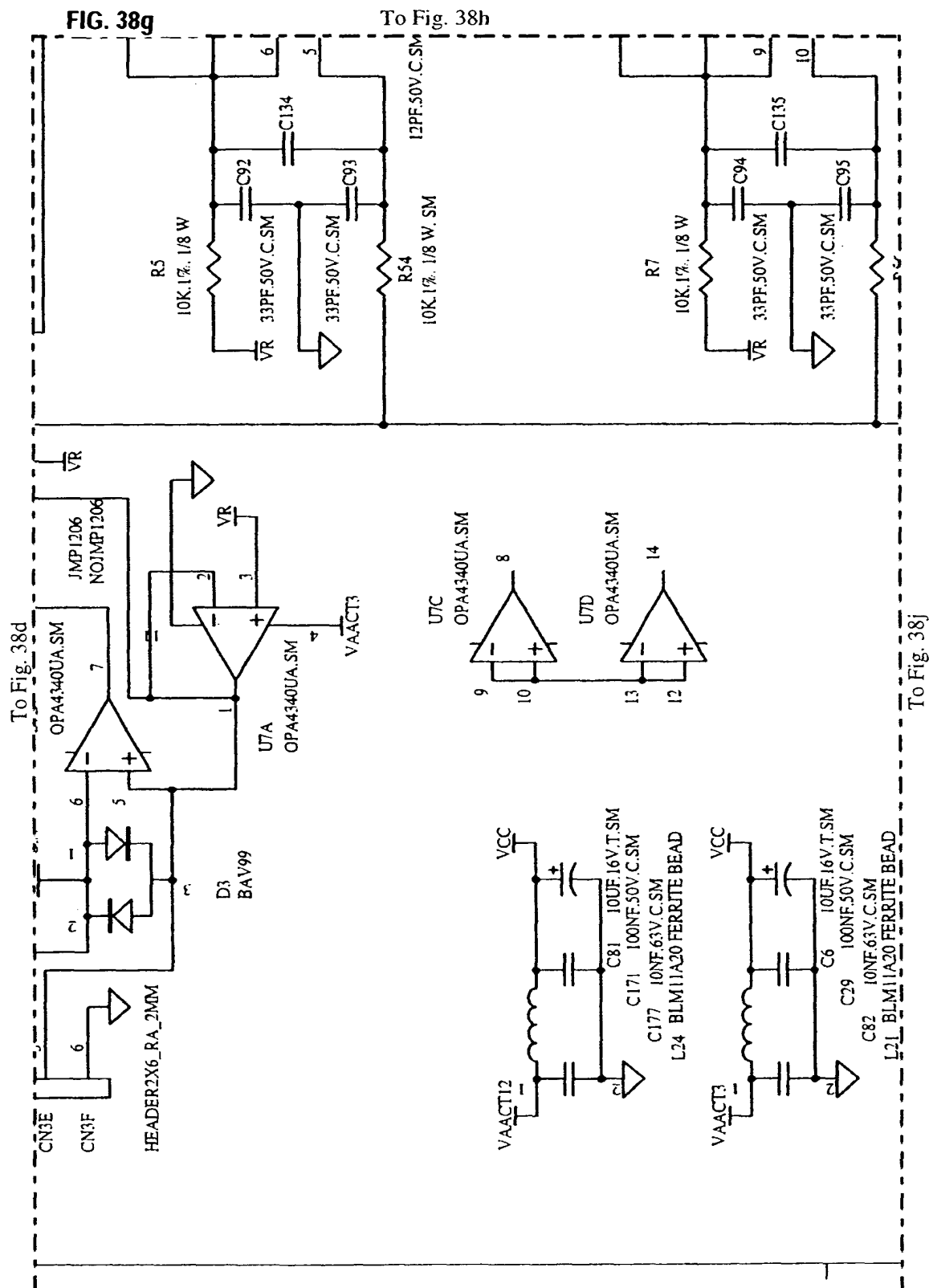
To Fig. 38f



To Fig. 38d

FIG. 38f





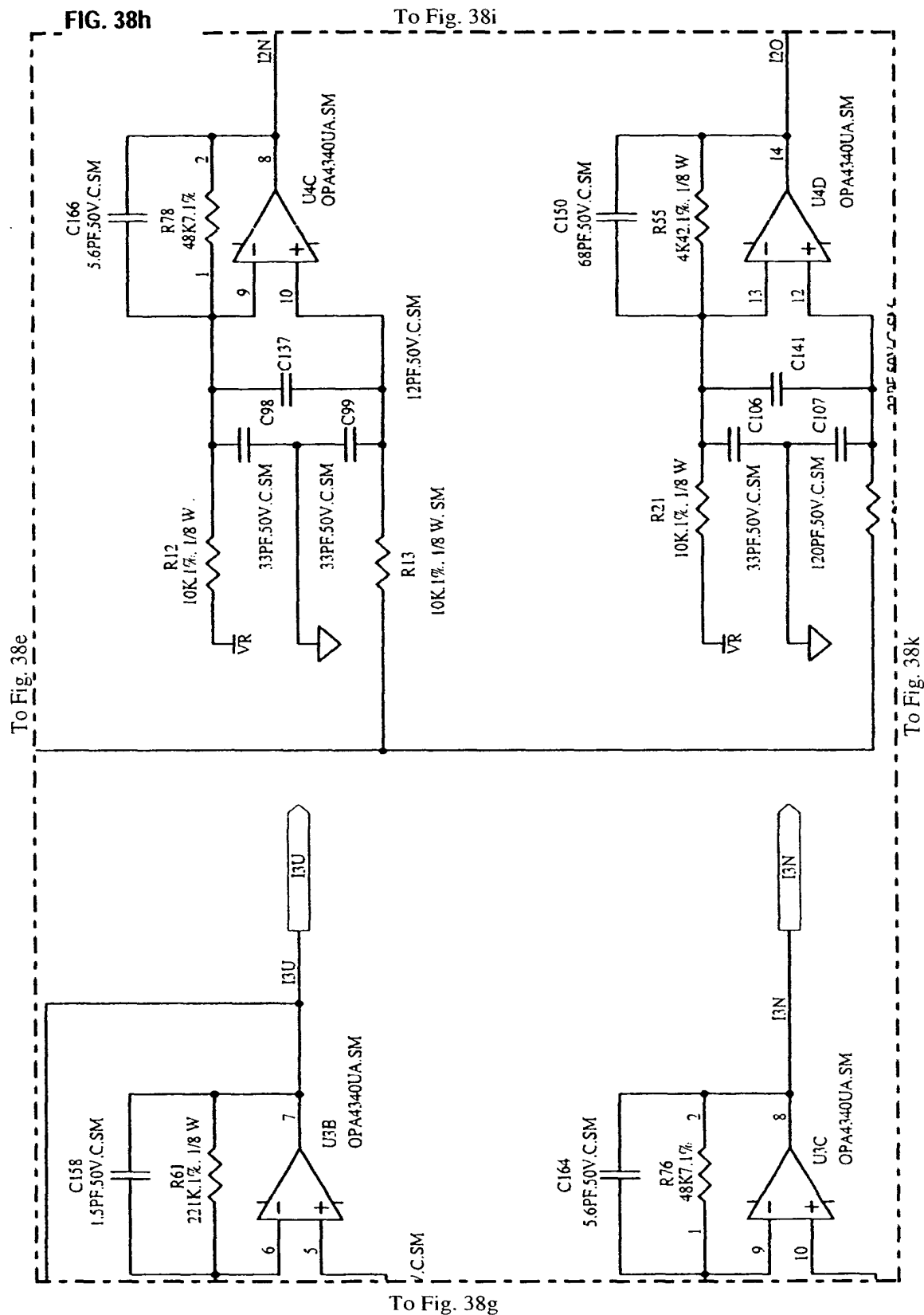
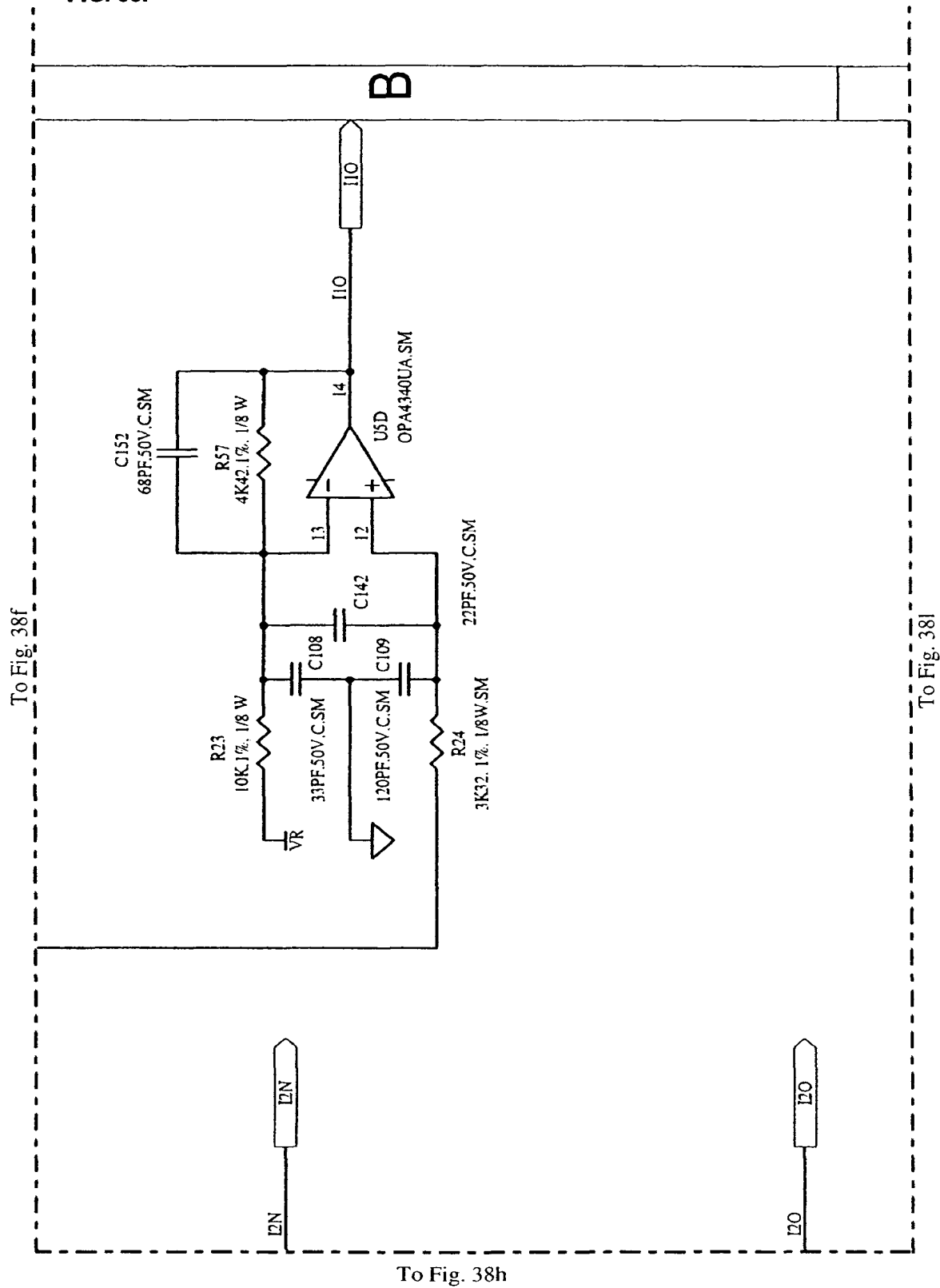
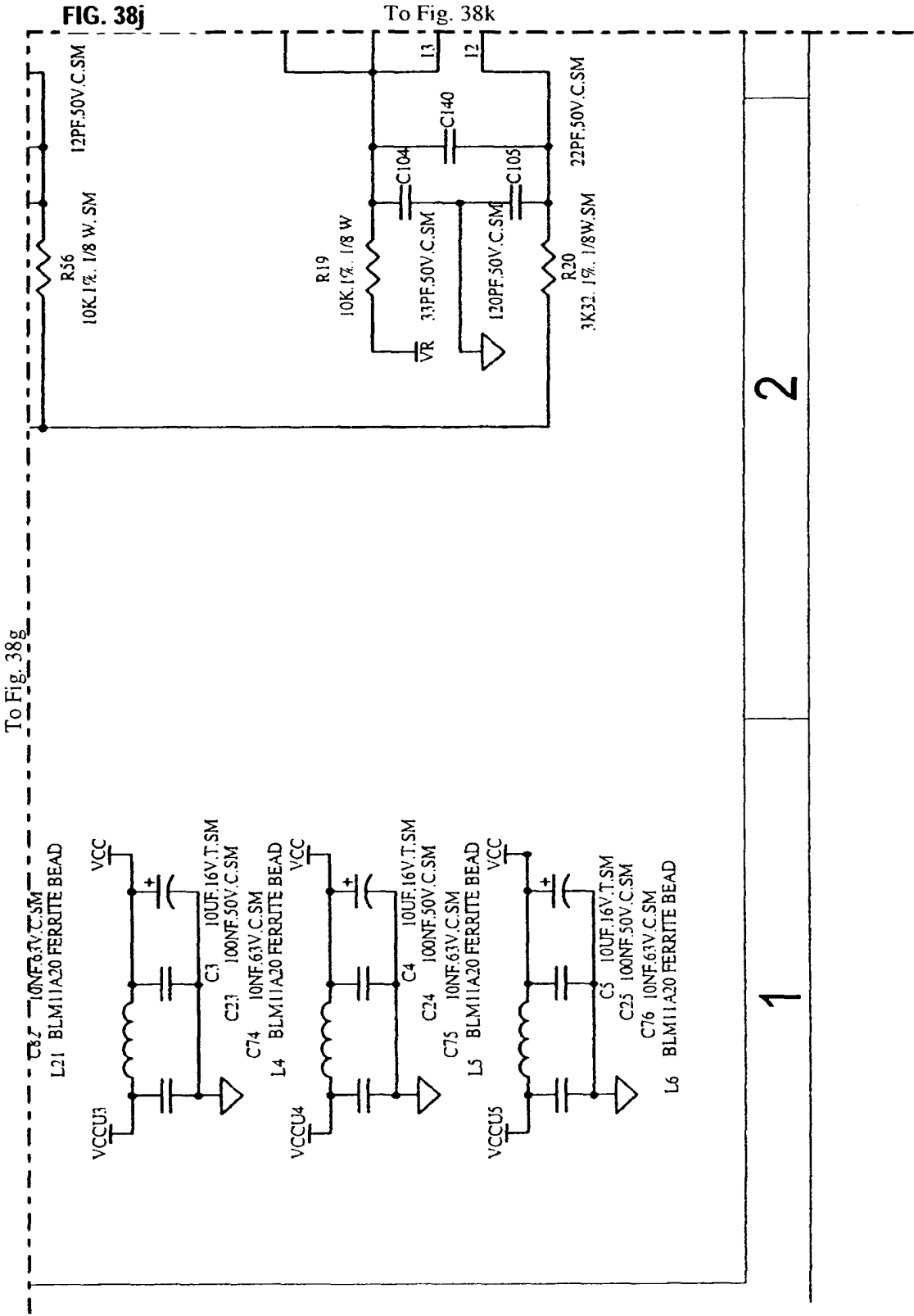


FIG. 38i





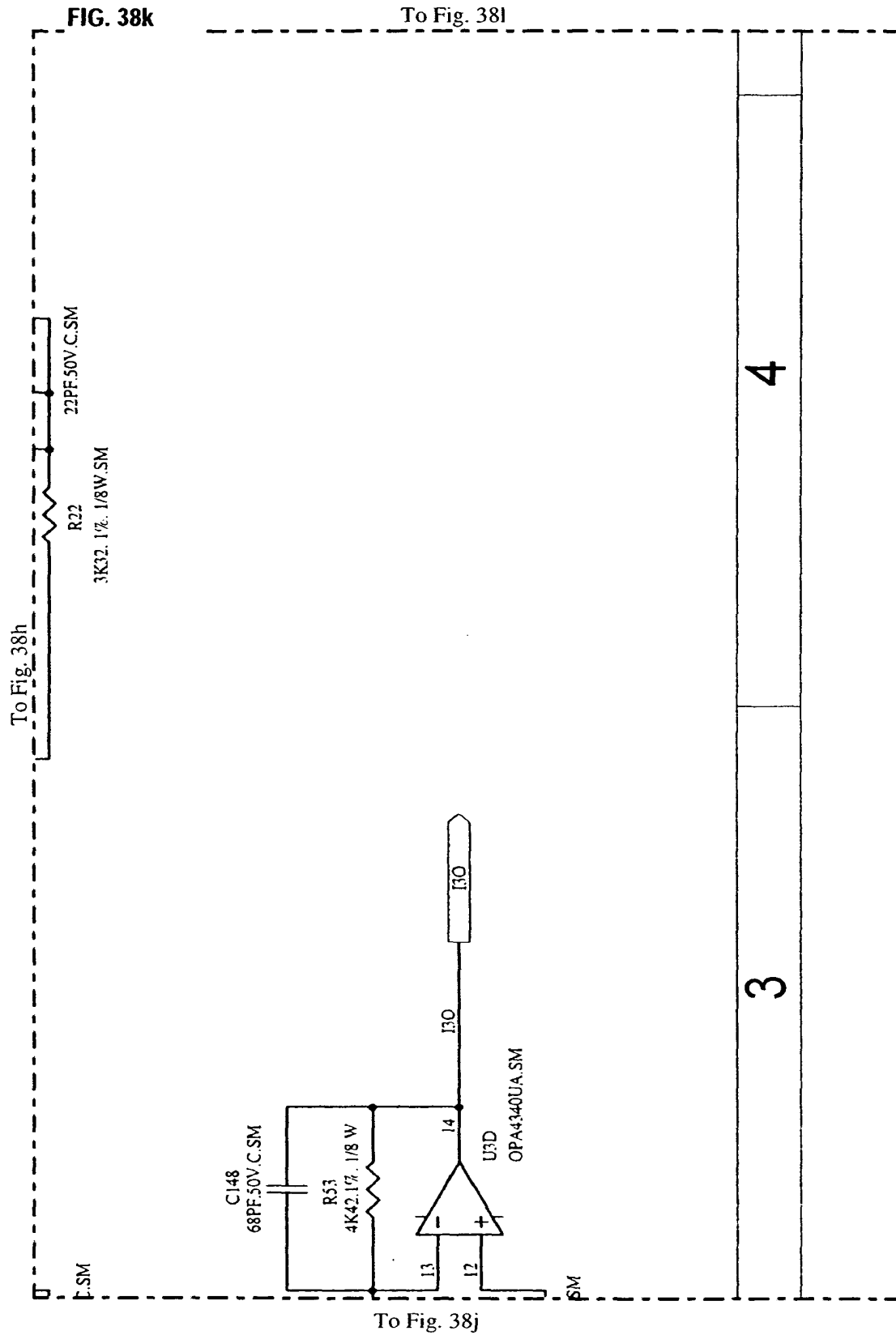


FIG. 38I

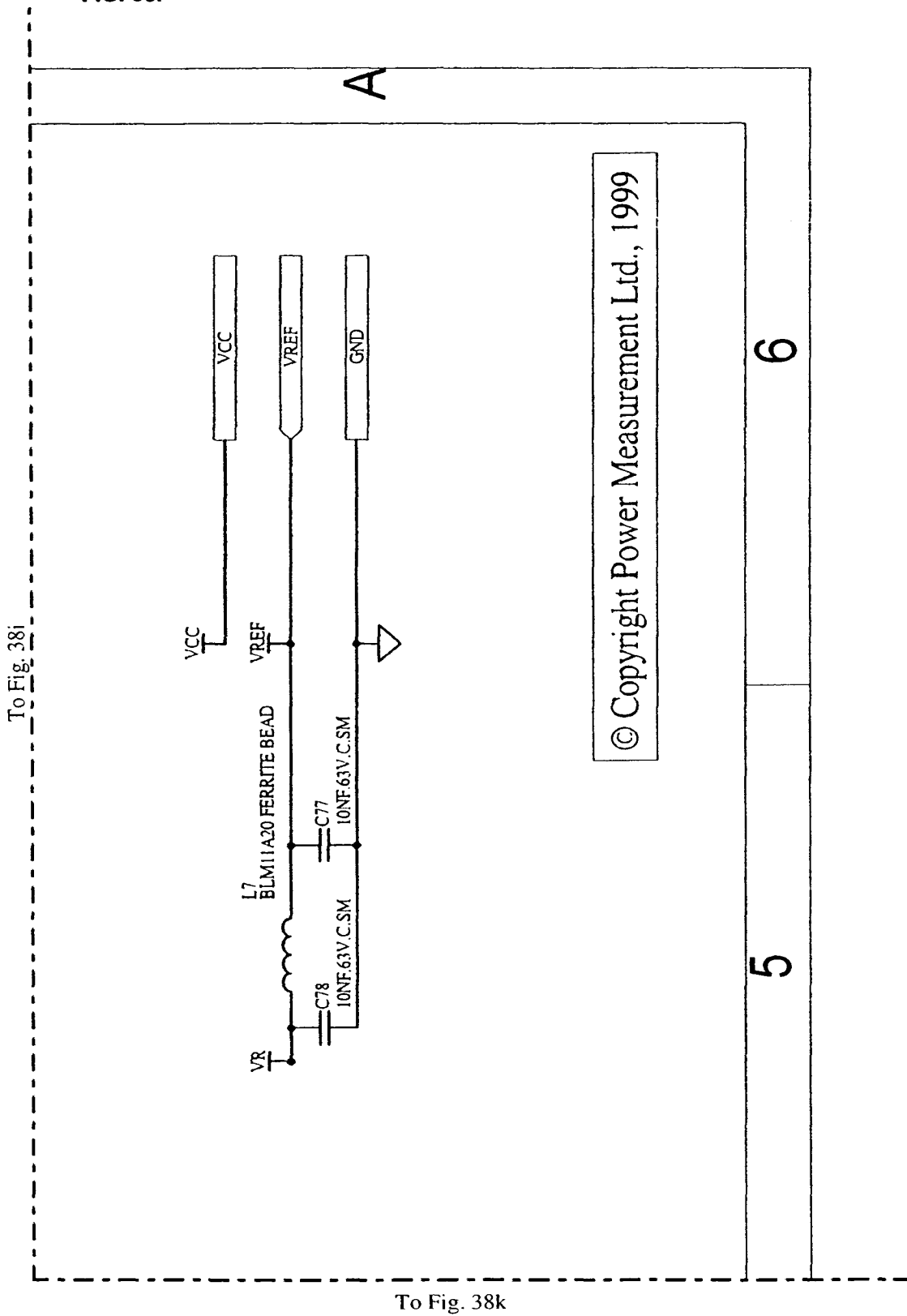
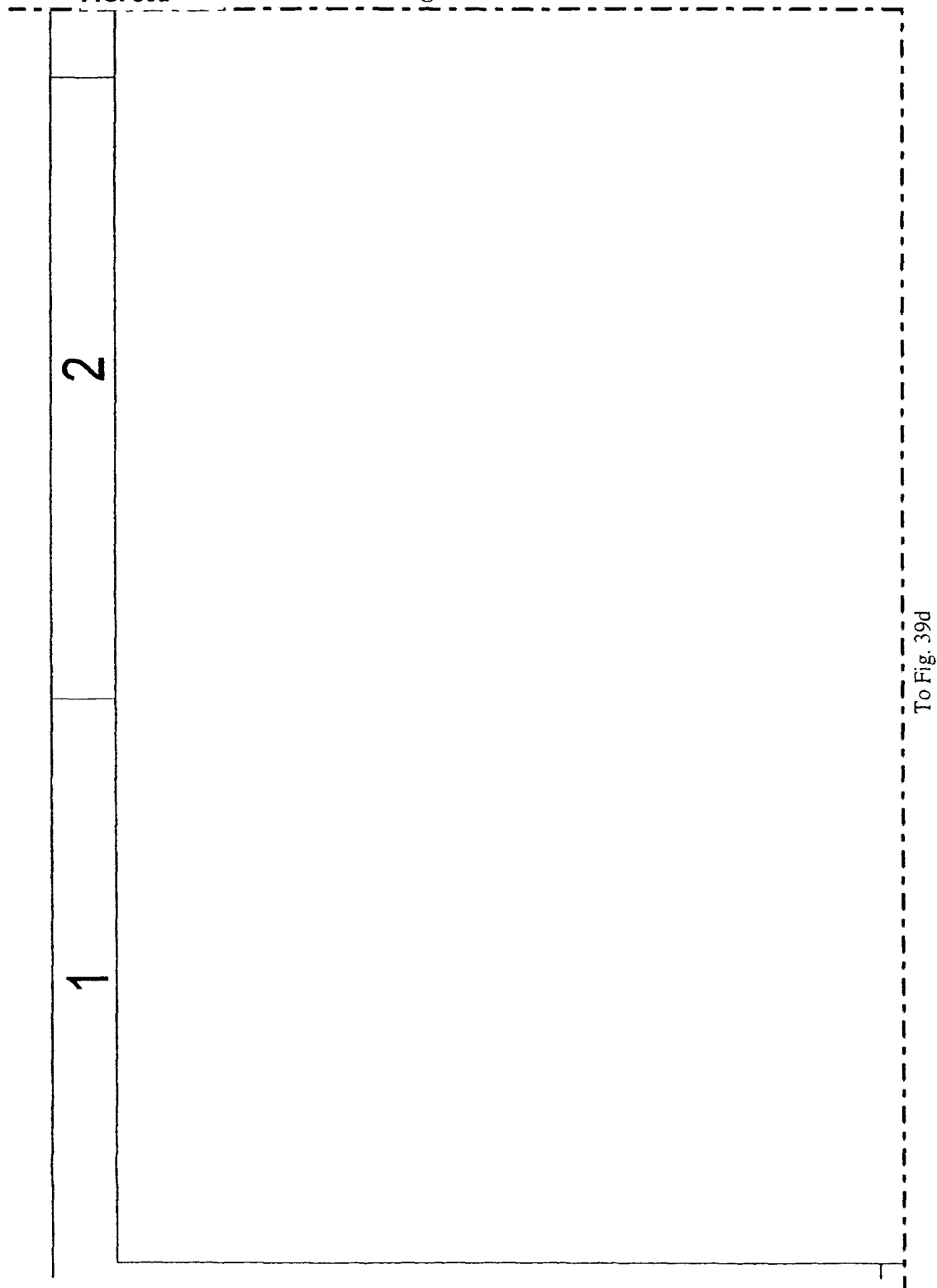


FIG. 39a

To Fig. 39b



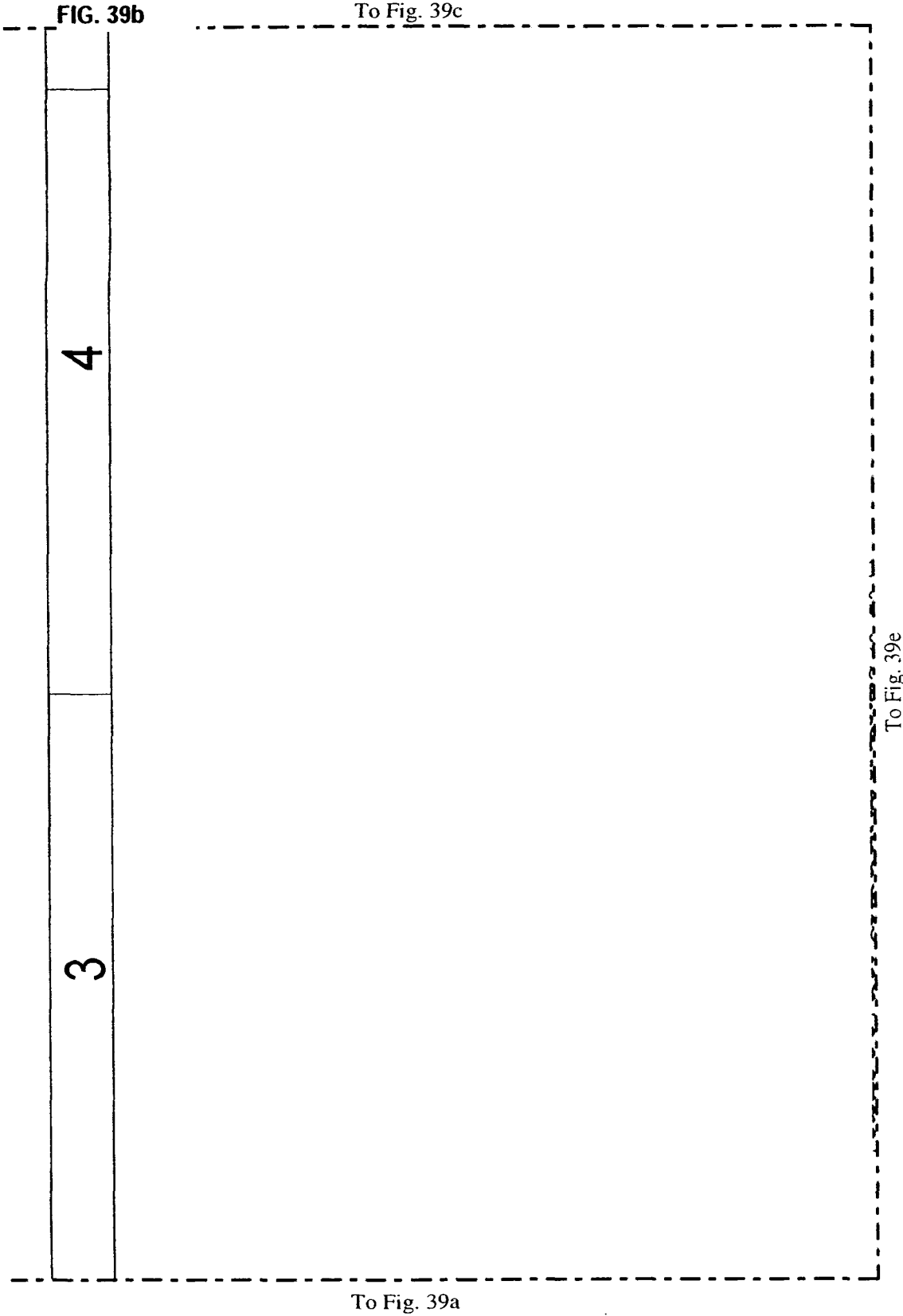
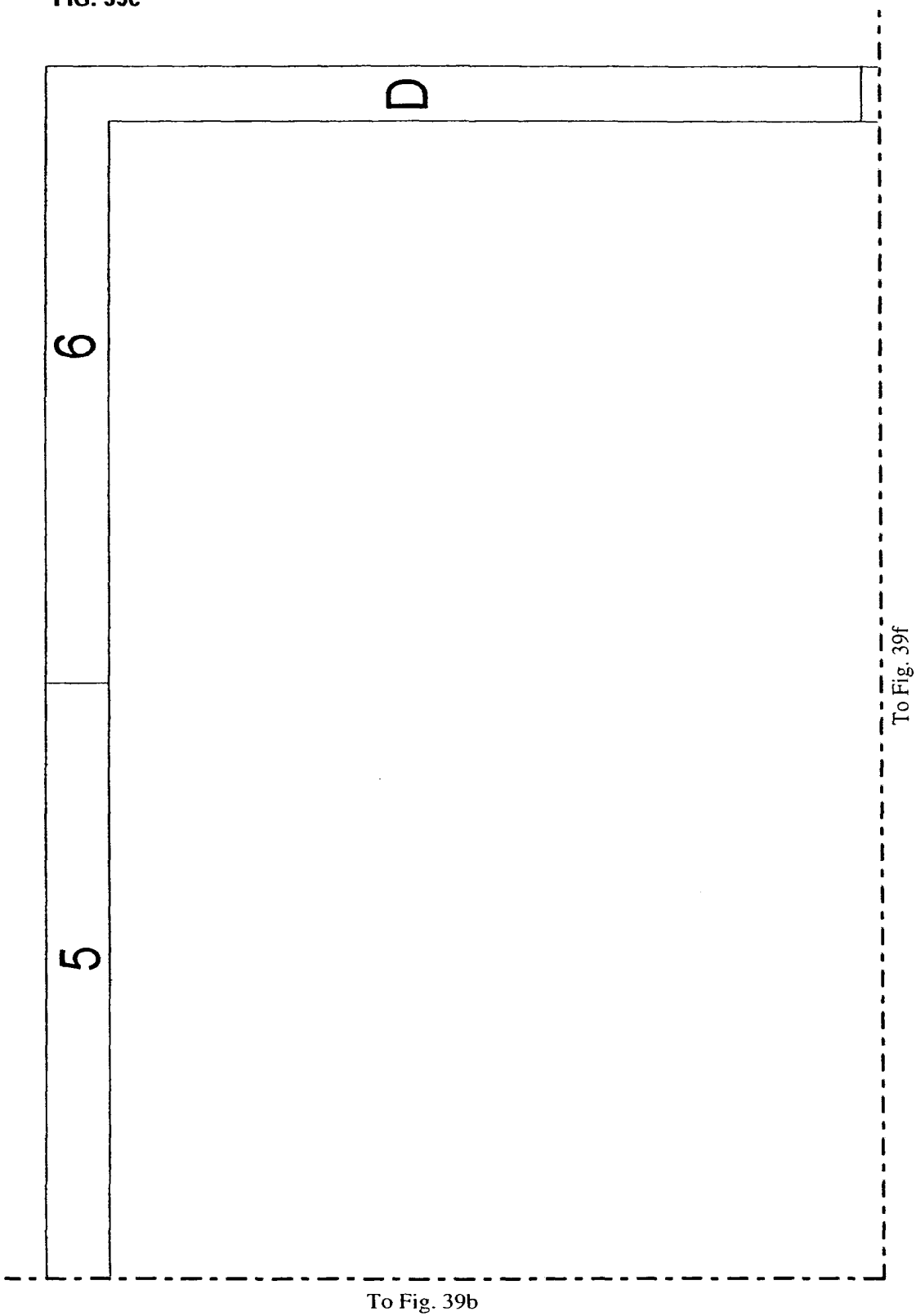


FIG. 39c



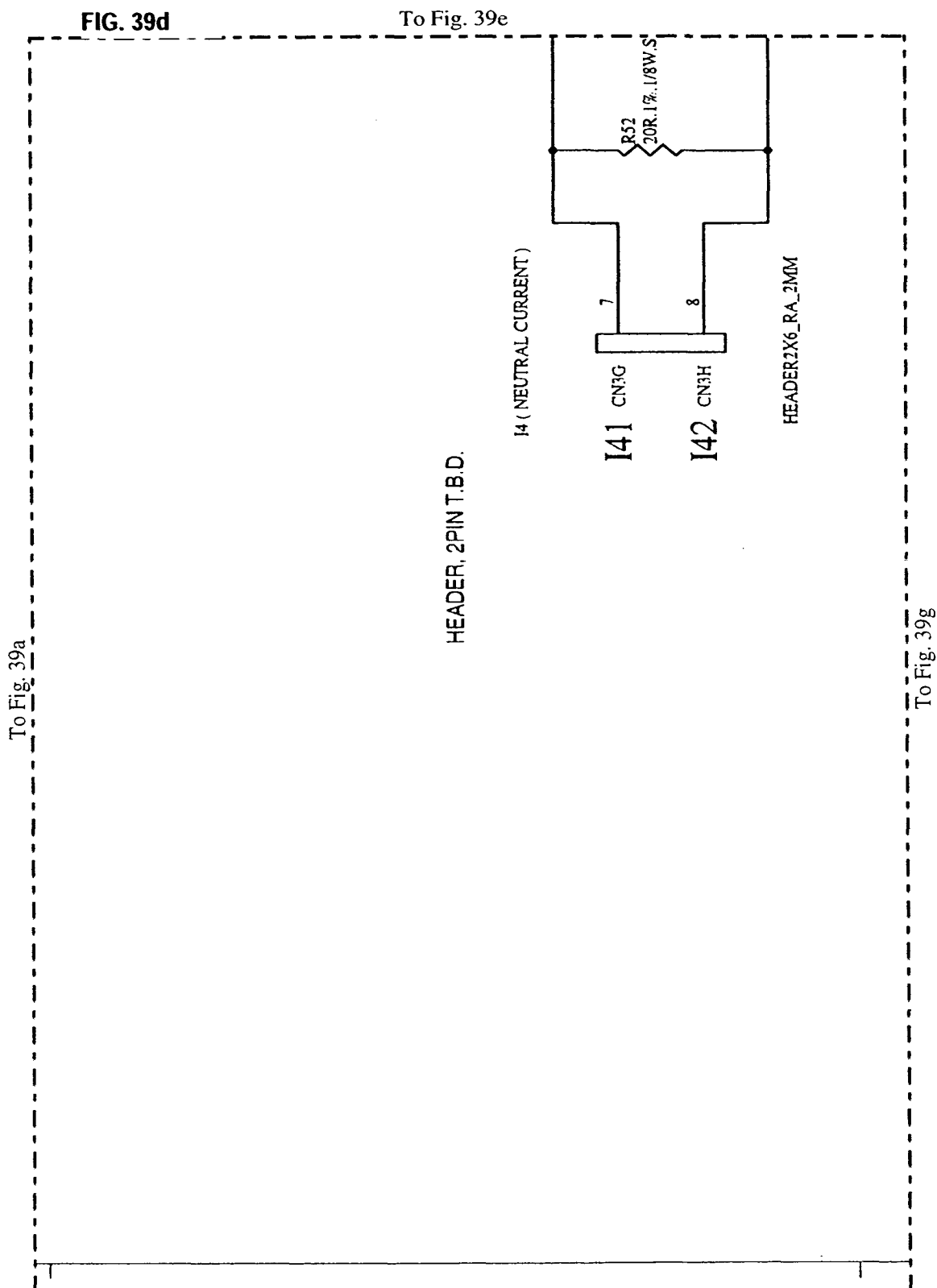


FIG. 39e

To Fig. 39f

AUXILIARY CURRENT INPUTS (0-50A)

To Fig. 39b

To Fig. 39d

To Fig. 39h

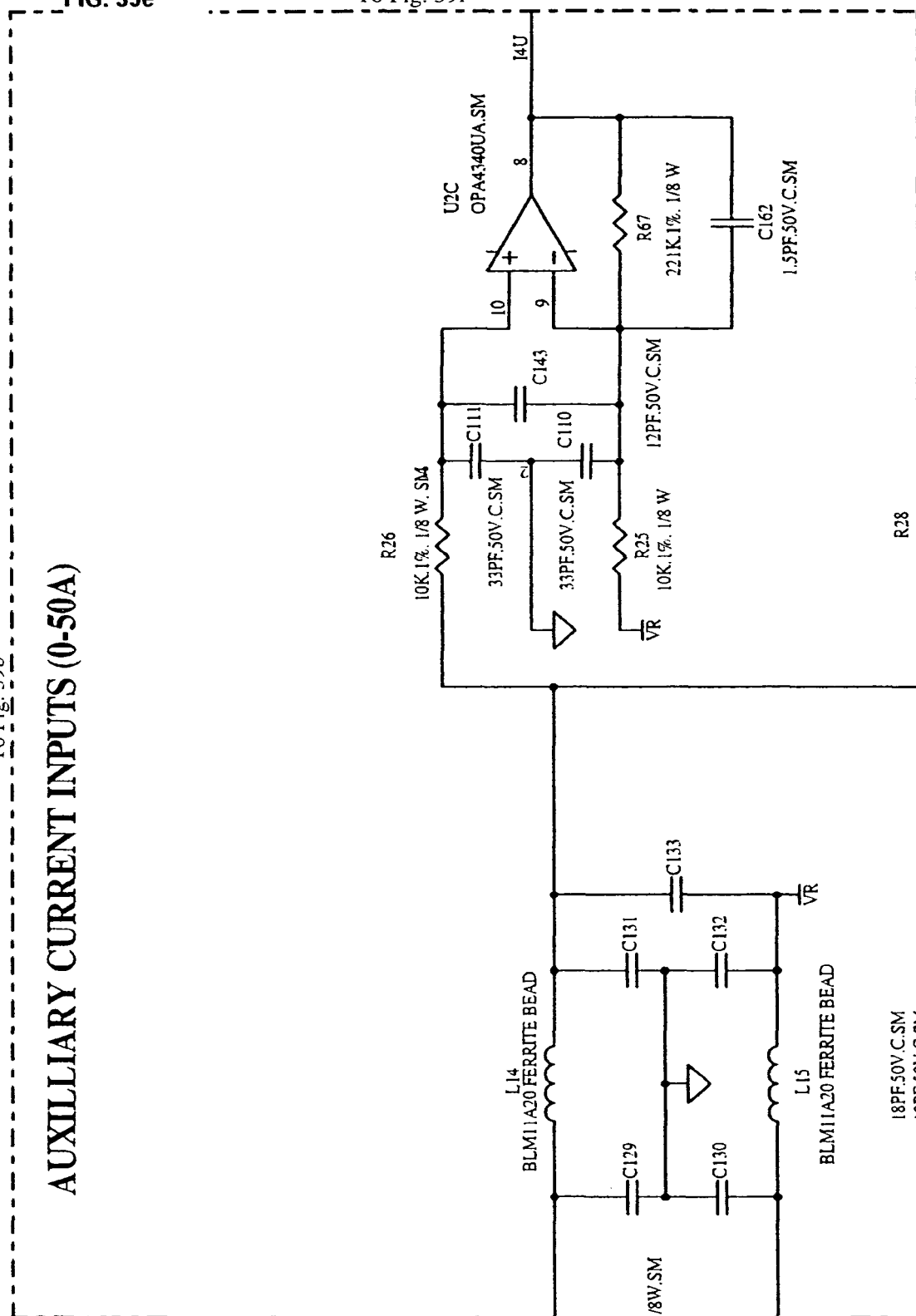


FIG. 39f

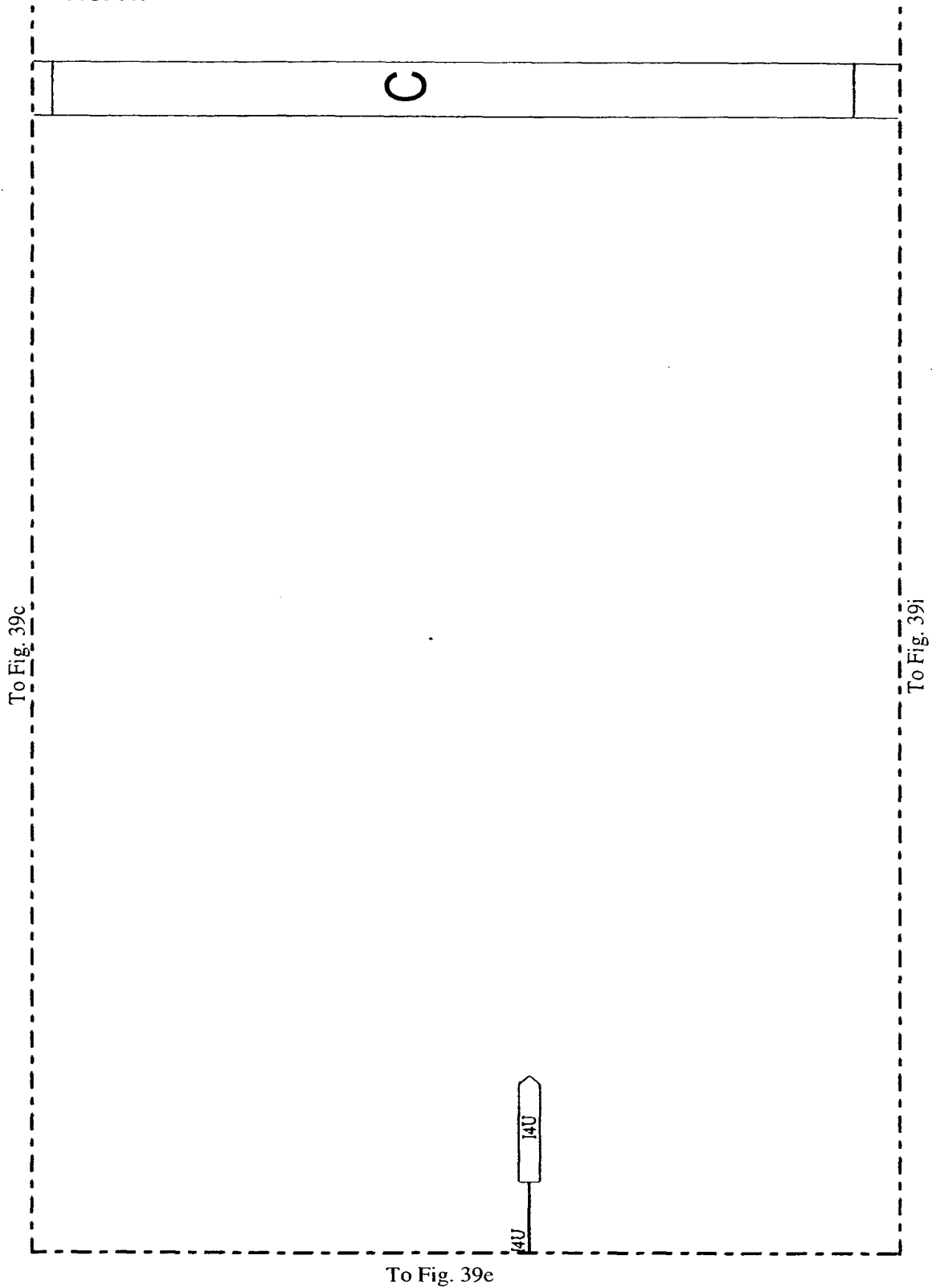


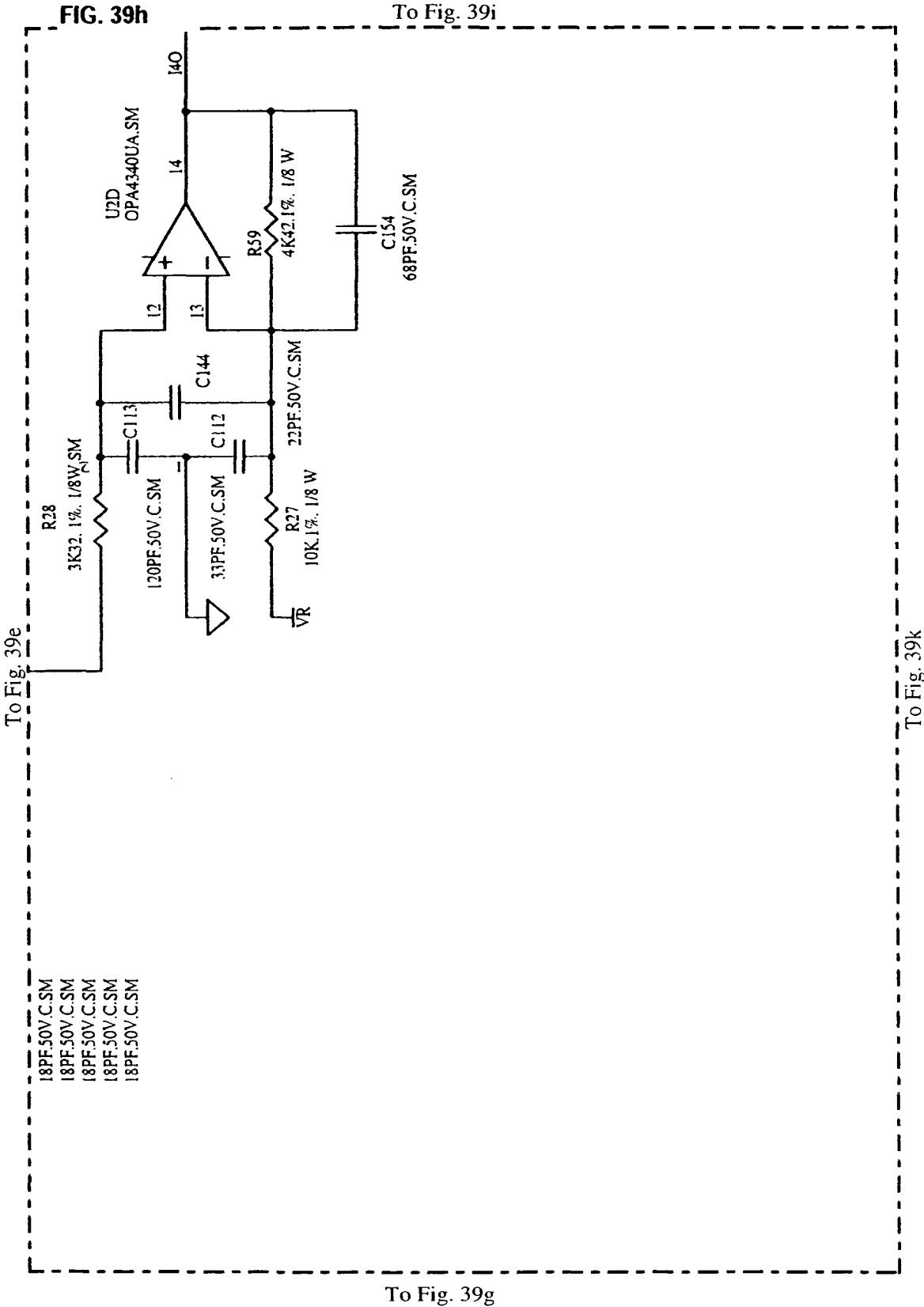
FIG. 39g

To Fig. 39h

To Fig. 39d

To Fig. 39j

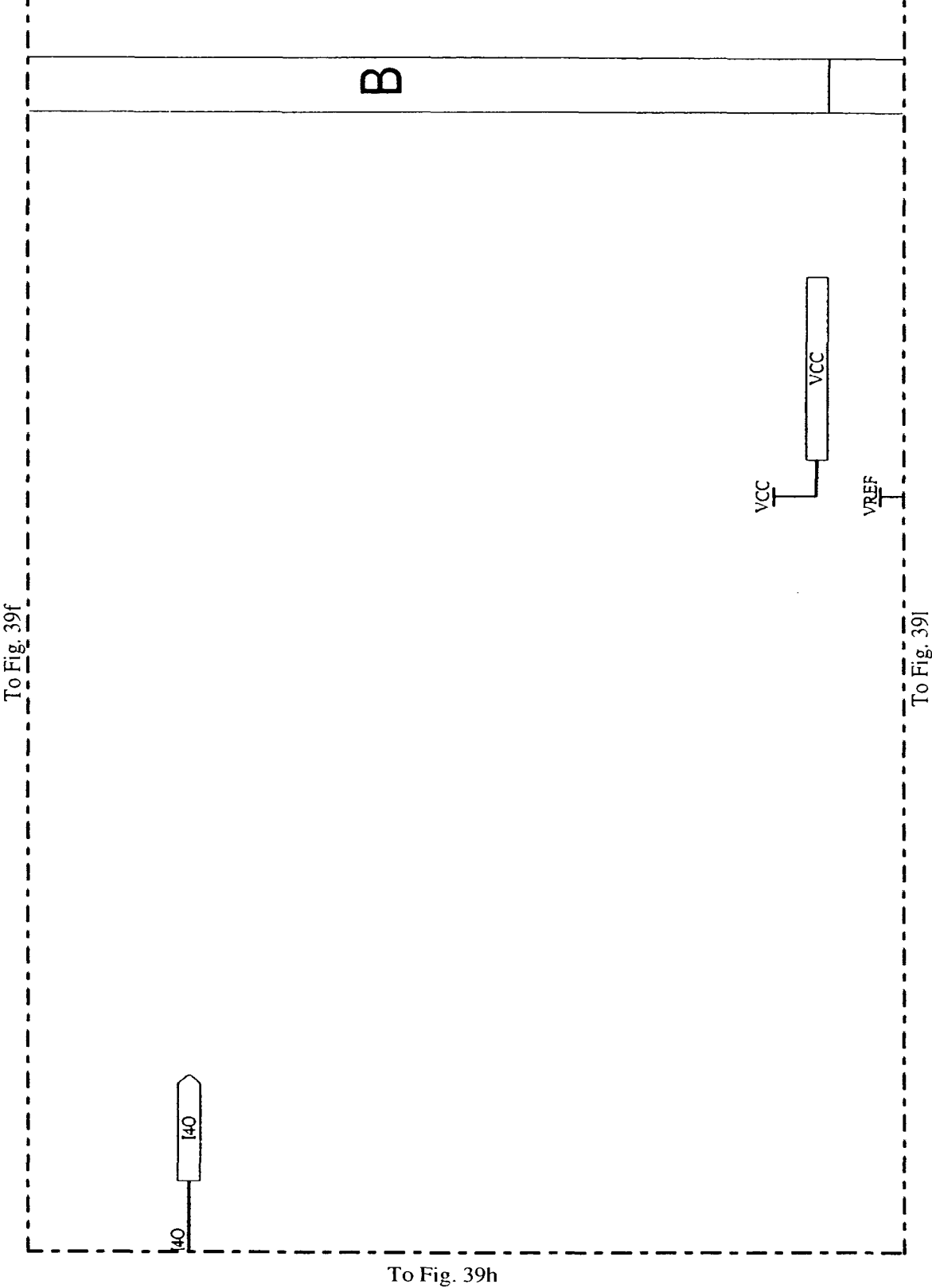
FIG. 39h

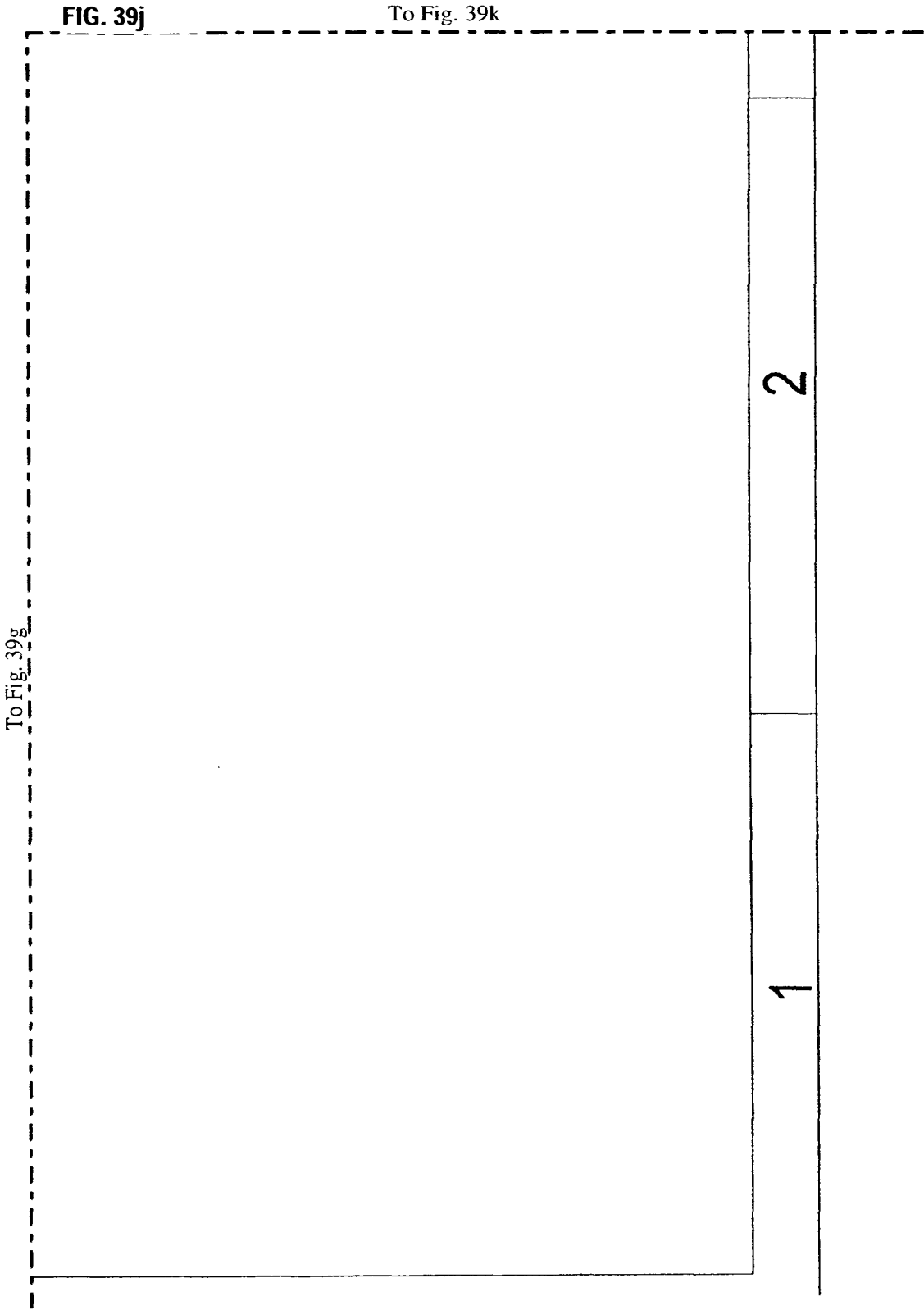


18PF, 50V, C.S.M.
18PF, 50V, C.S.M.
18PF, 50V, C.S.M.
18PF, 50V, C.S.M.
18PF, 50V, C.S.M.

To Fig. 39g

FIG. 39i





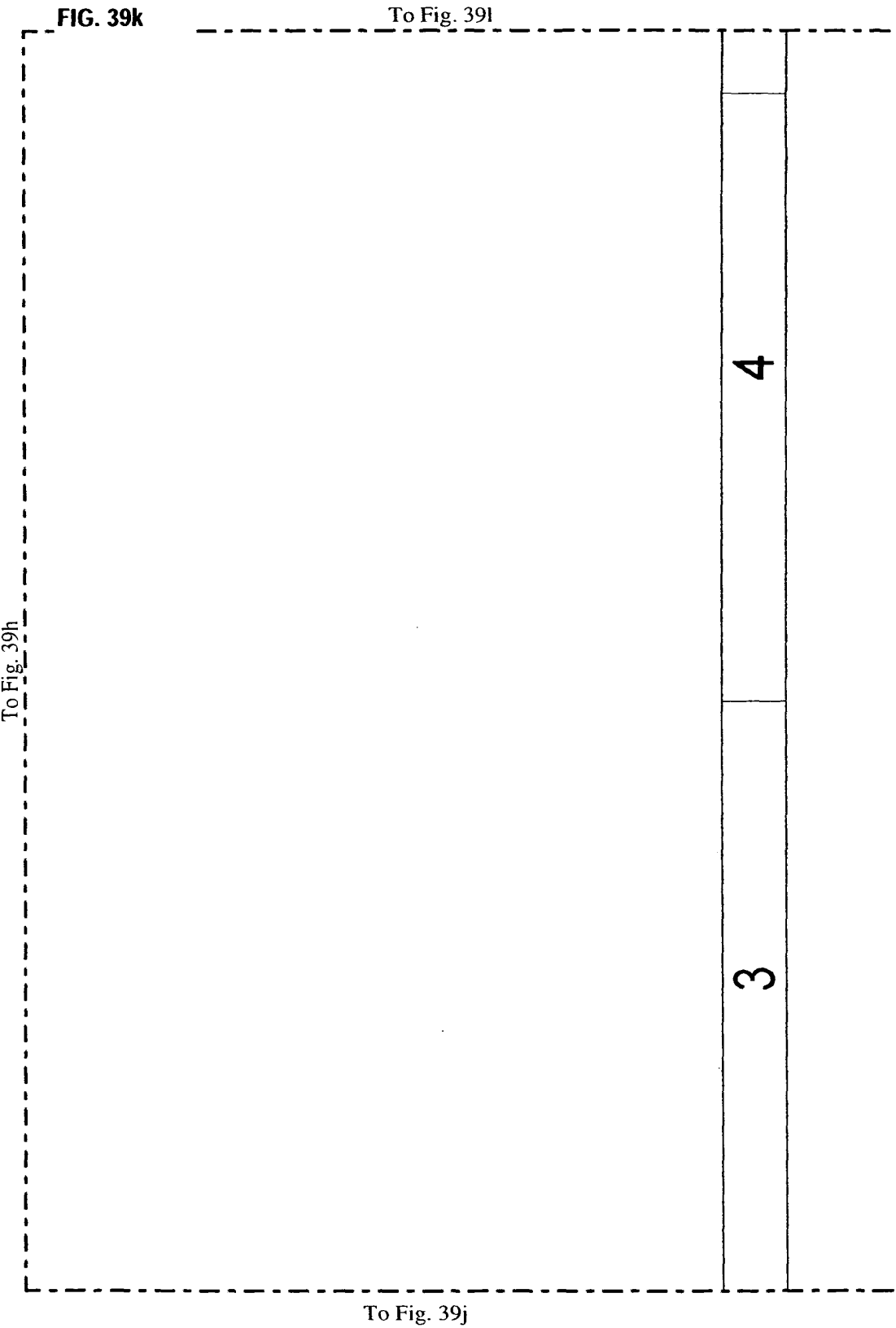


FIG. 39l

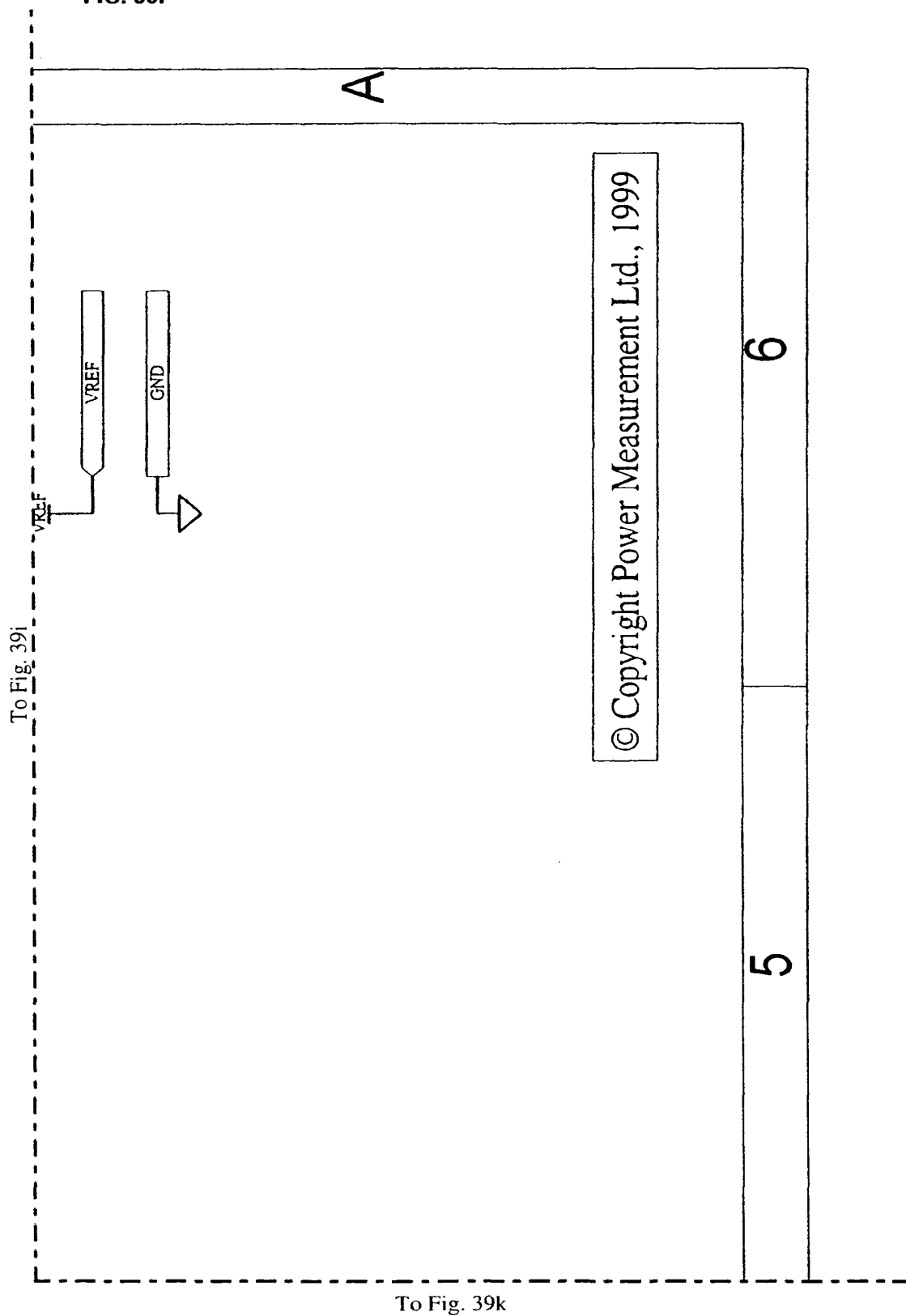
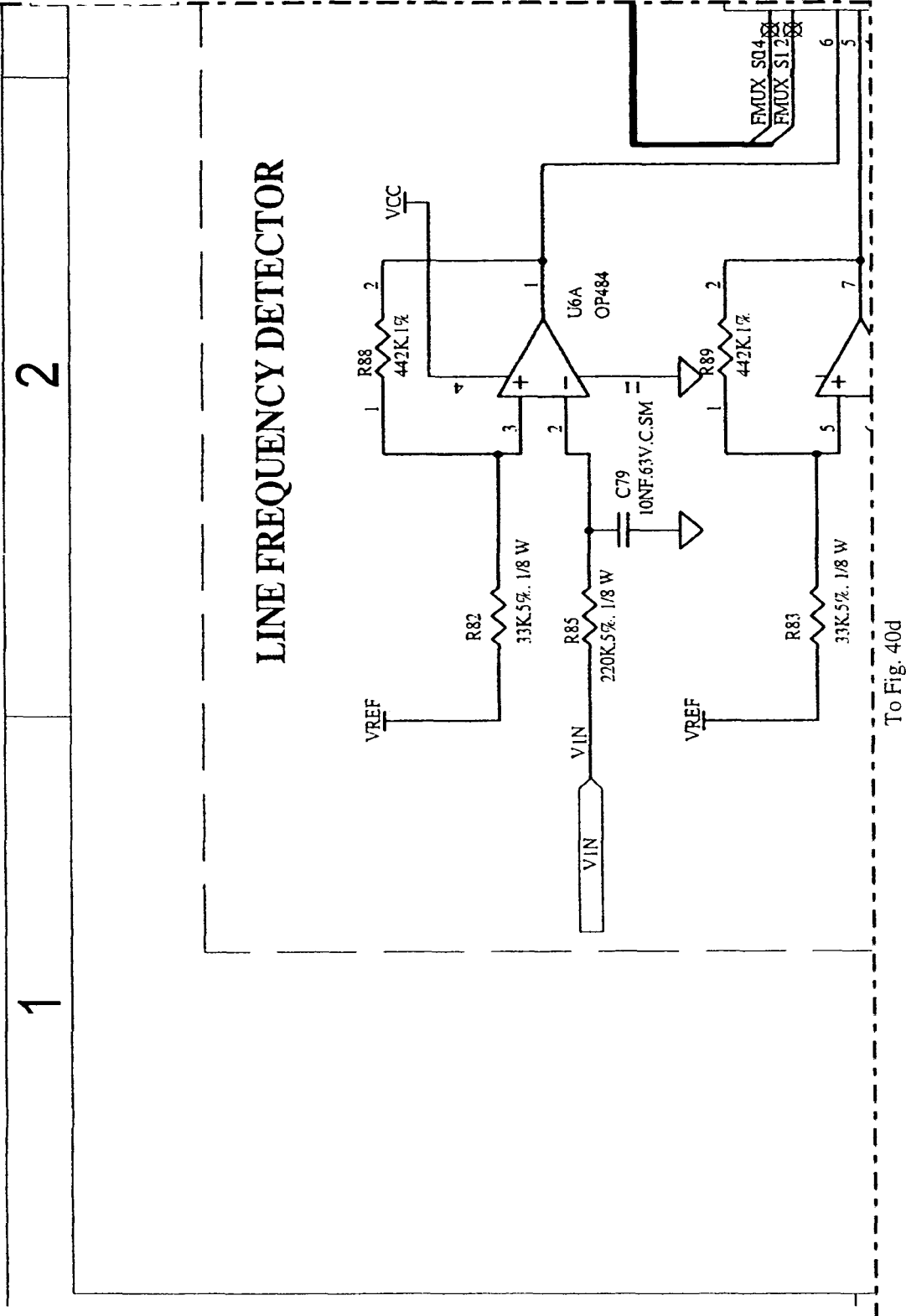


FIG. 40a

To Fig. 40b



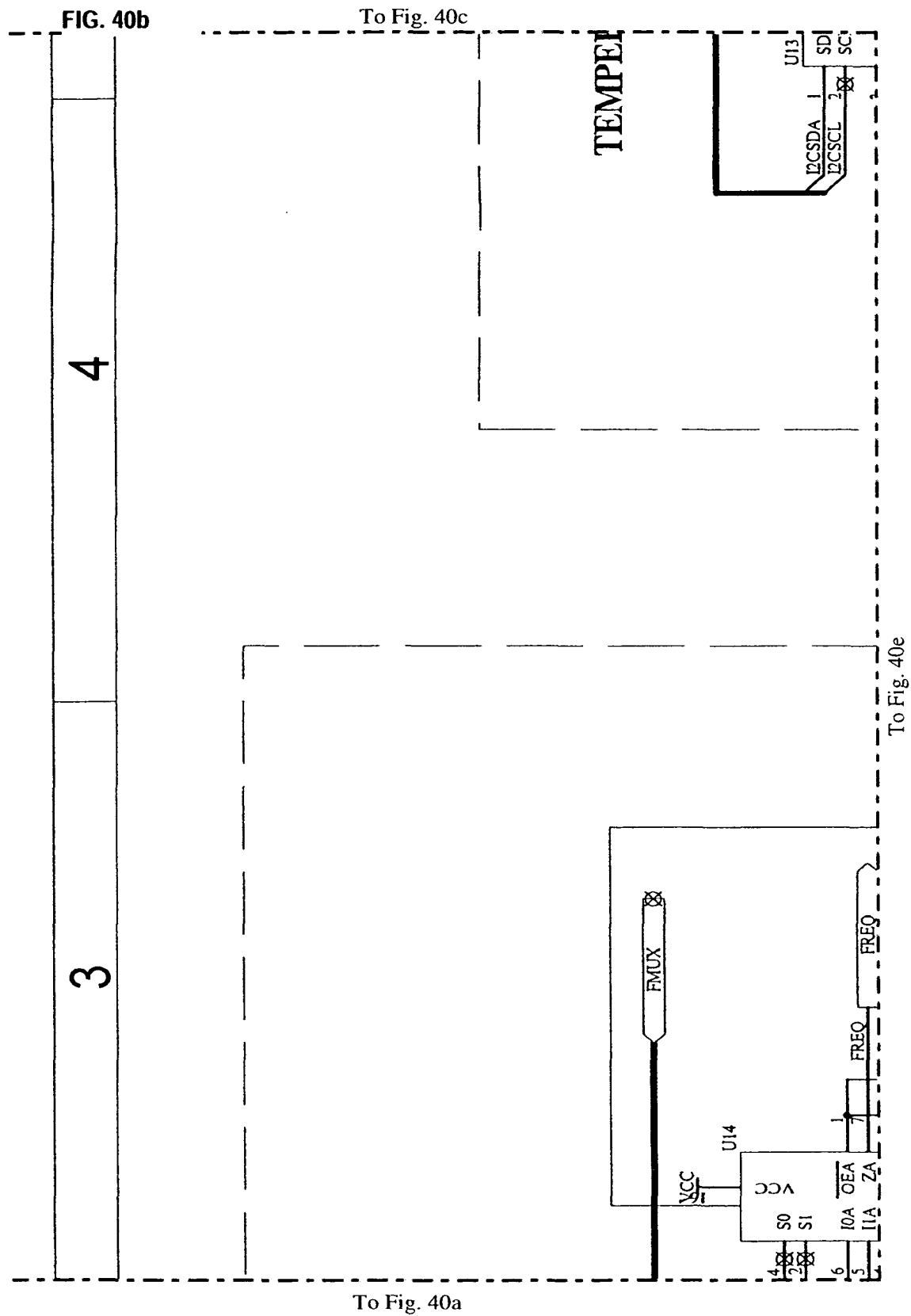
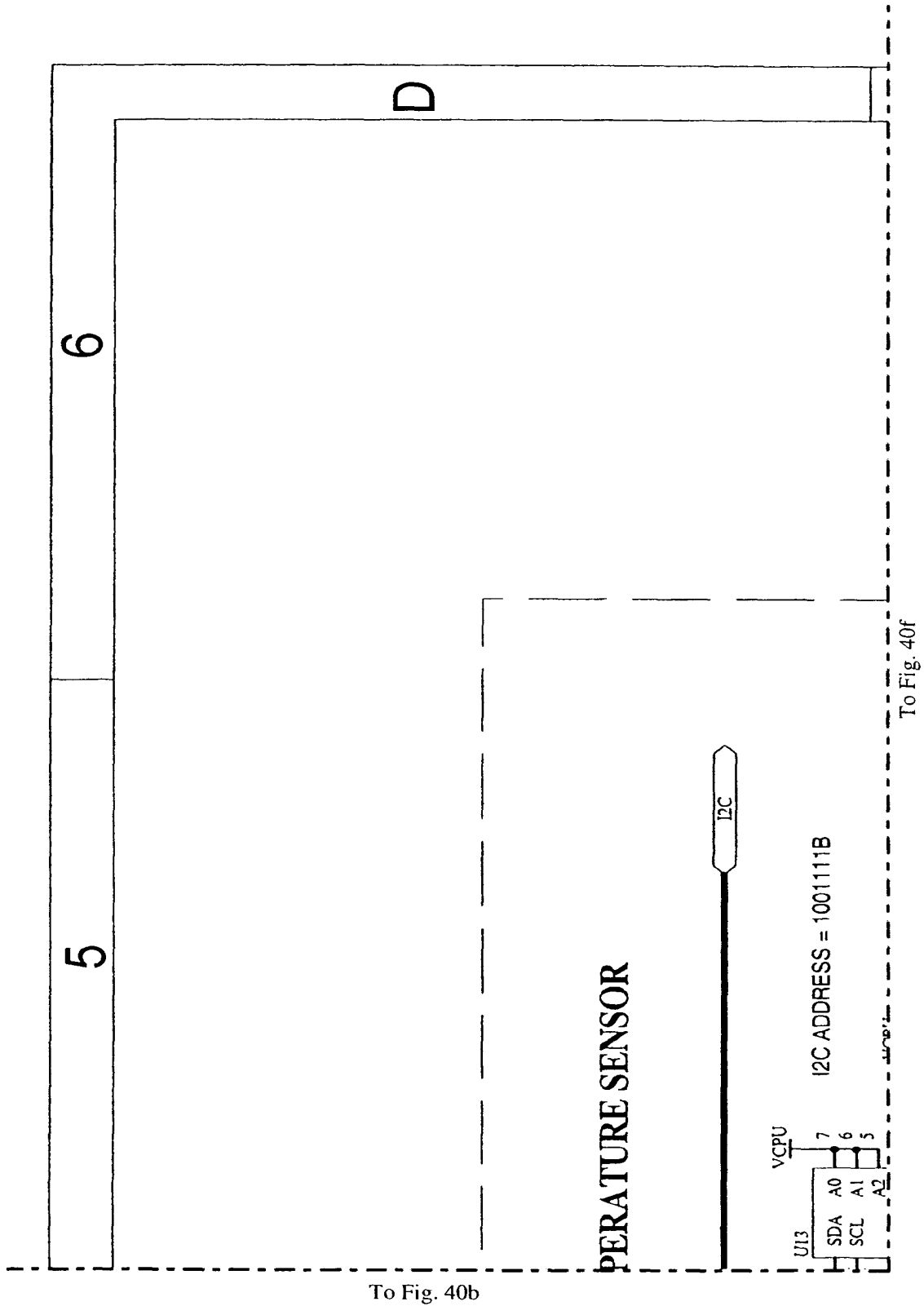
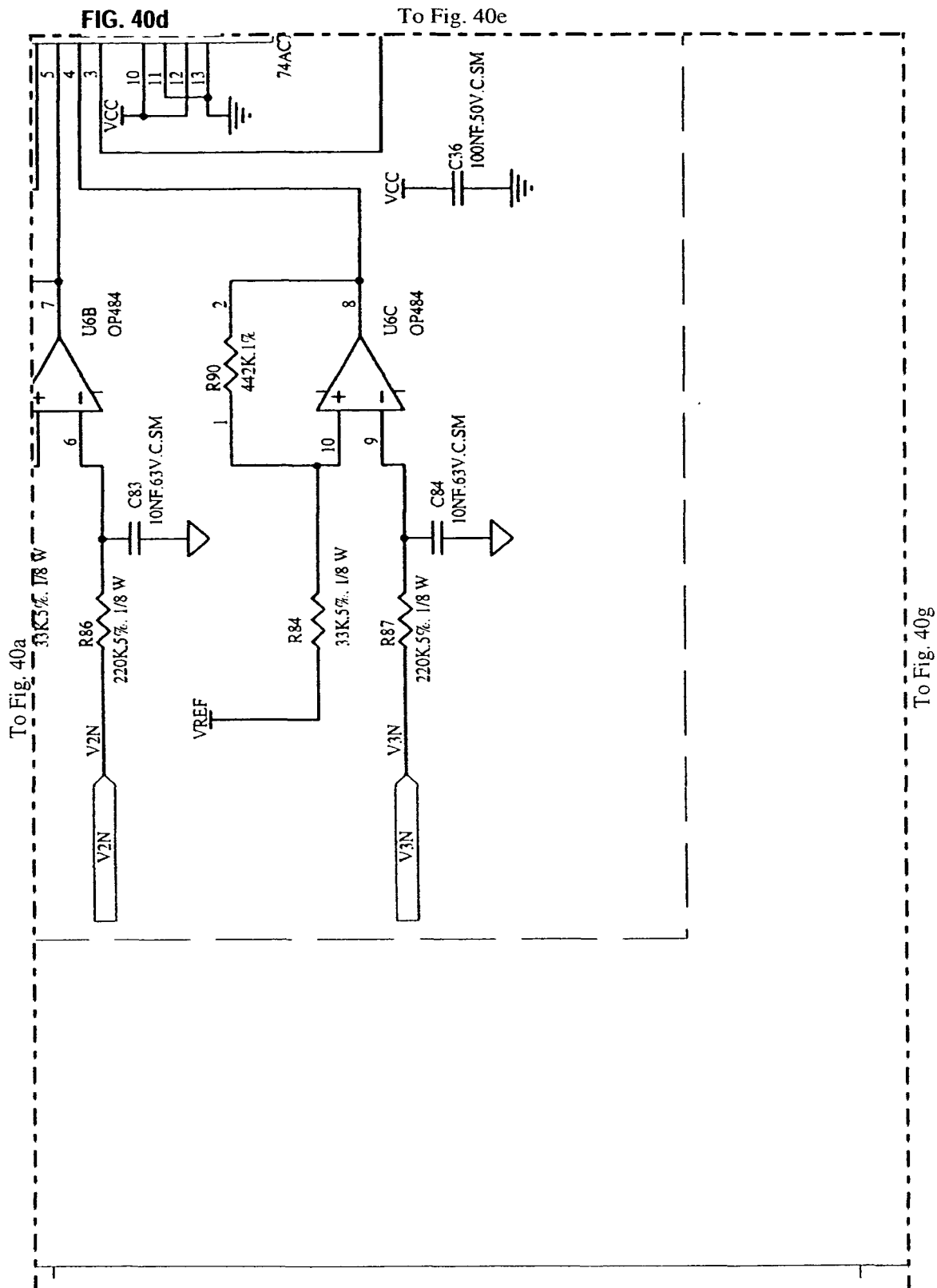
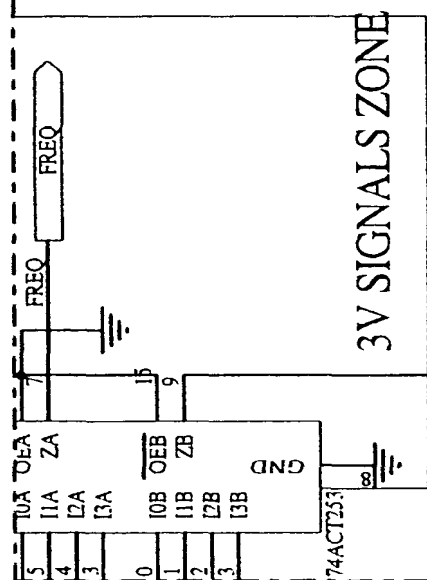


FIG. 40c





To Fig. 40b



Note: 2nd multiplexer is used to encode board type.
1010b = 9S (ANSI C12)

MS.

To Fig. 40d

To Fig. 40h

FIG. 40f

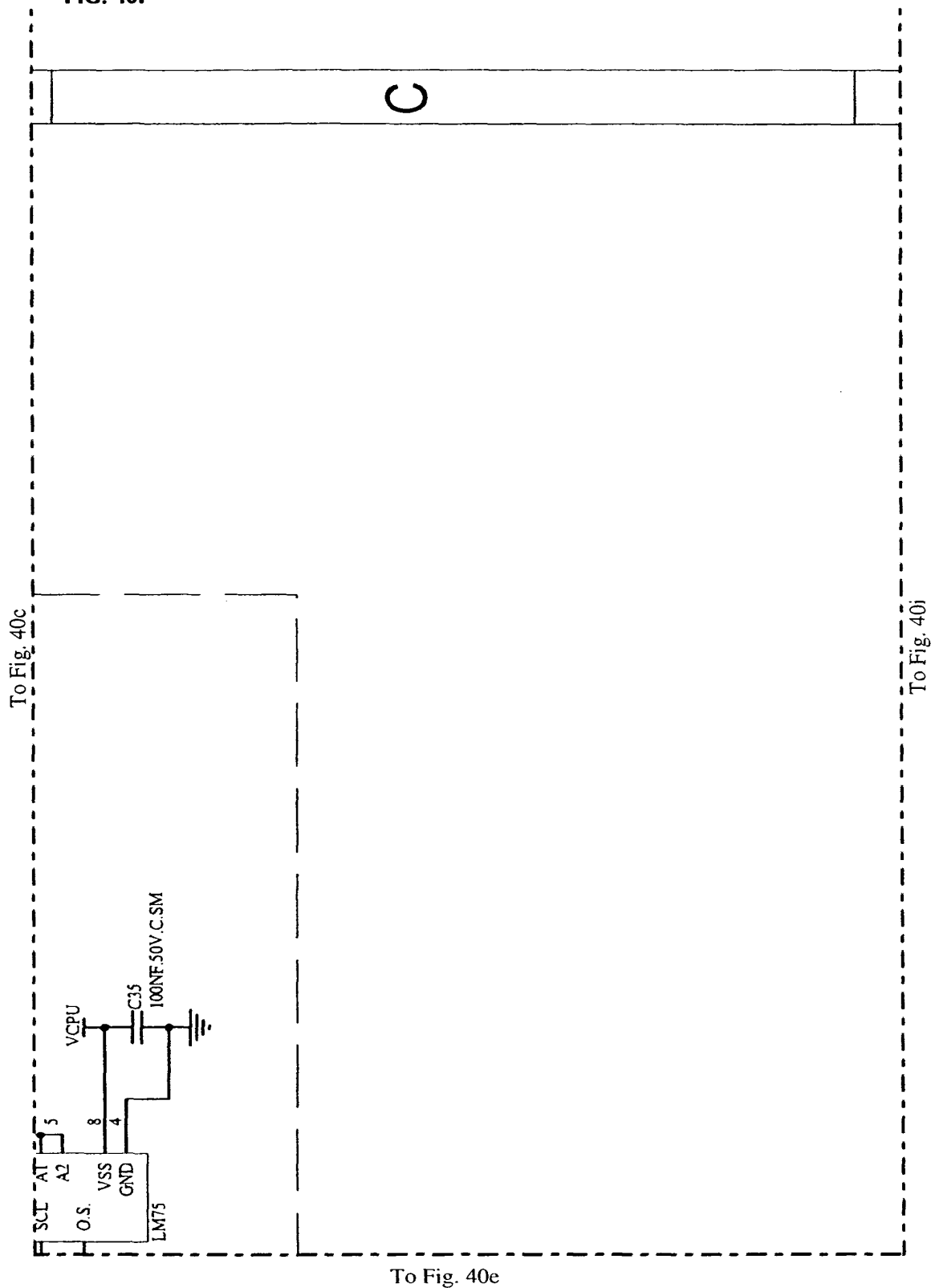
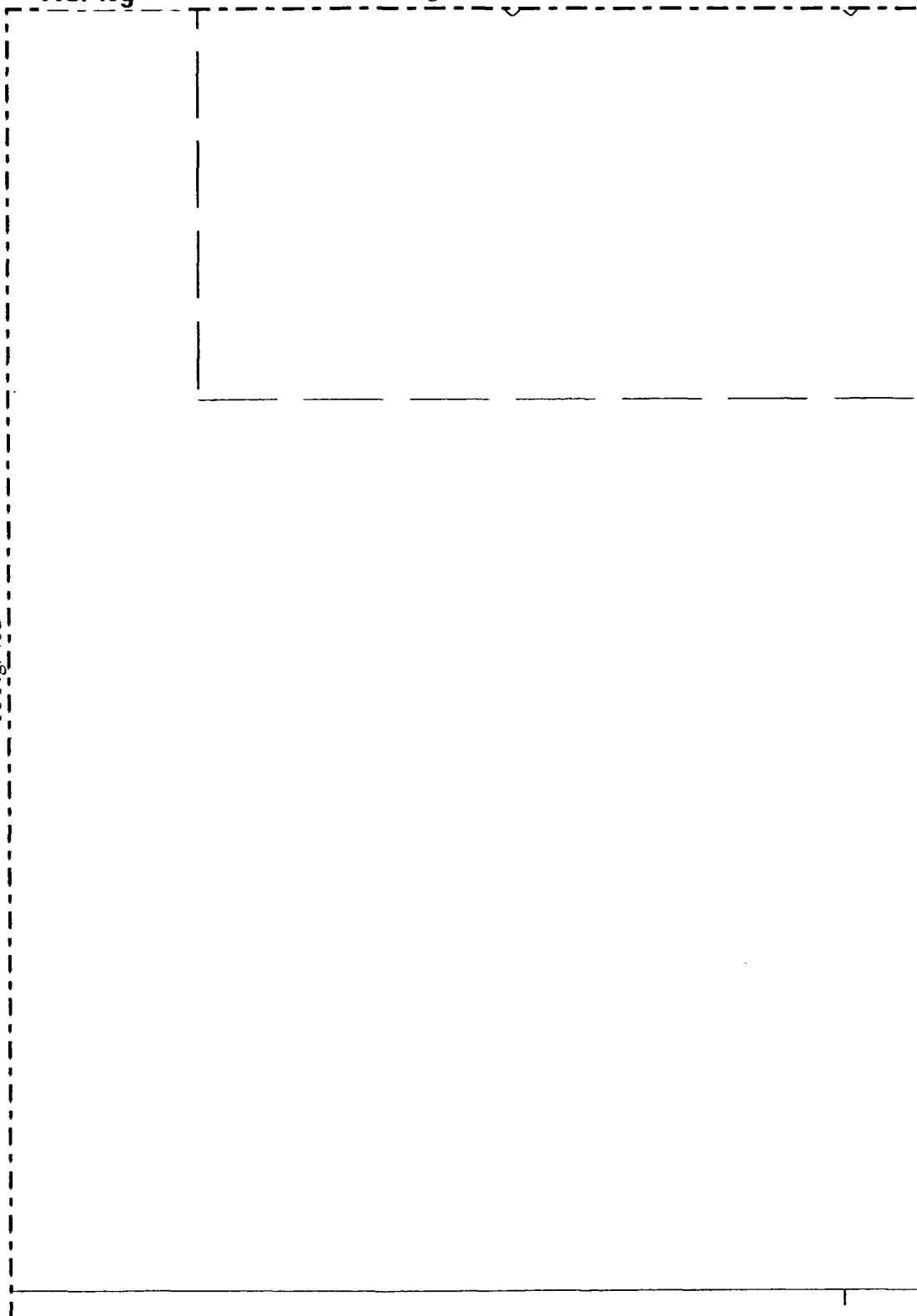


FIG. 40g

To Fig. 40h

To Fig. 40d

To Fig. 40j



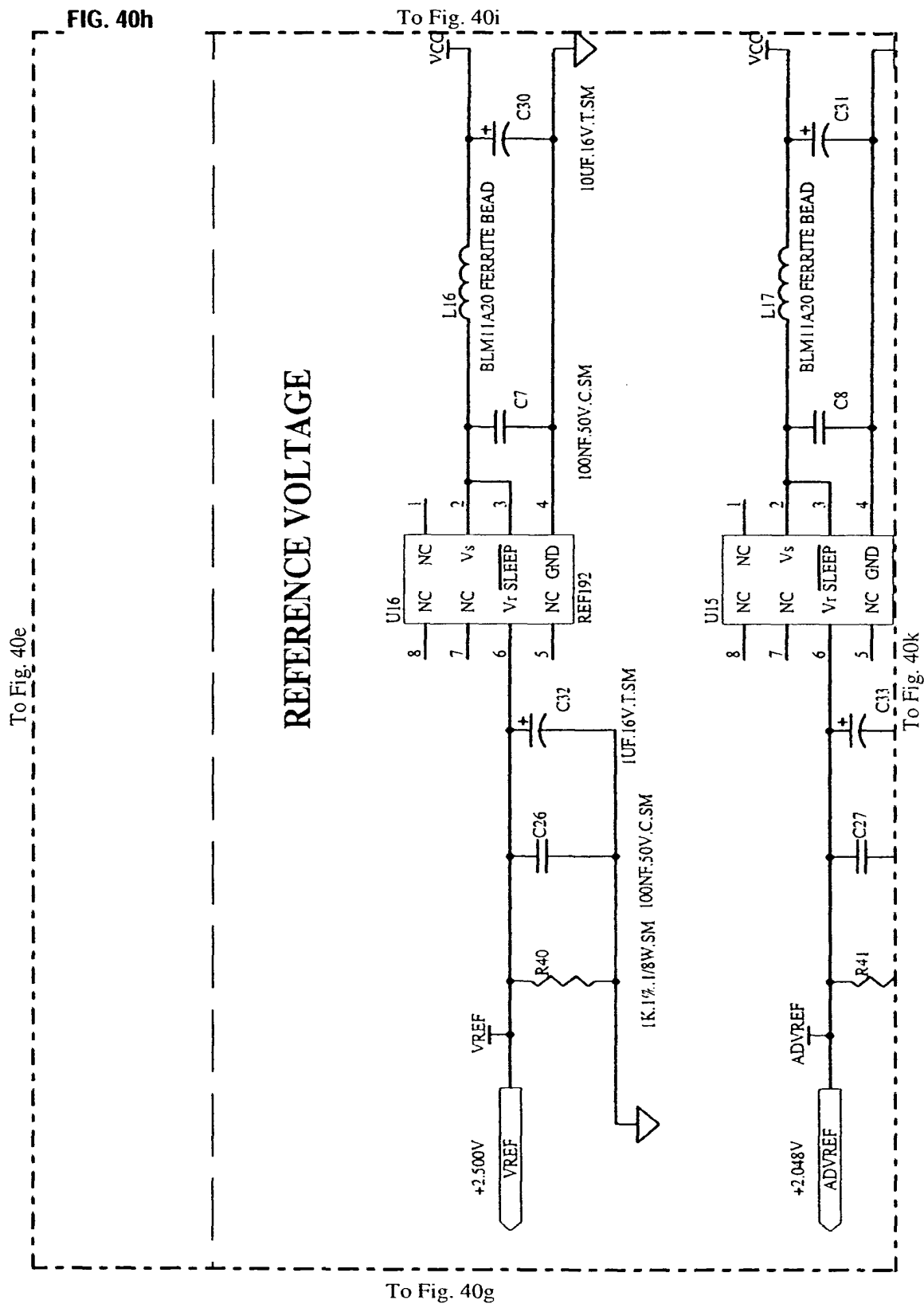
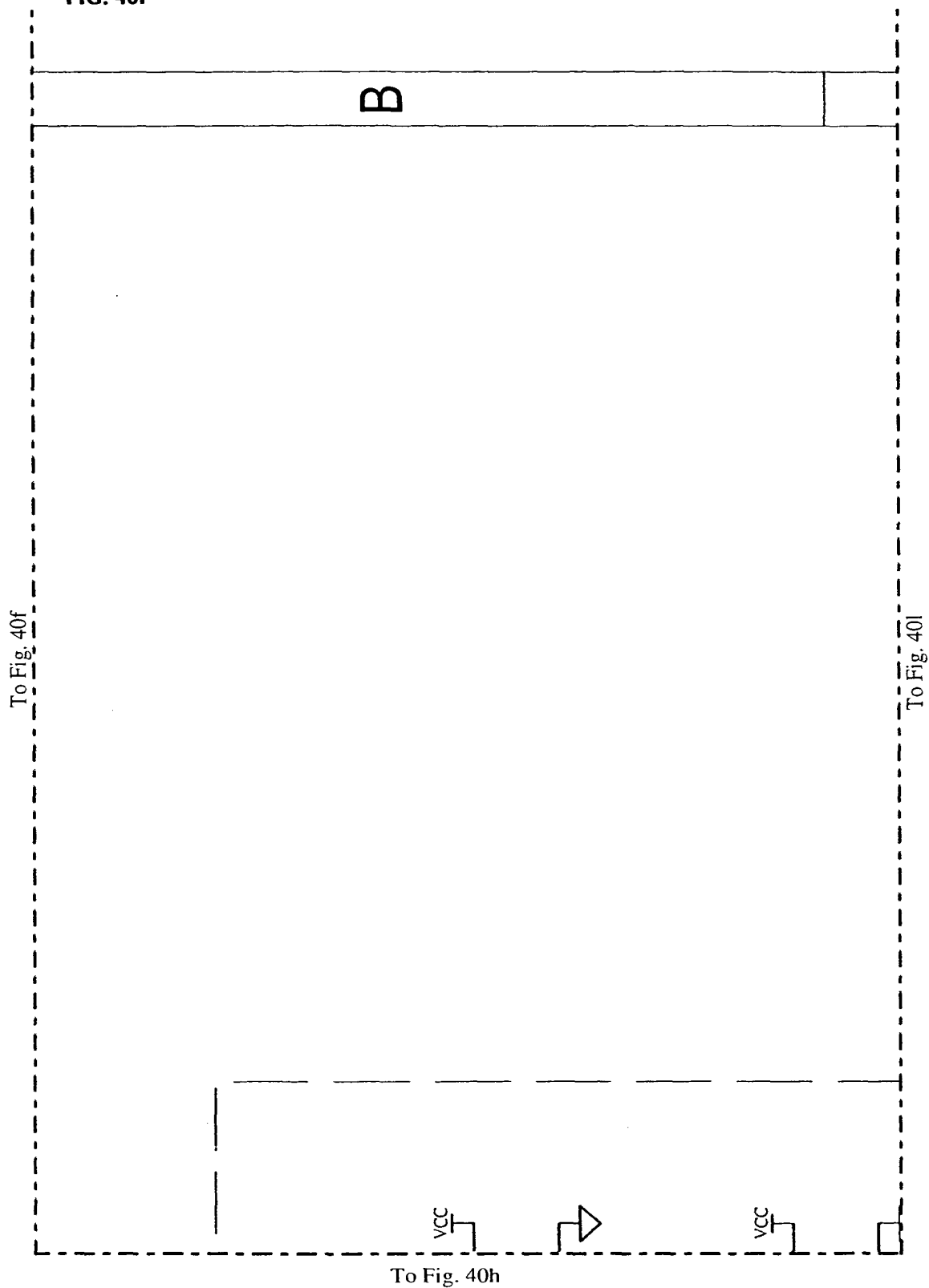
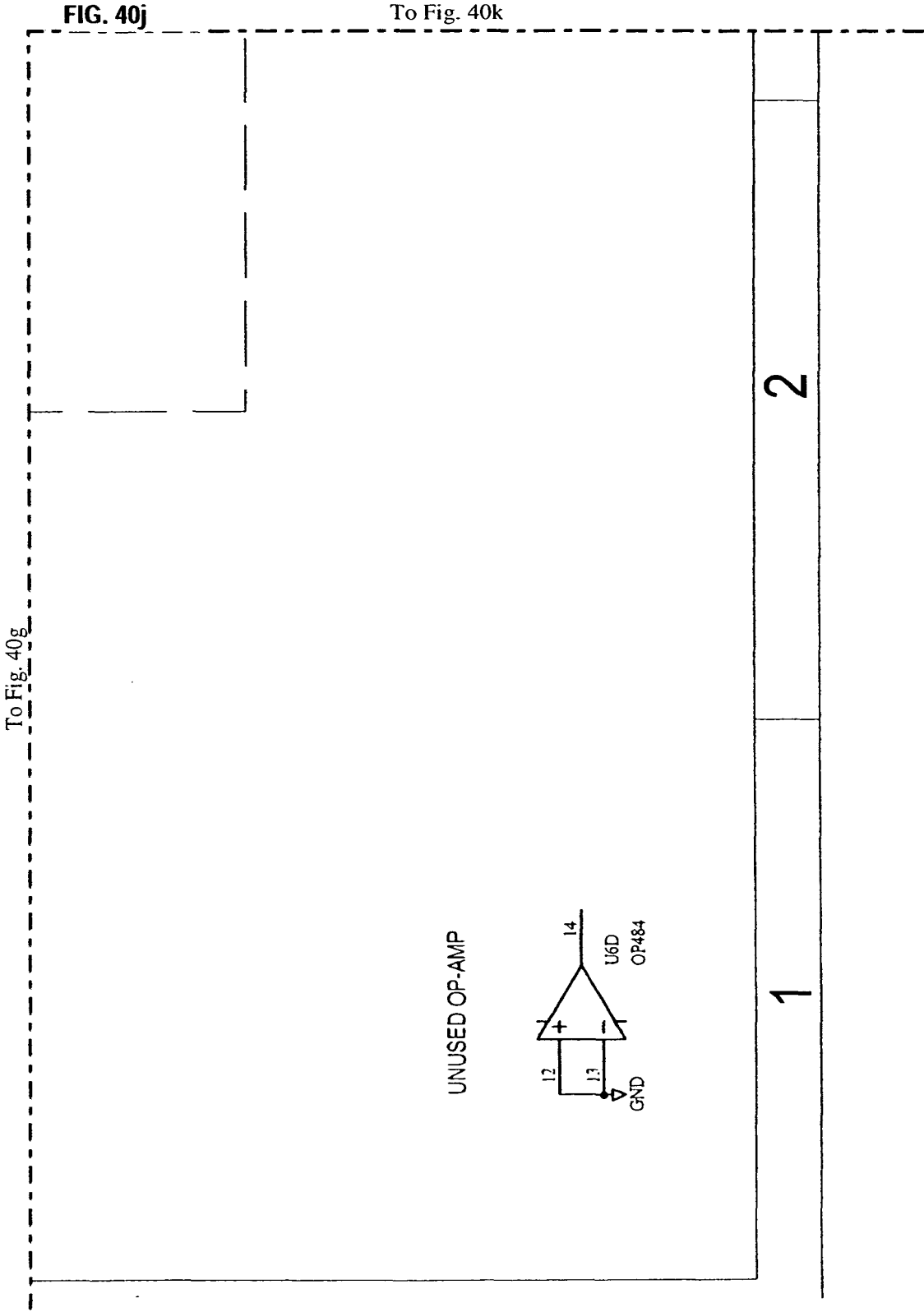


FIG. 40i





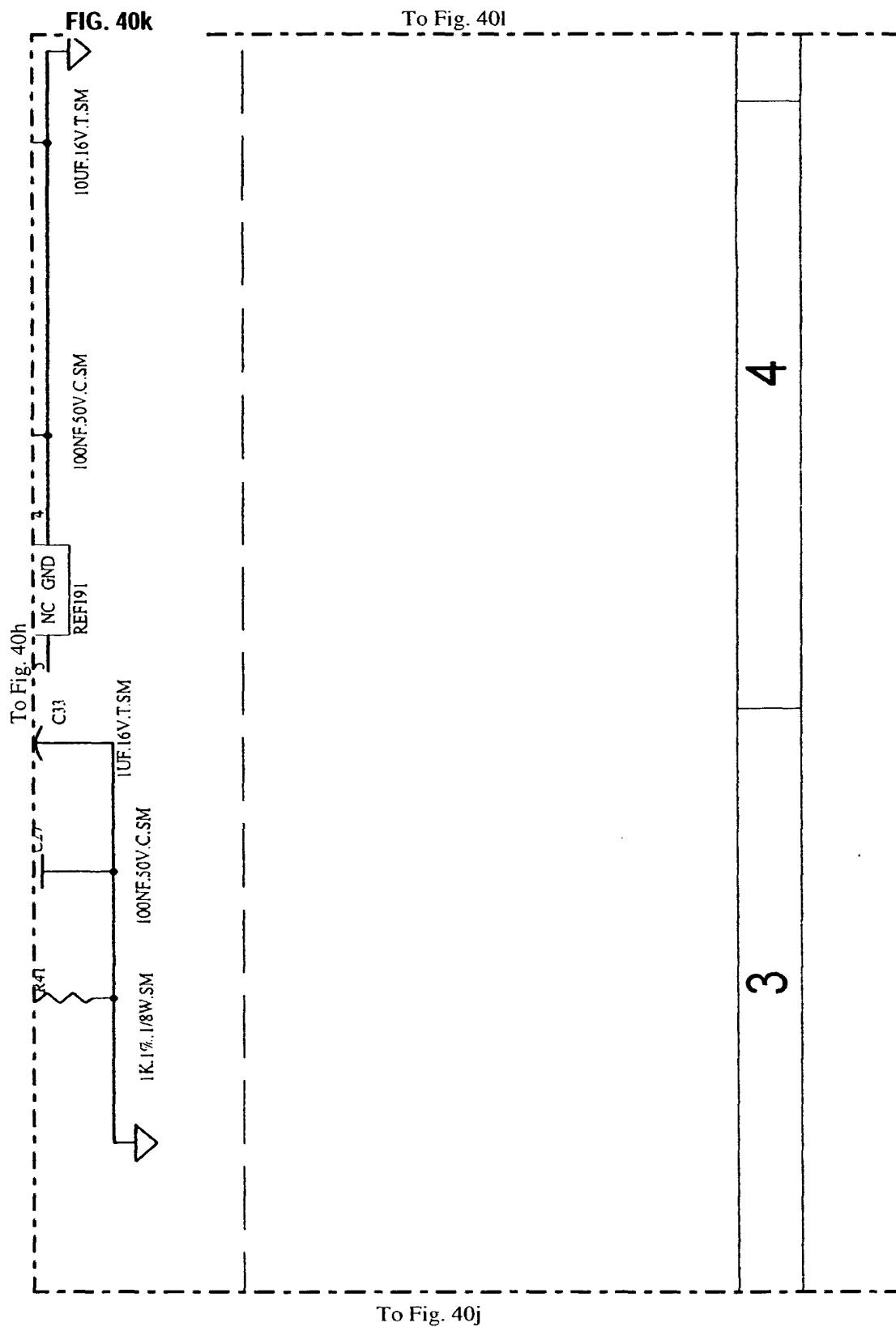
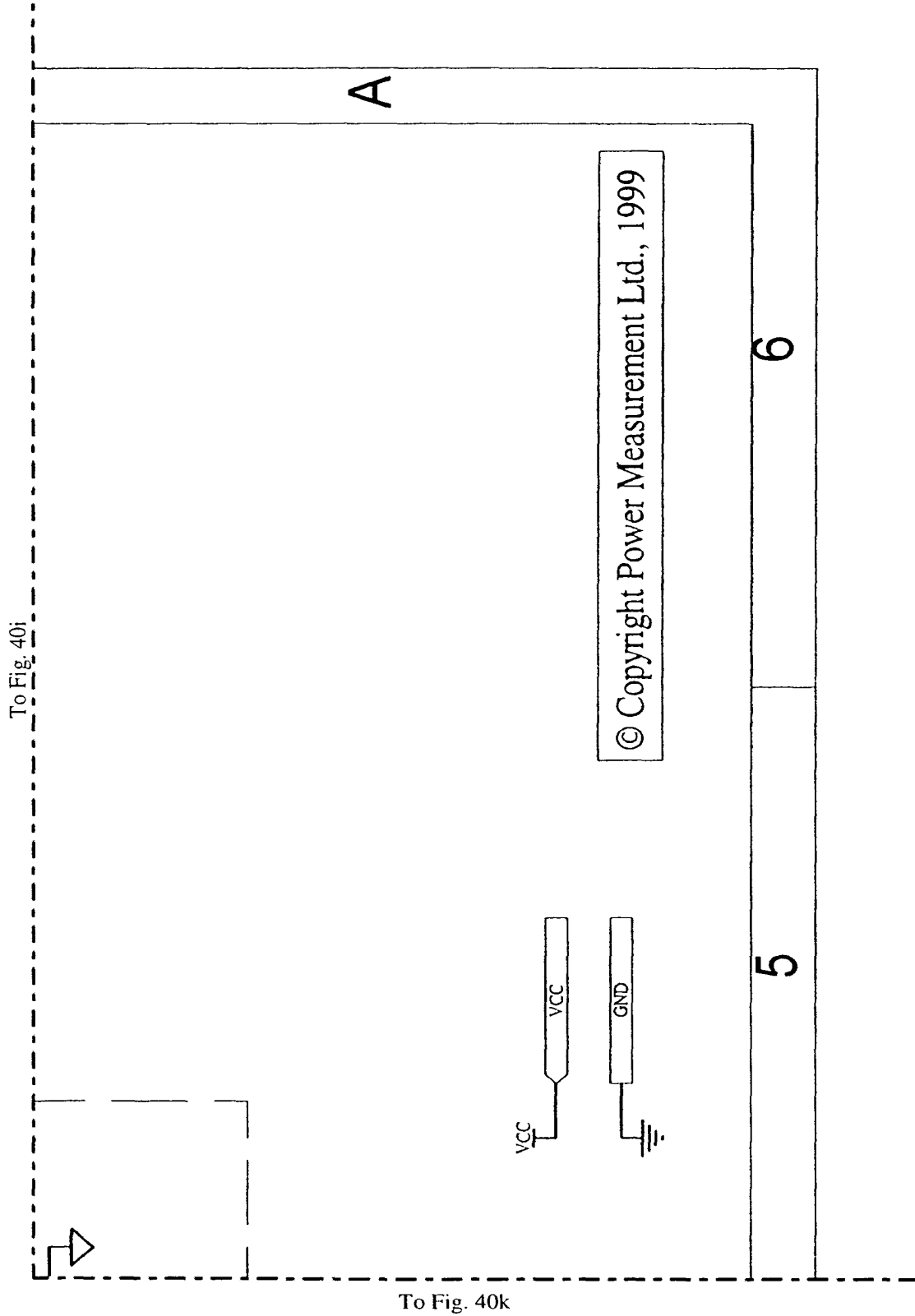
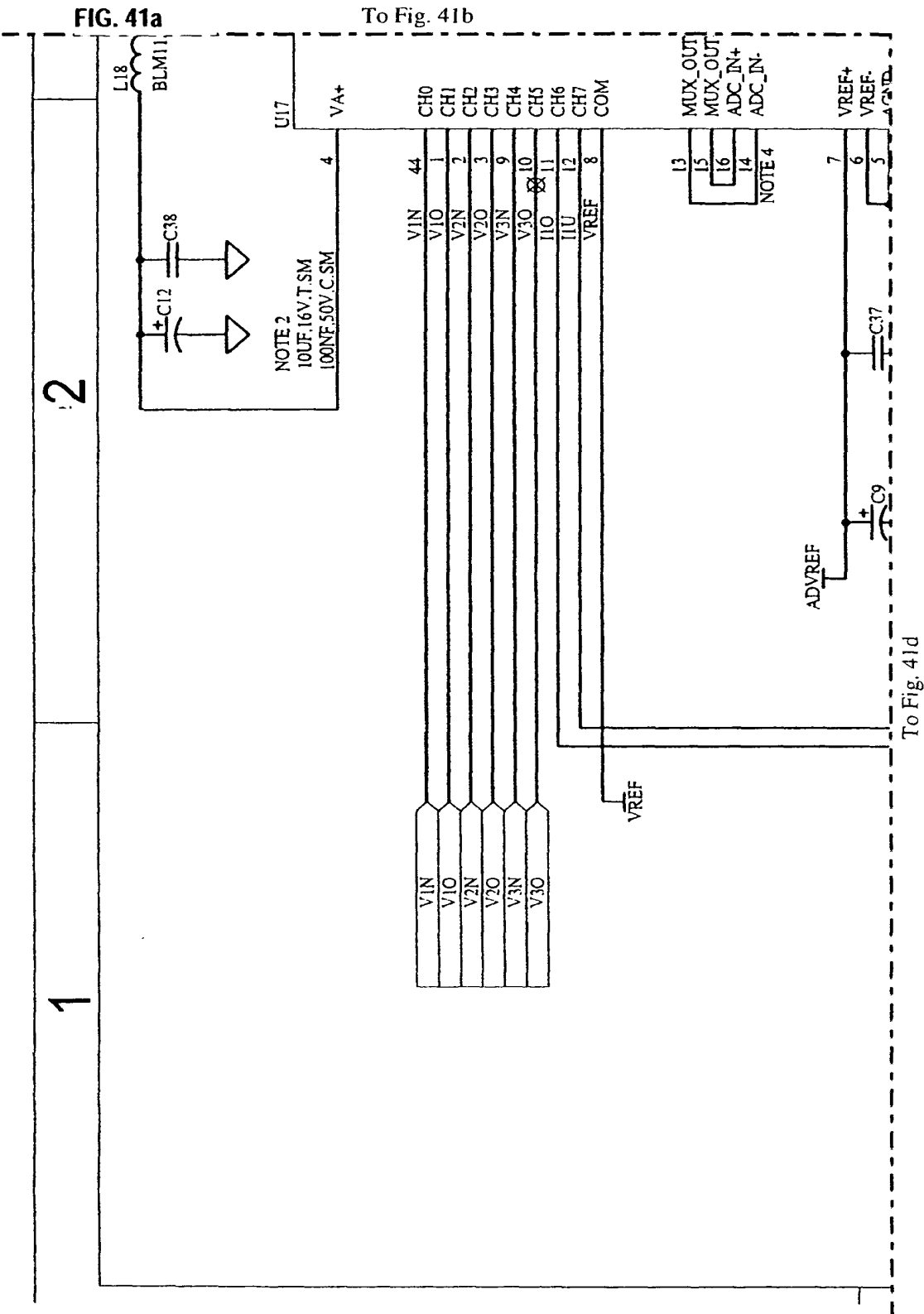


FIG. 40i





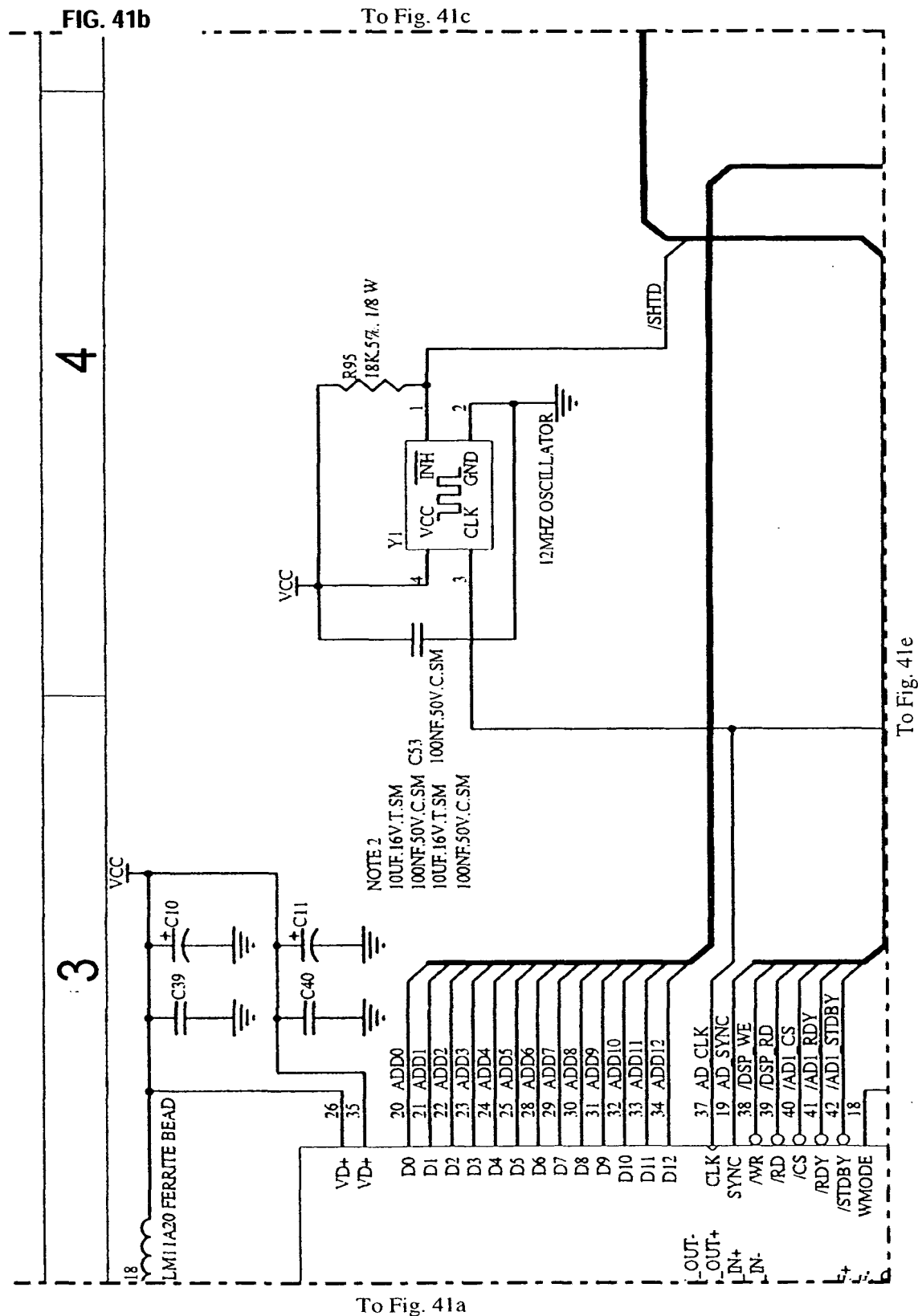
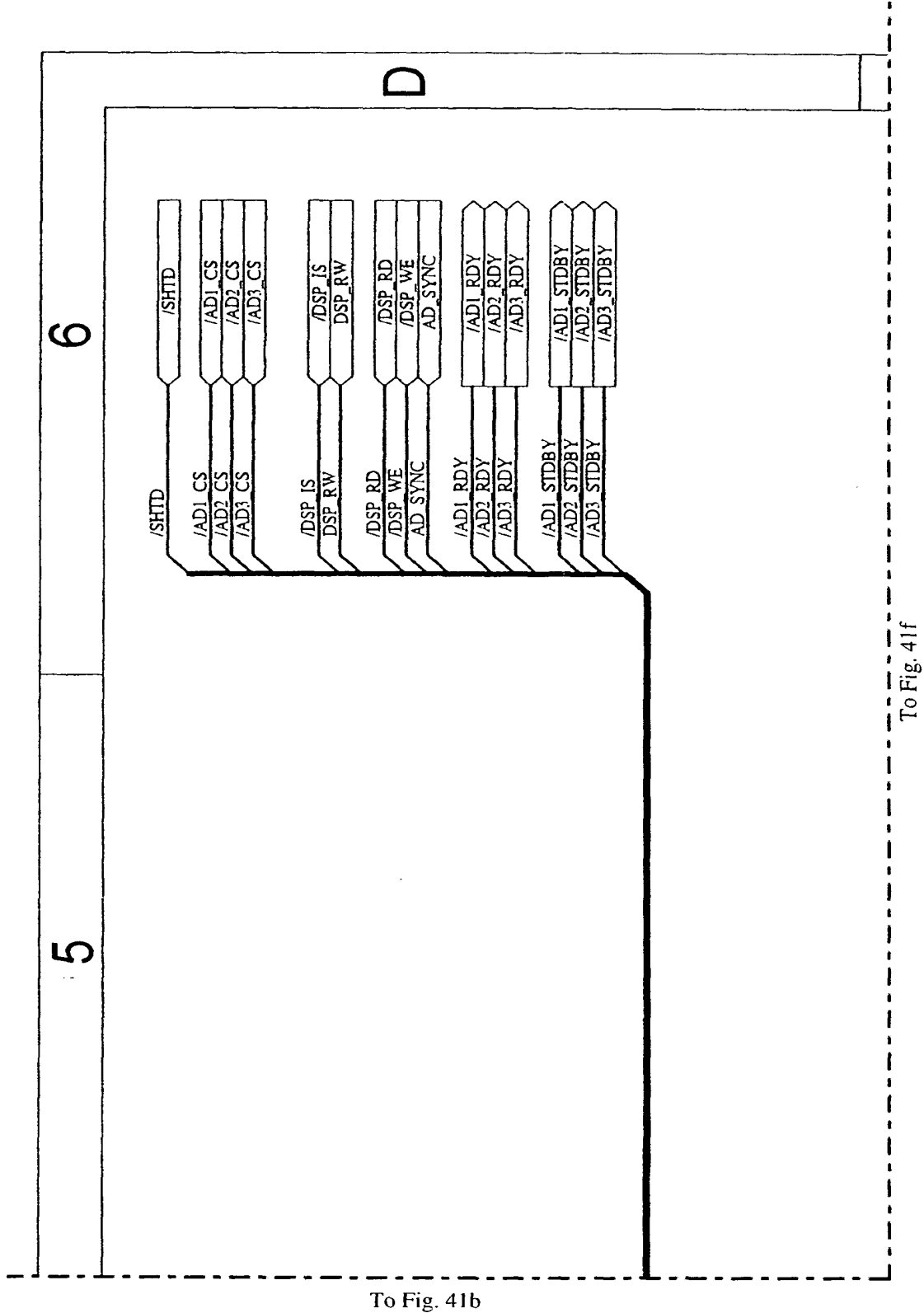
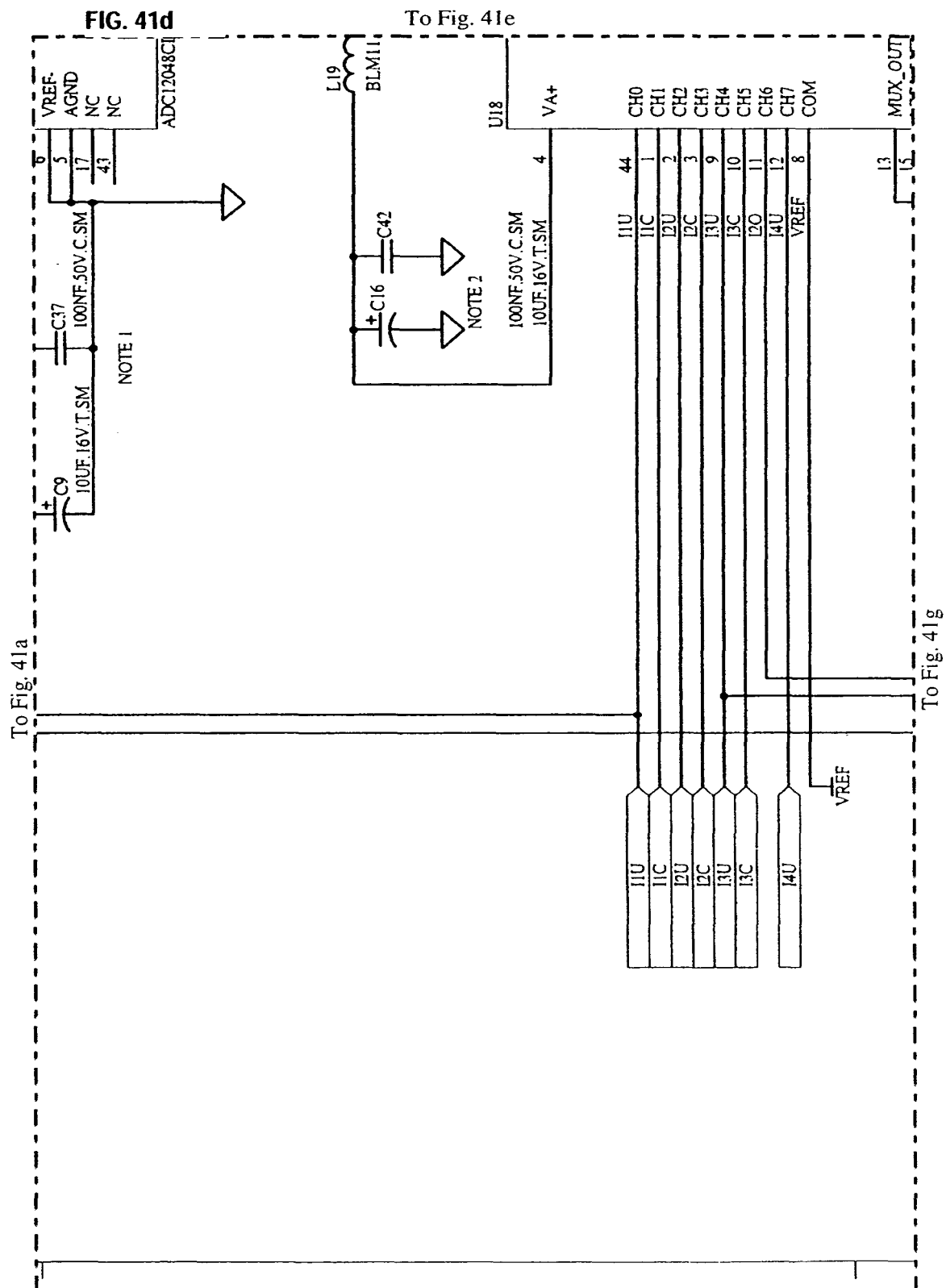


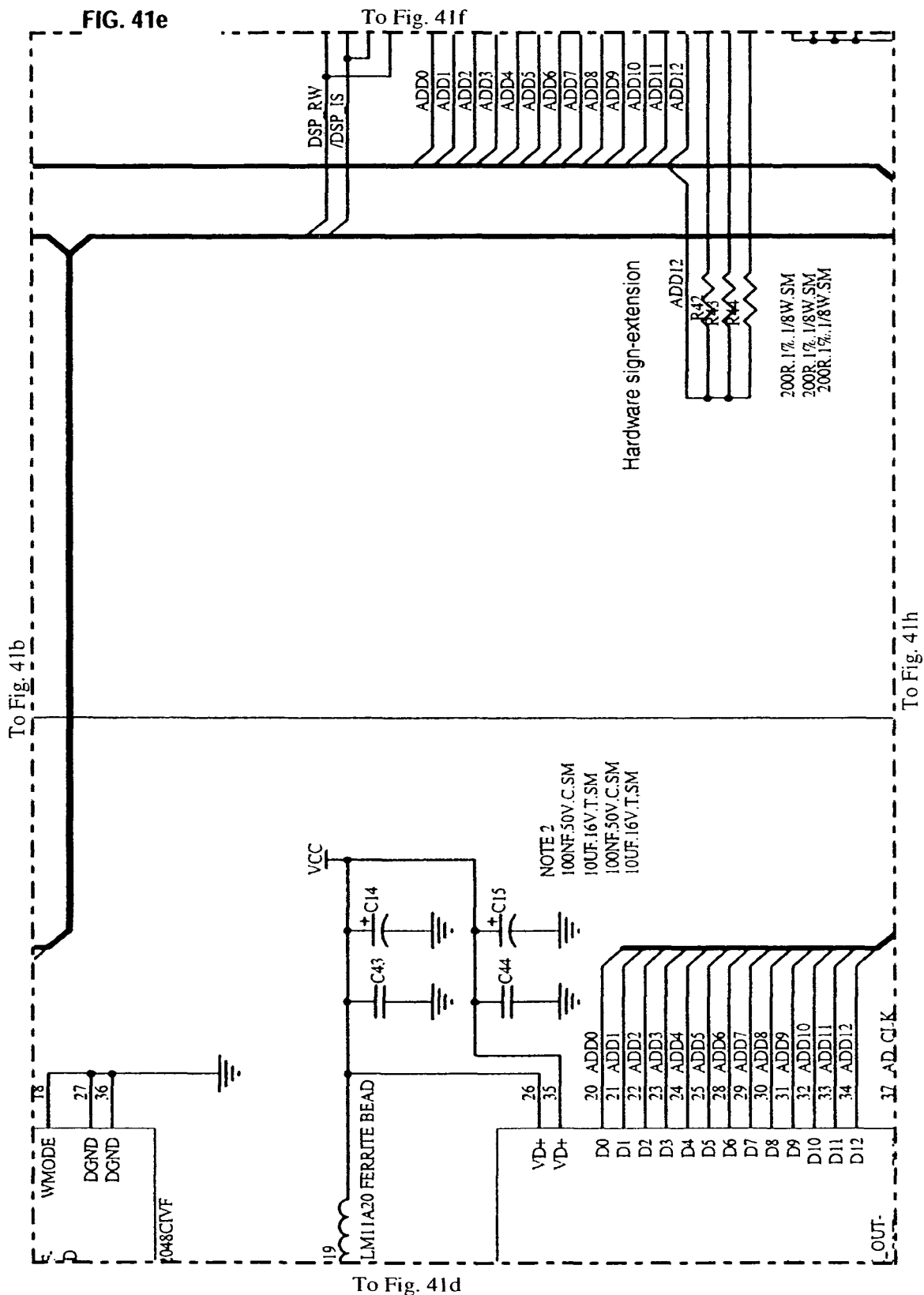
FIG. 41c



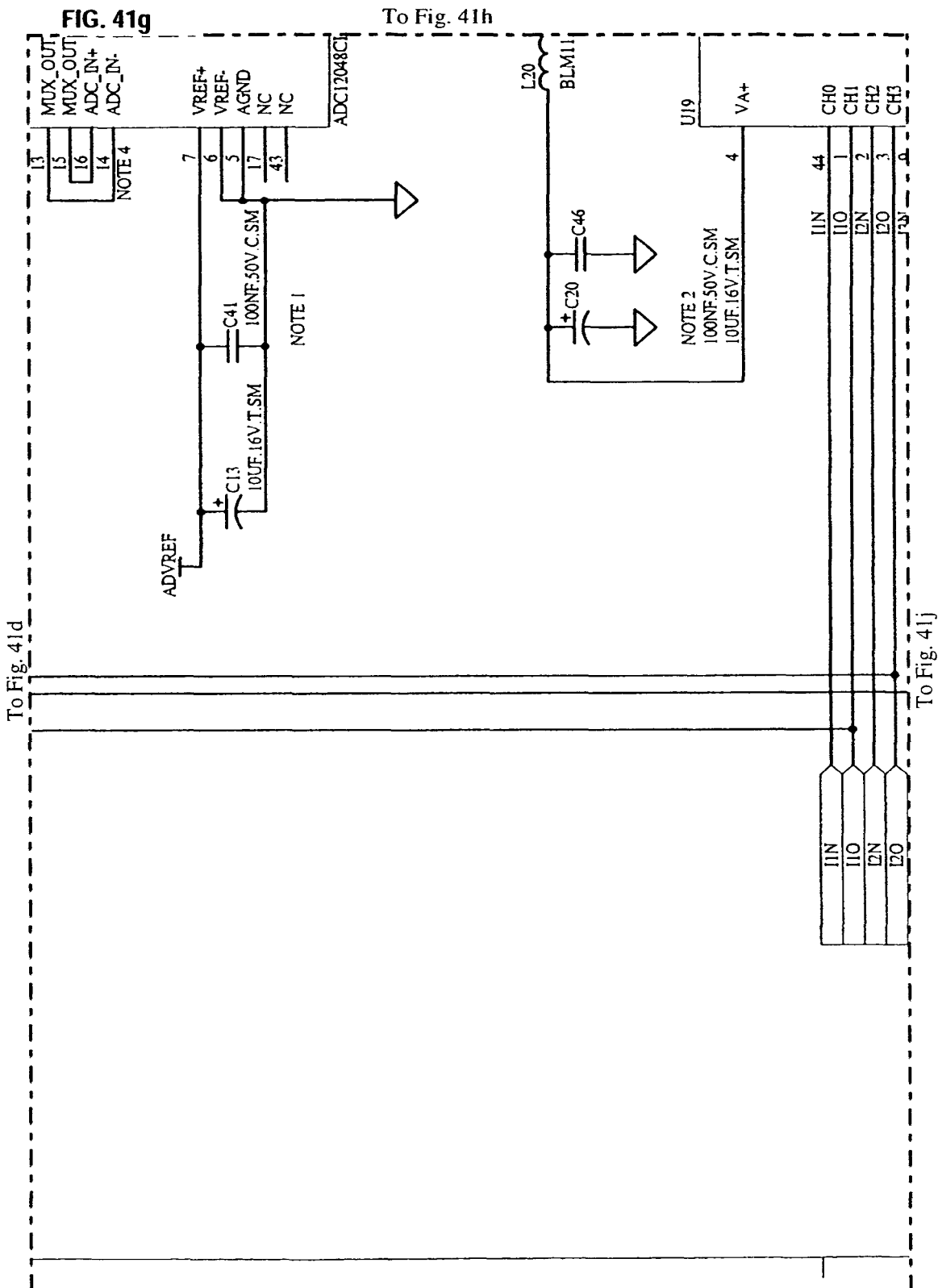
Inventor(s): Rene T. Jonker, Piotr B. Przydatek, Colin N. Gunn, Mike E. Teachman, Constantine A. Antoniou
Attorney Docket No.: OUR CASE NO. 6270/114

Attorney Docket No.: OUR CASE NO. 6270/114





To Fig. 41e



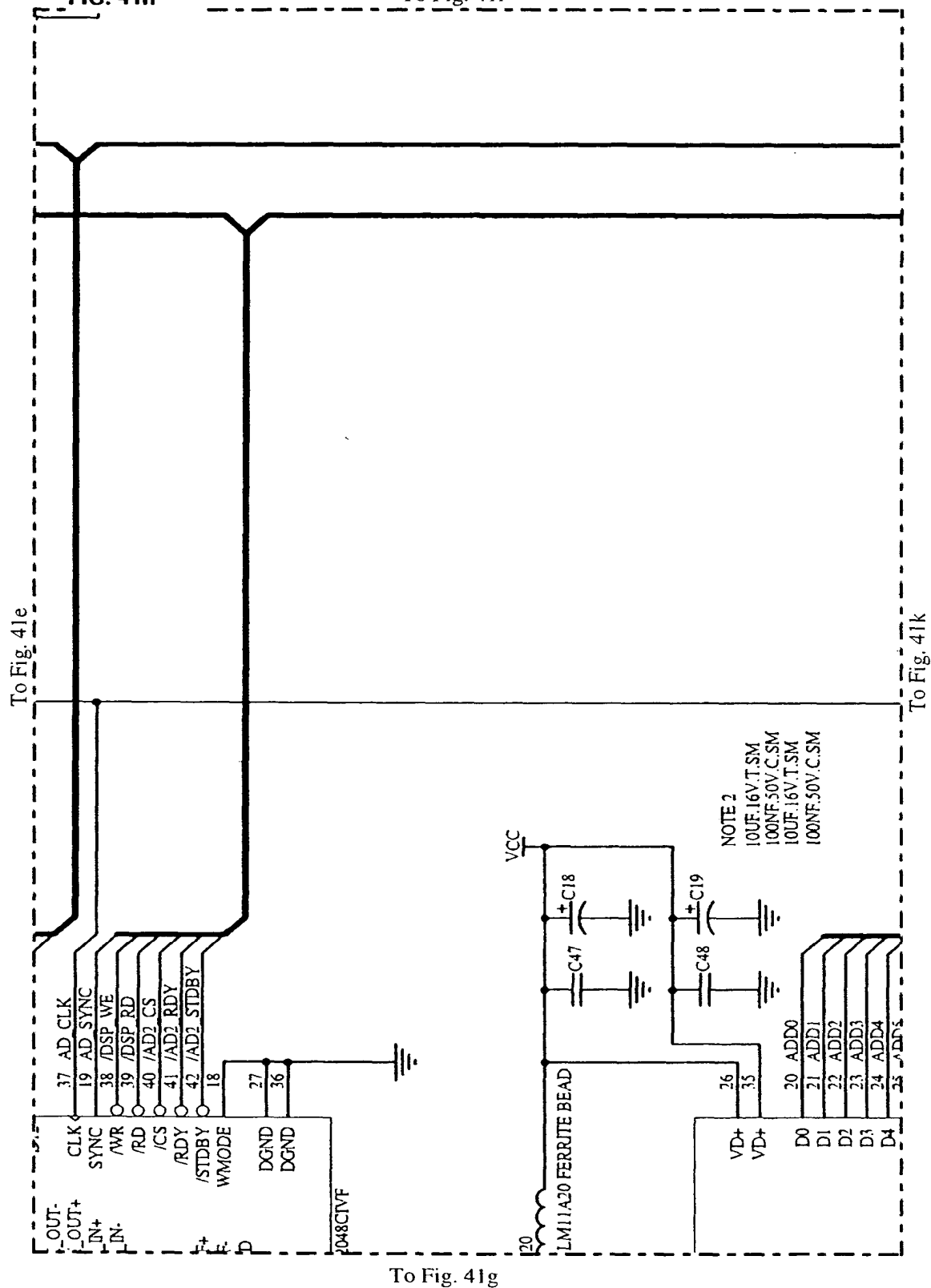
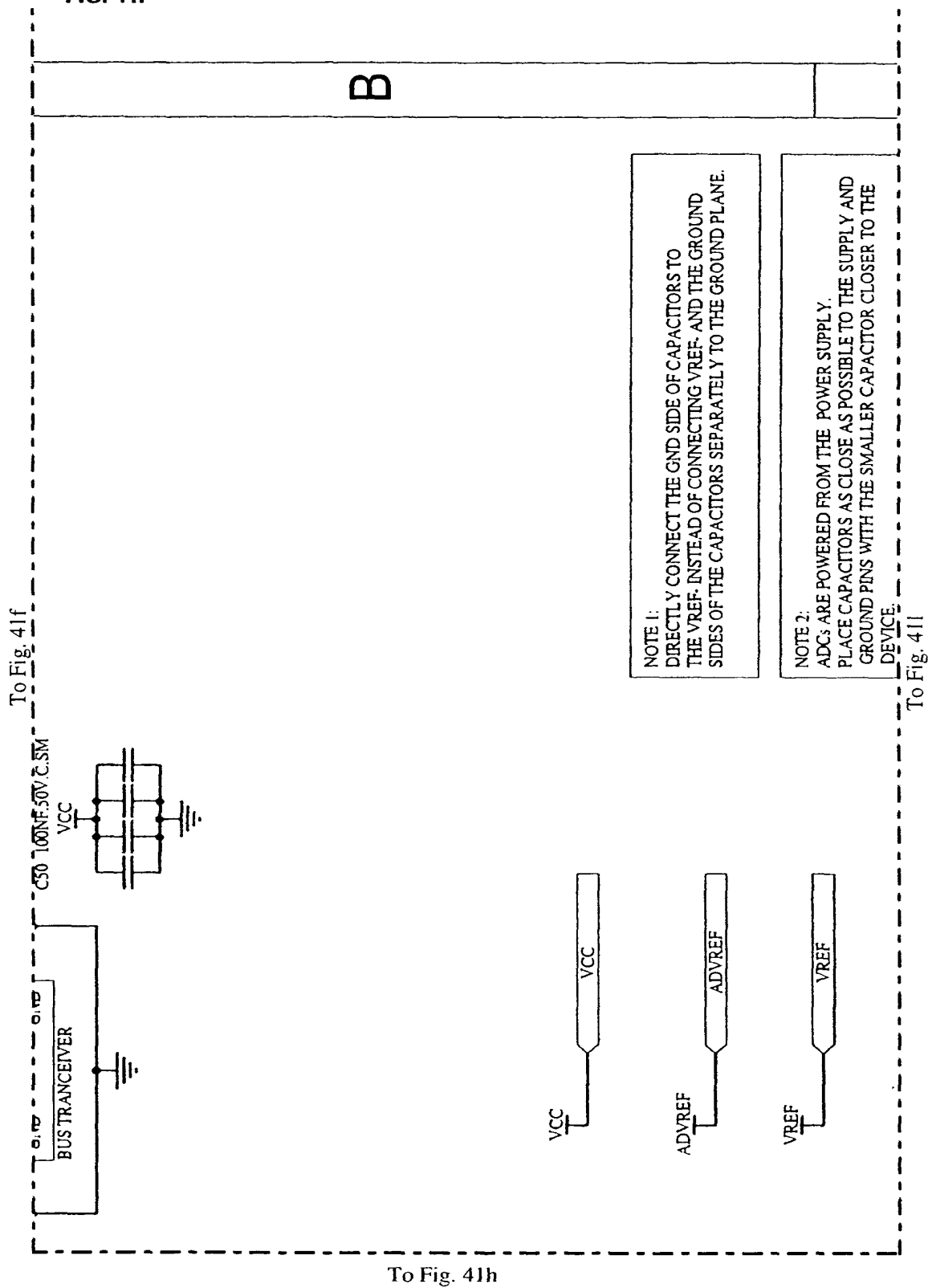
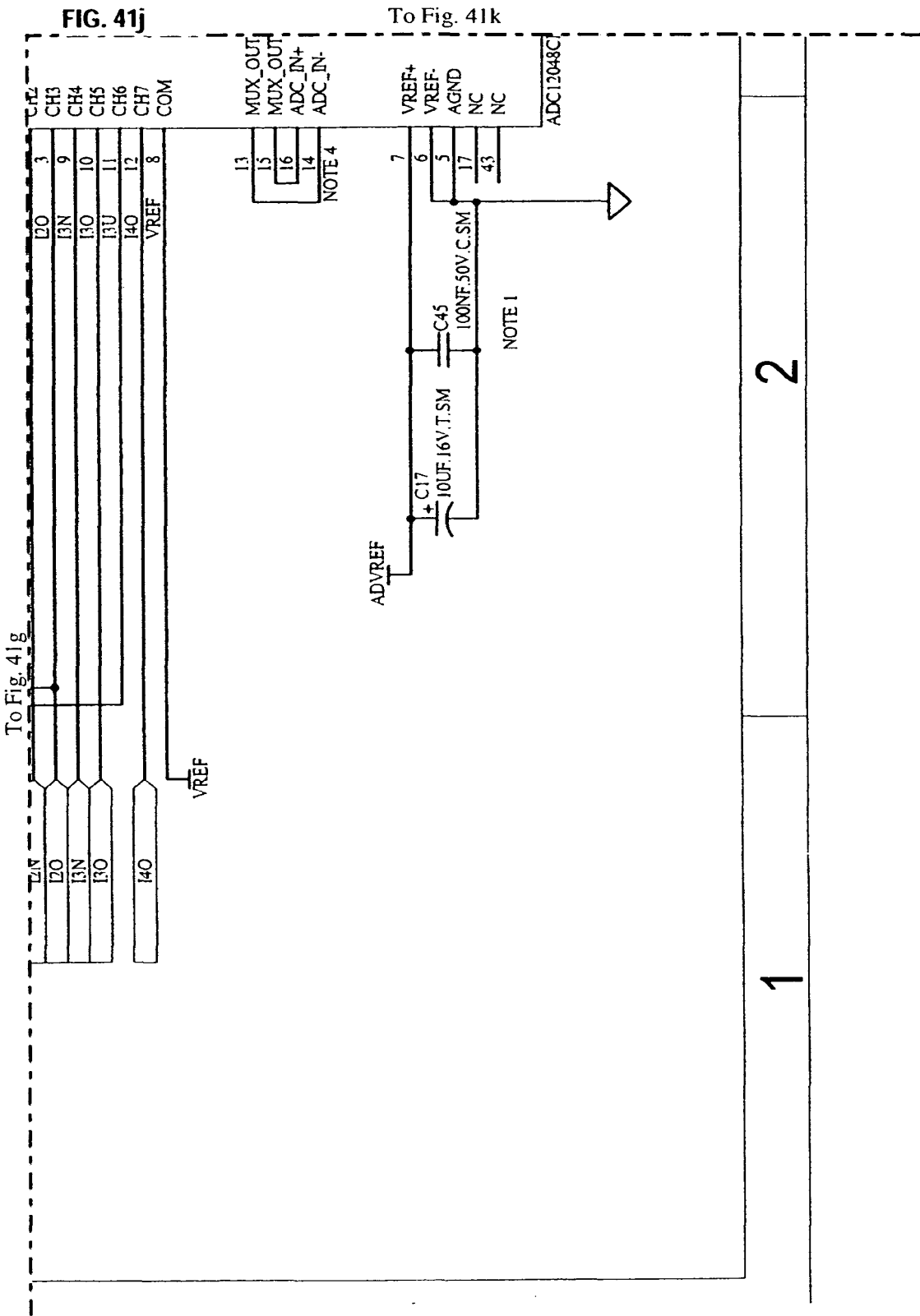


FIG. 41i





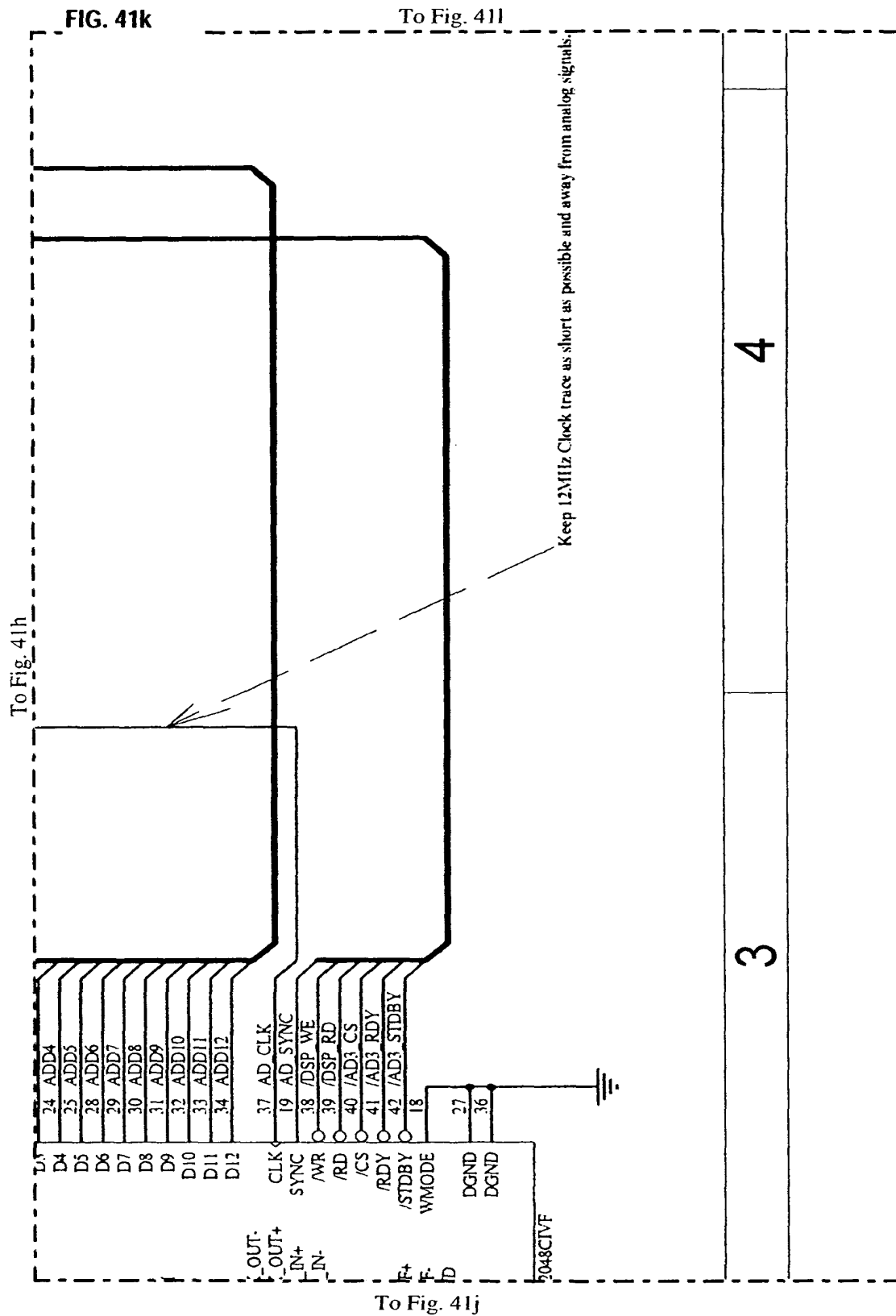


FIG. 41I

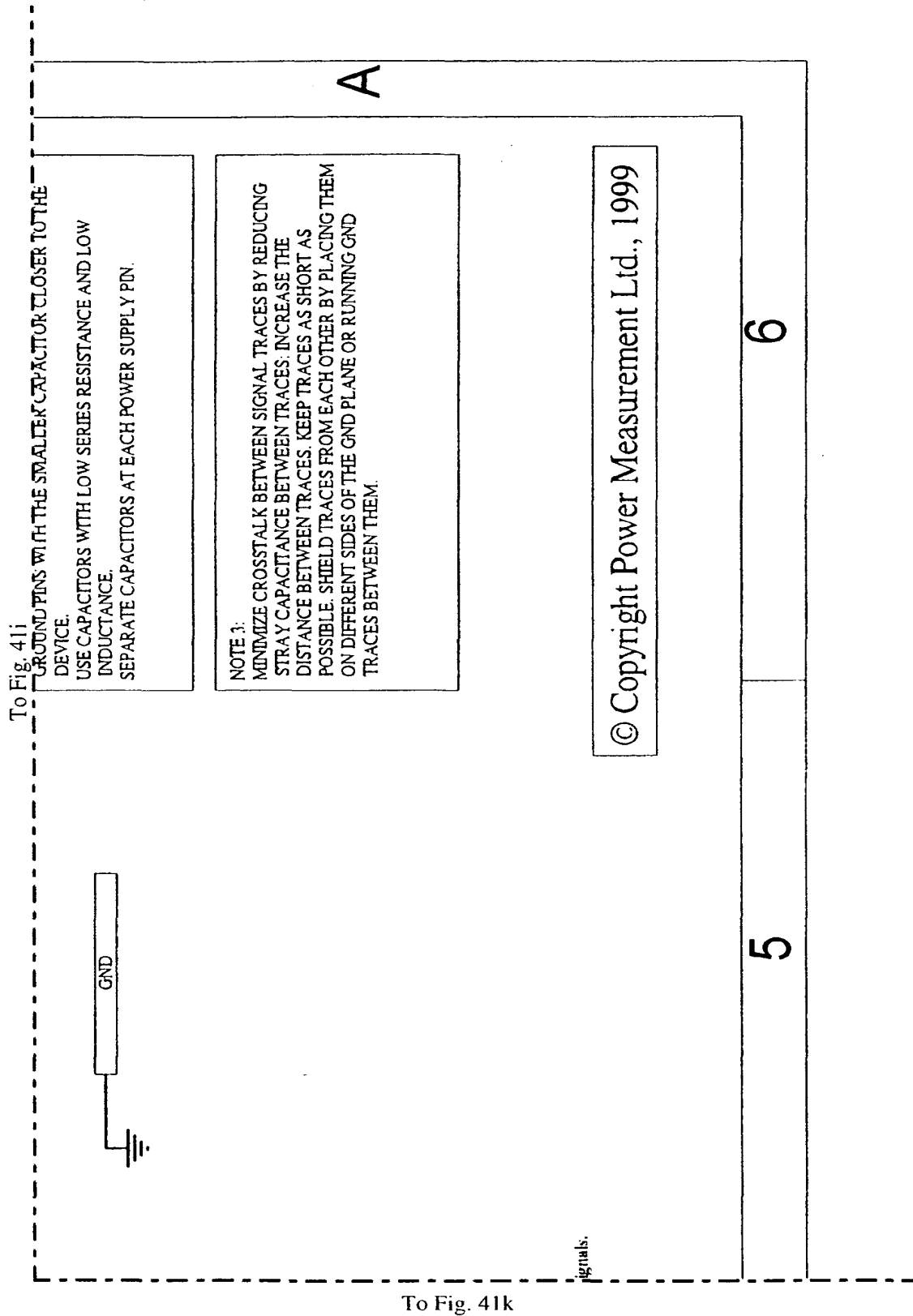


FIG. 42a

To Fig. 42b

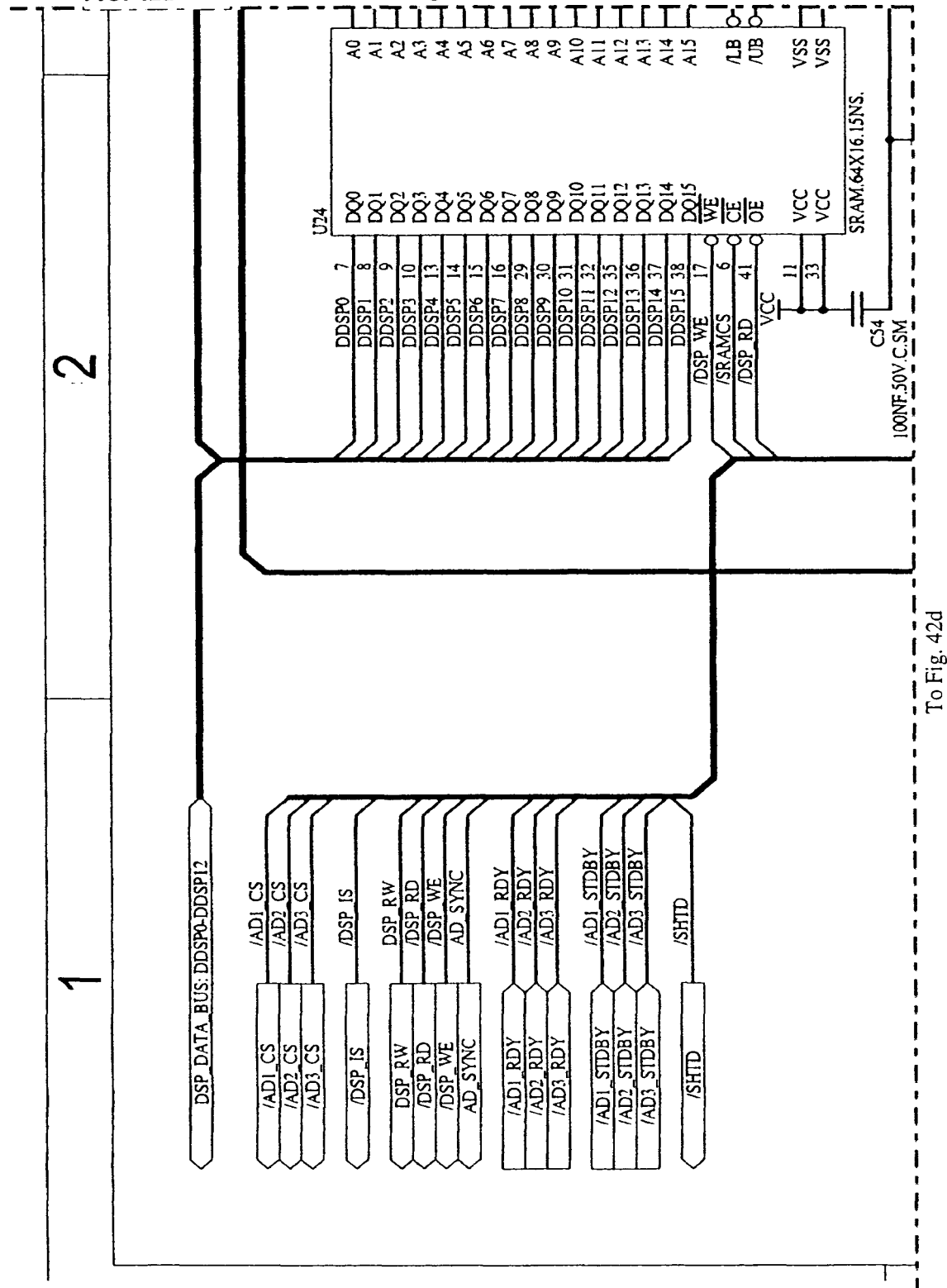


FIG. 42b

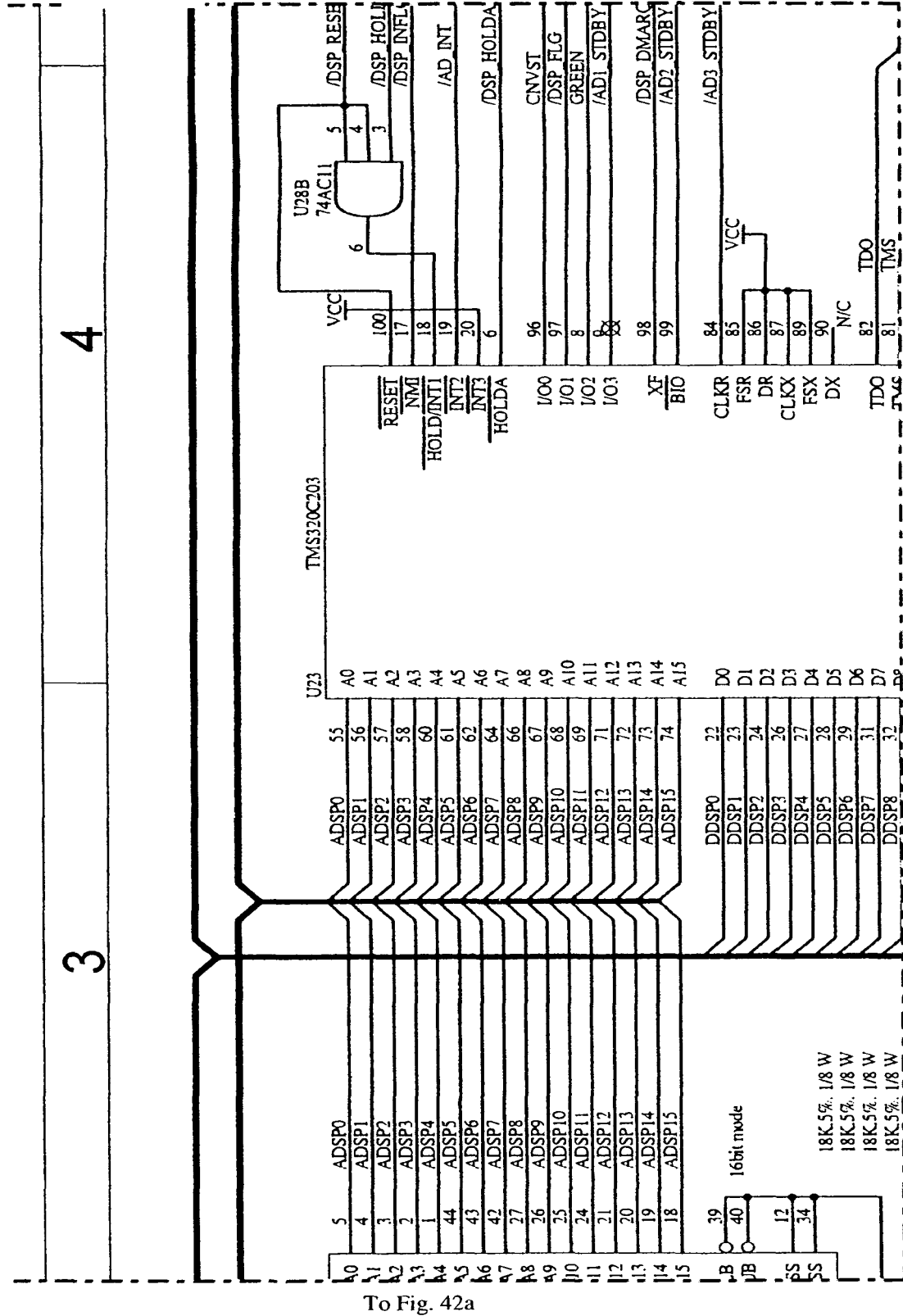
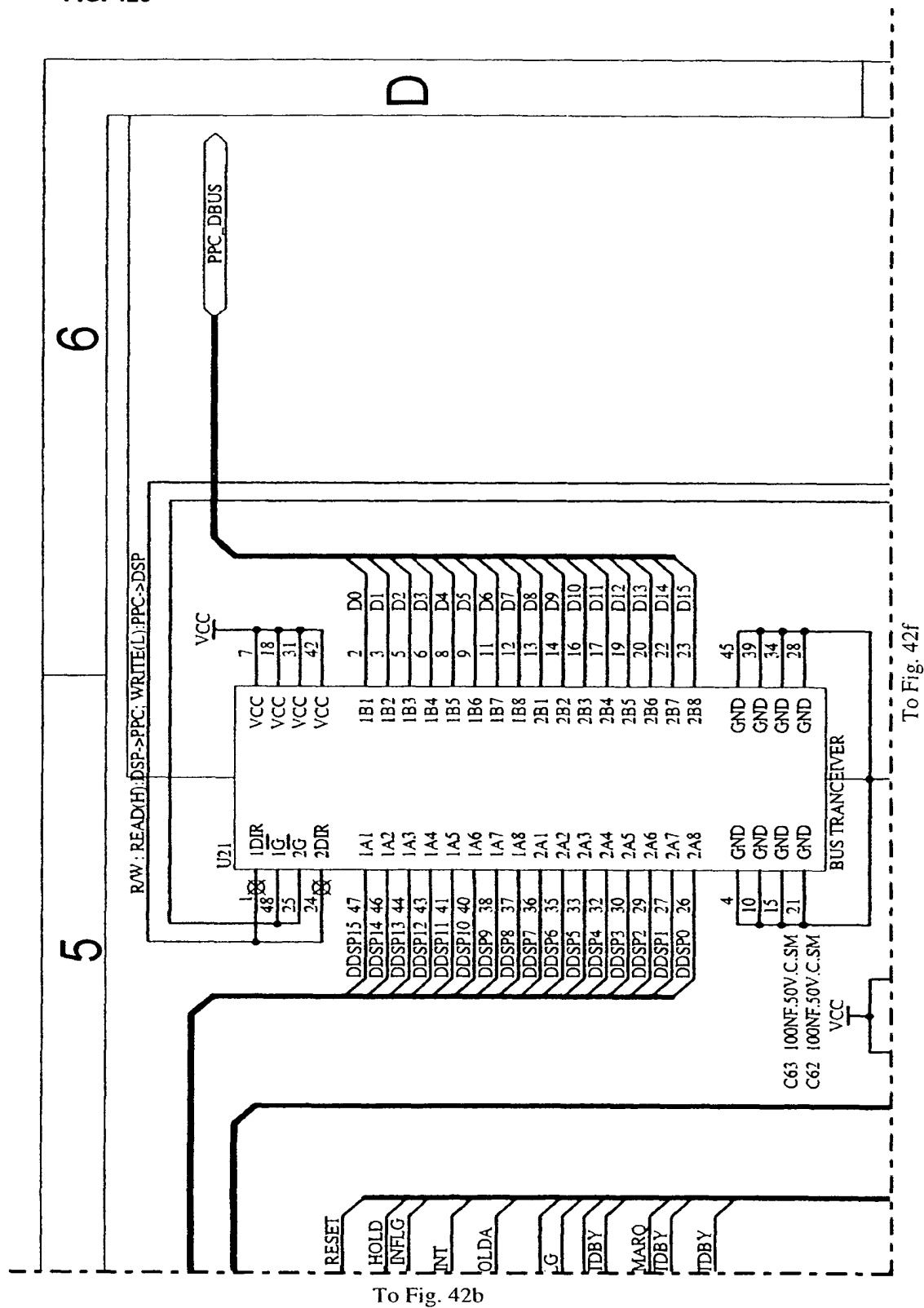
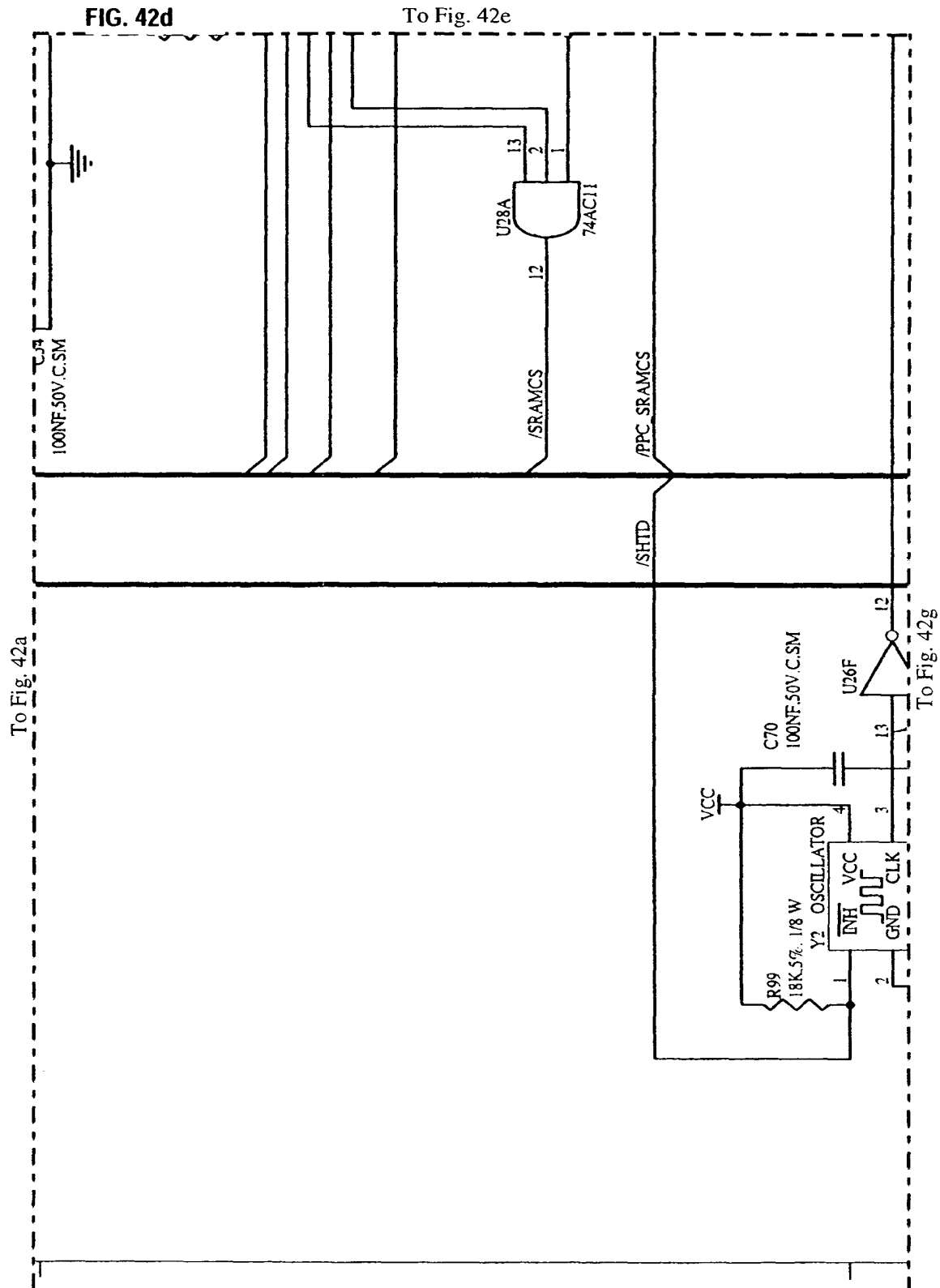


FIG. 42c





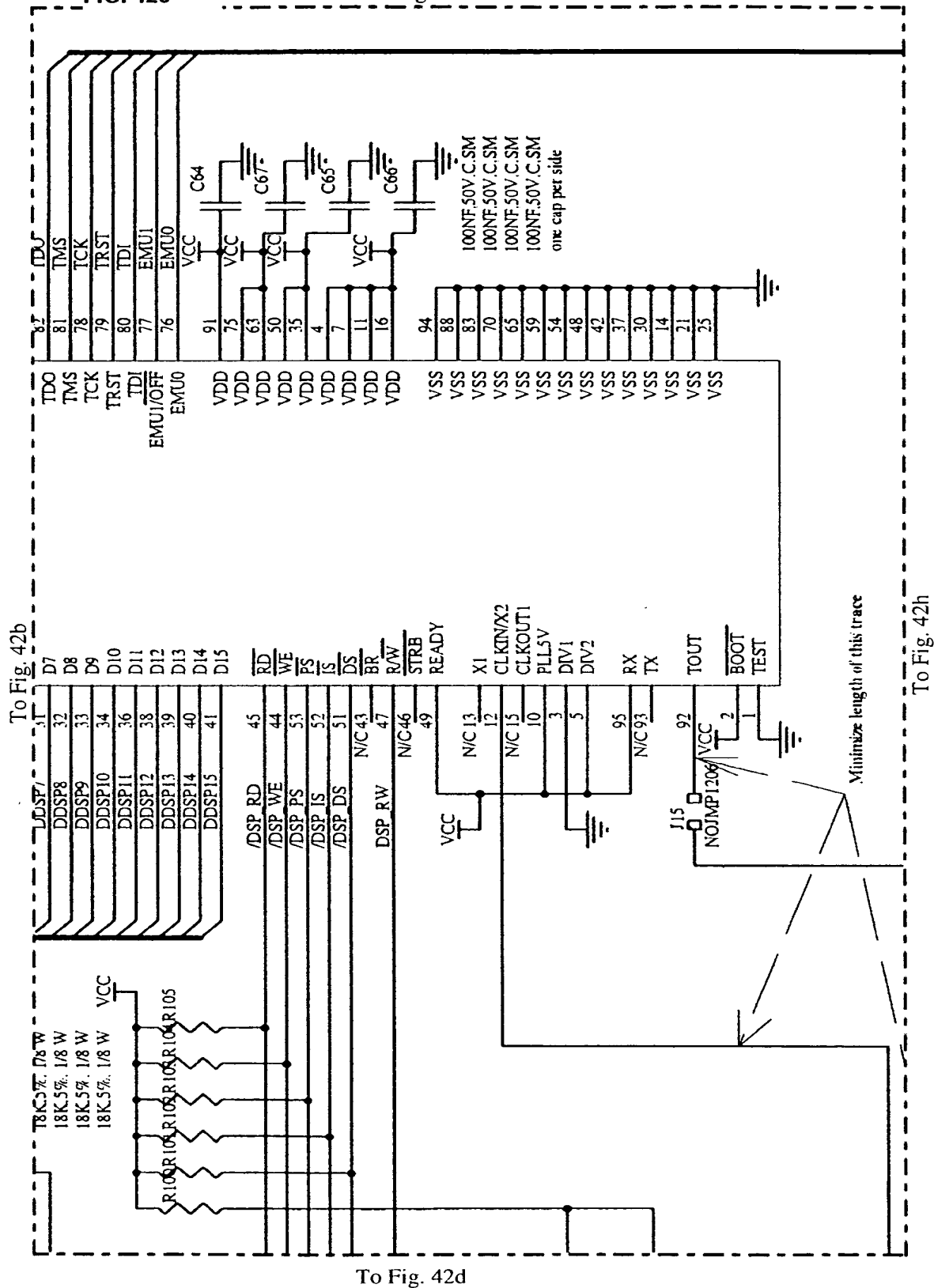
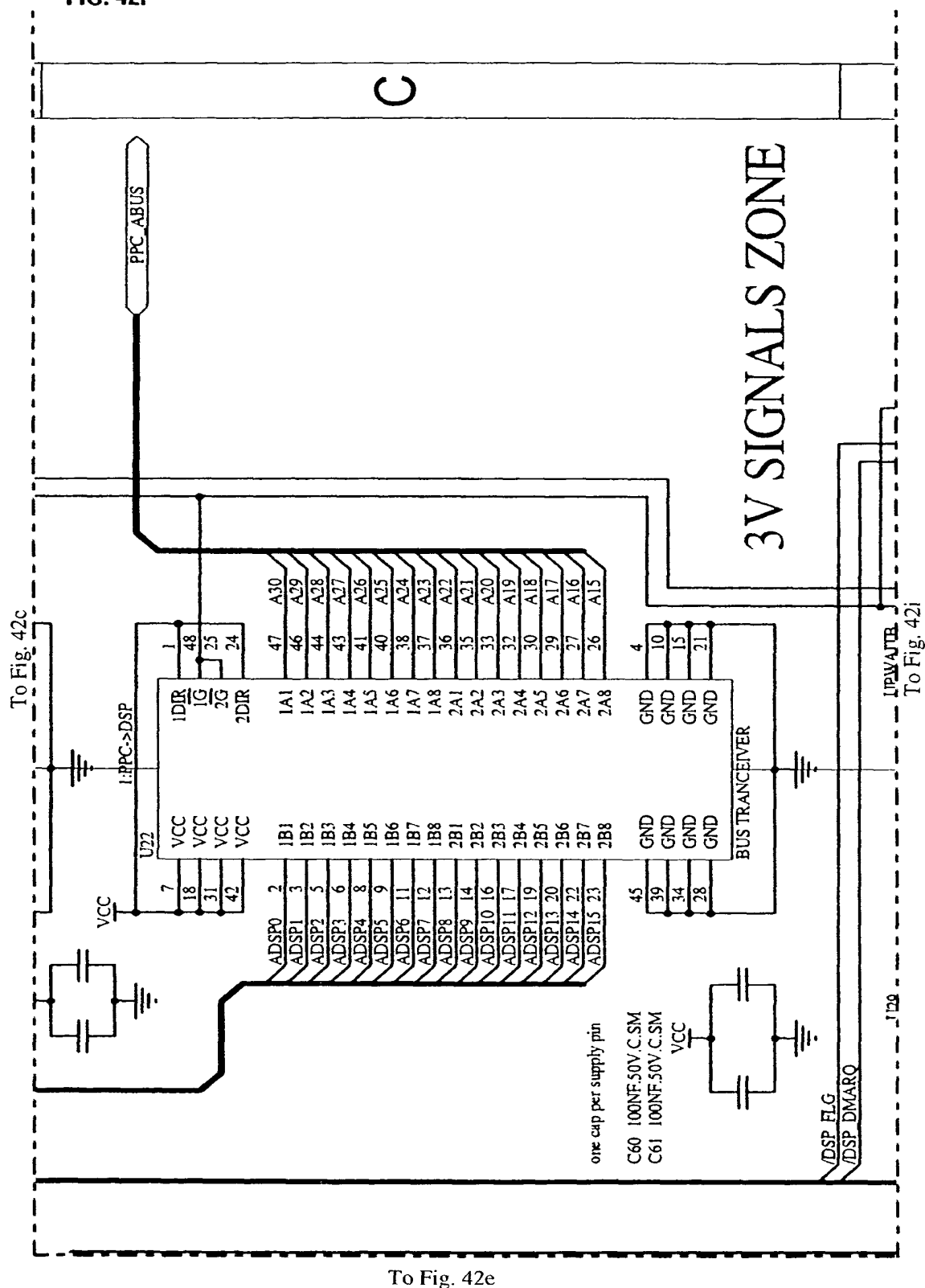
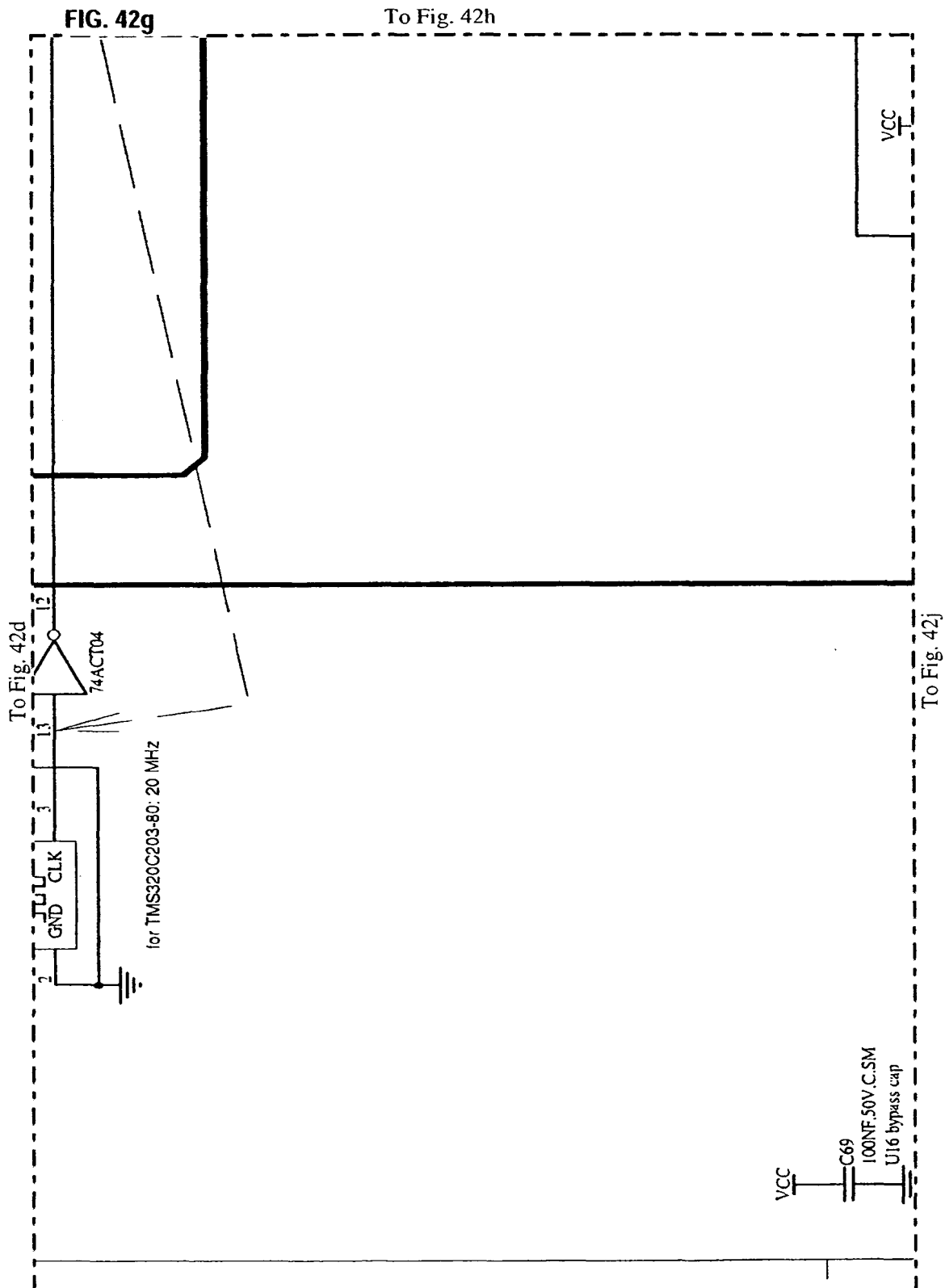


FIG. 42f





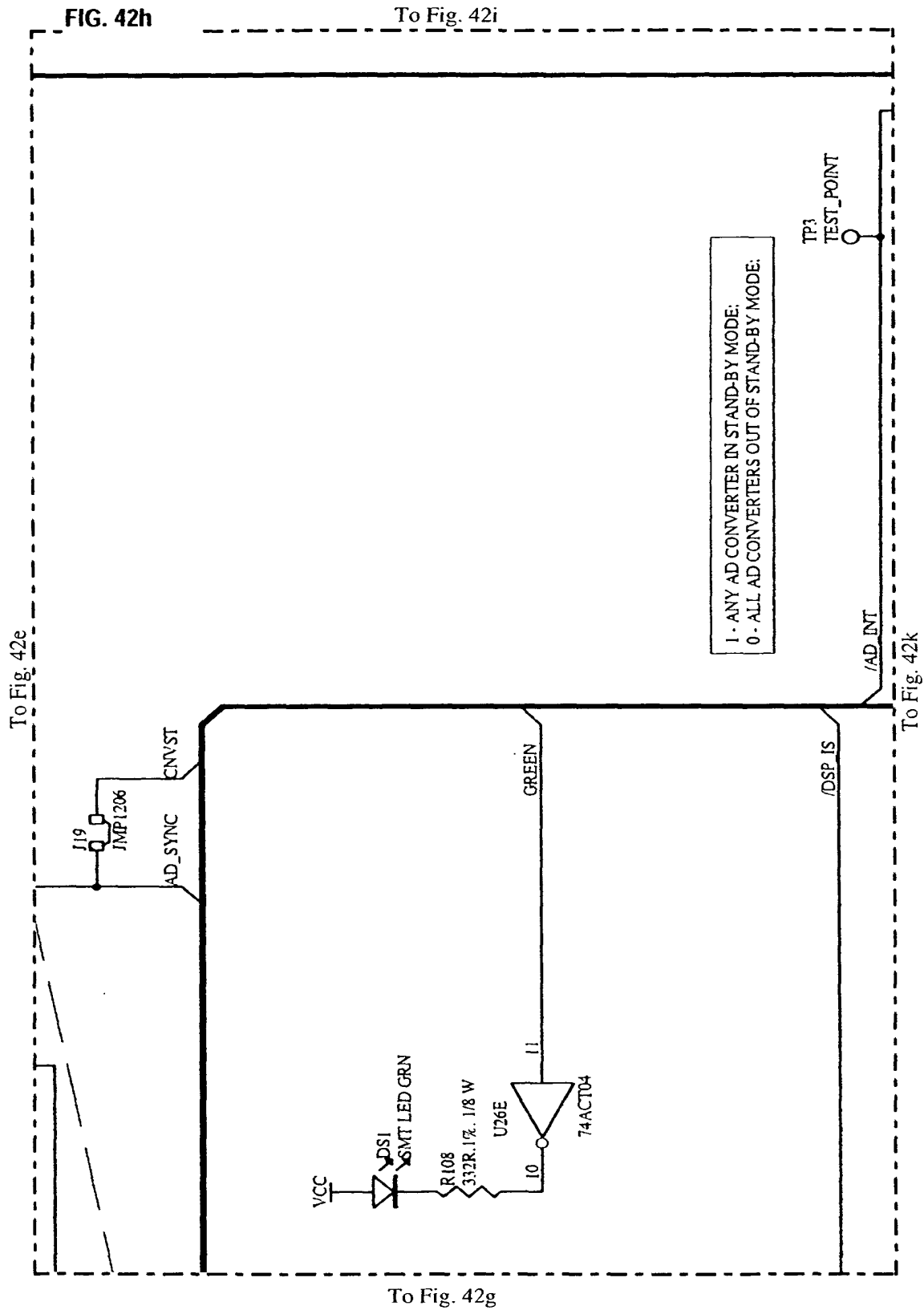
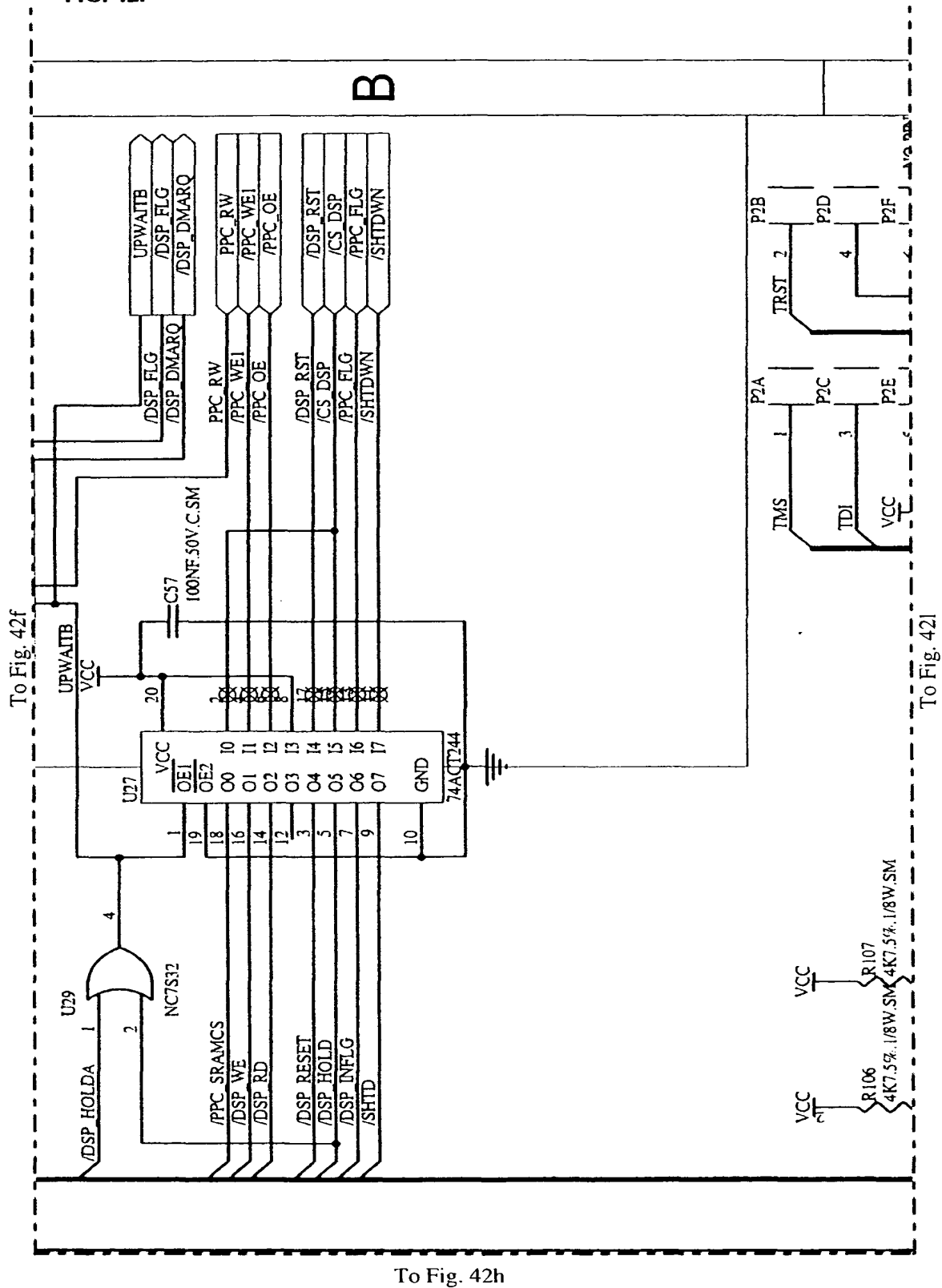
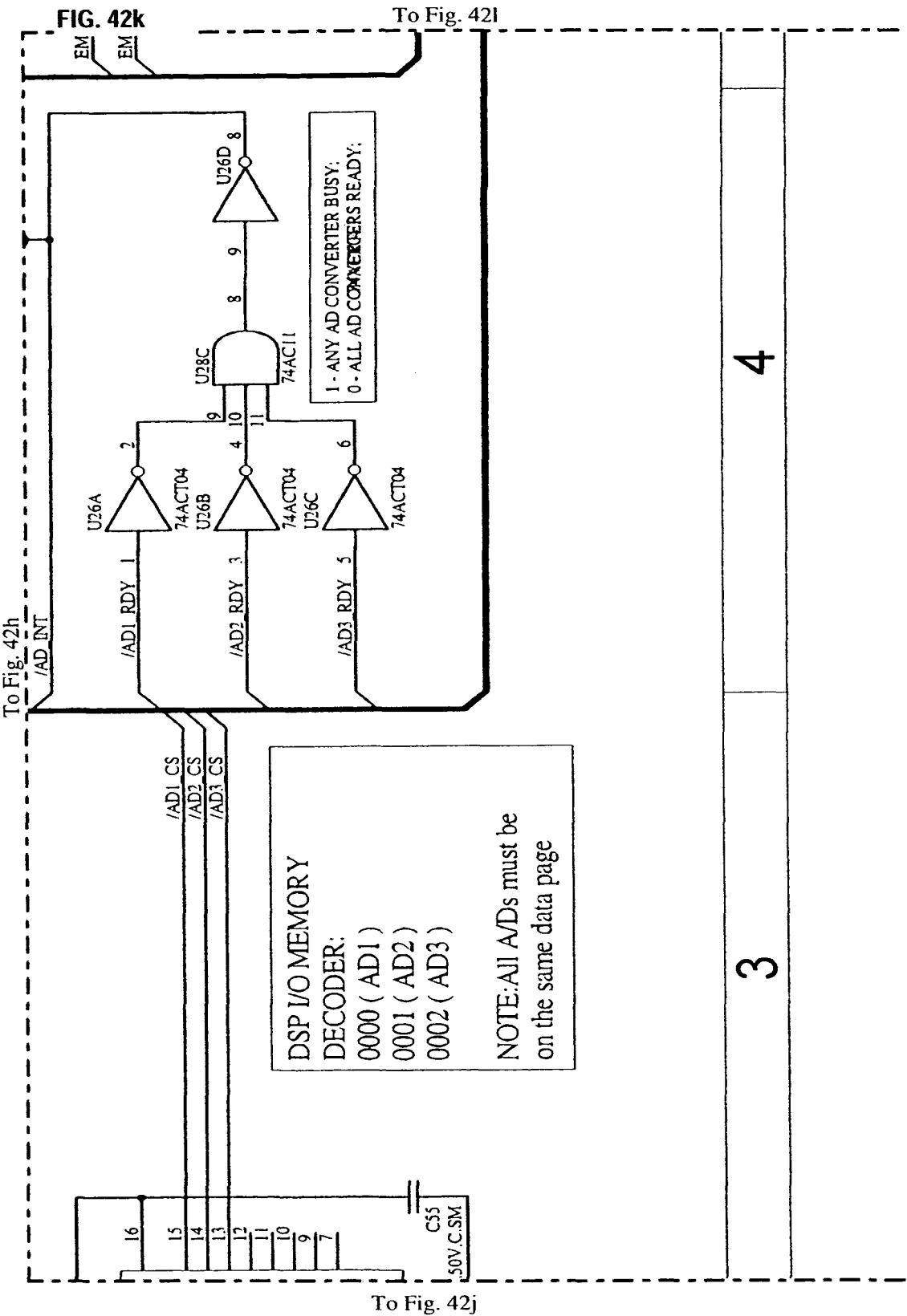
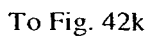


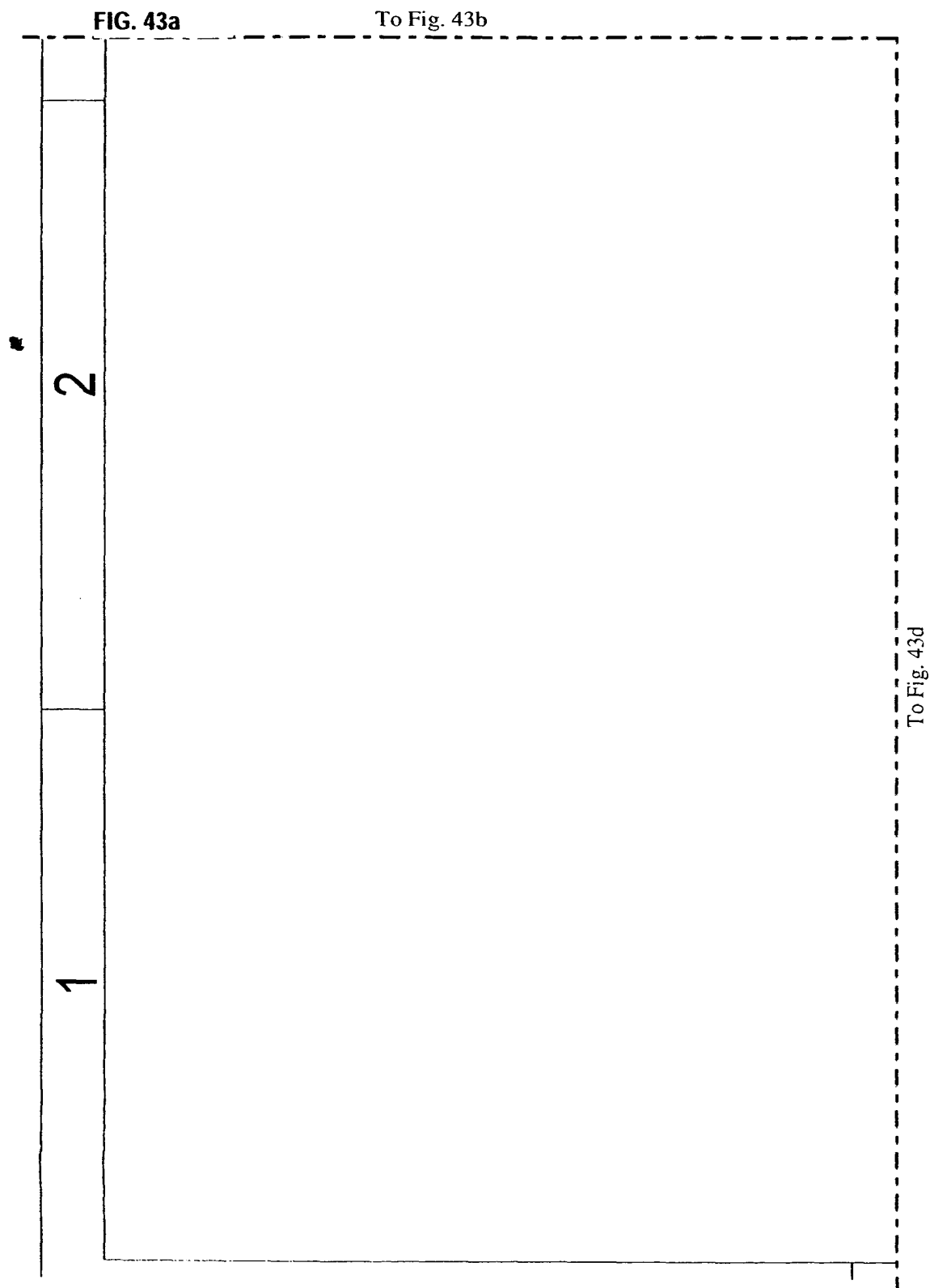
FIG. 42i



To Fig. 42h







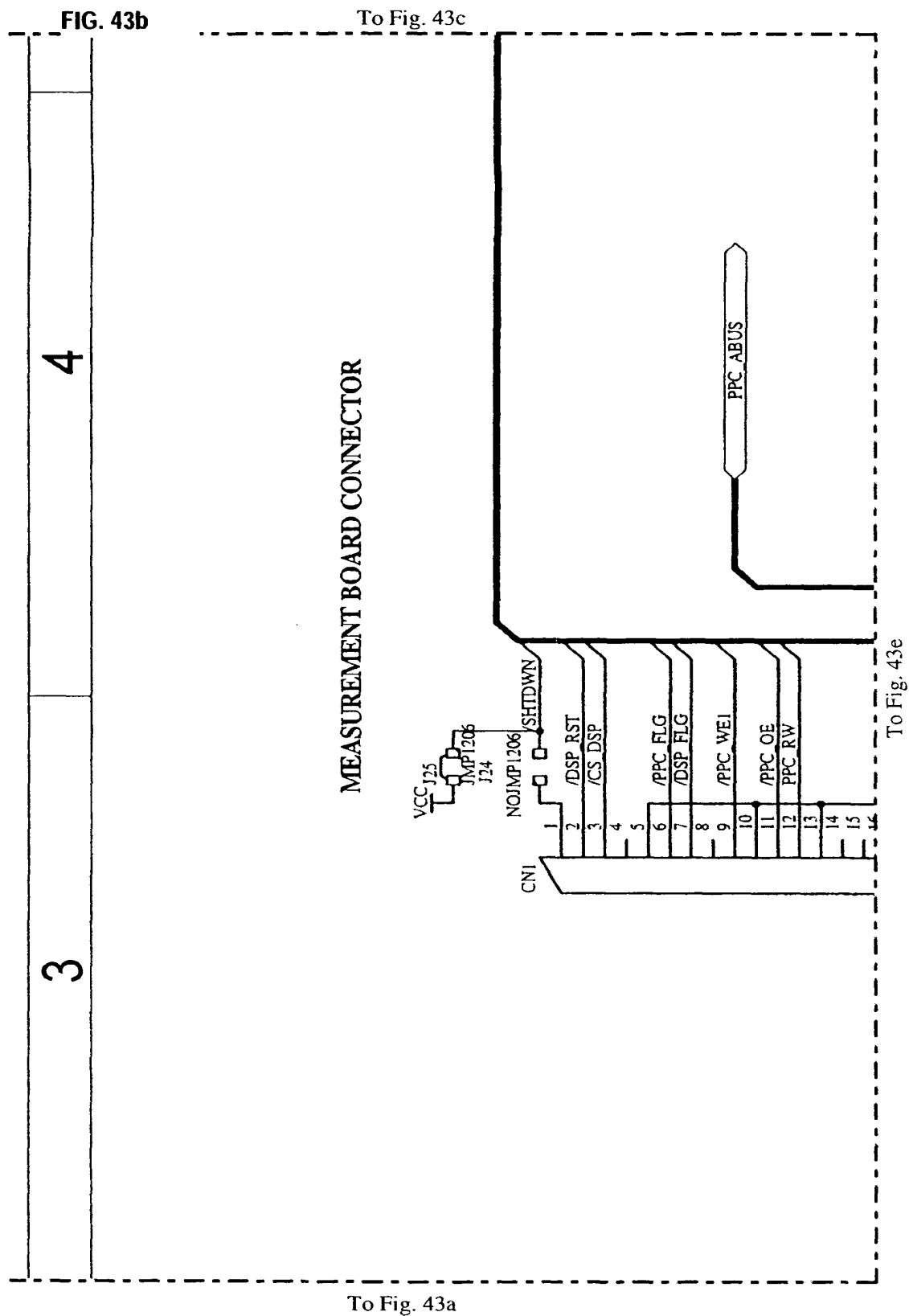


FIG. 43c

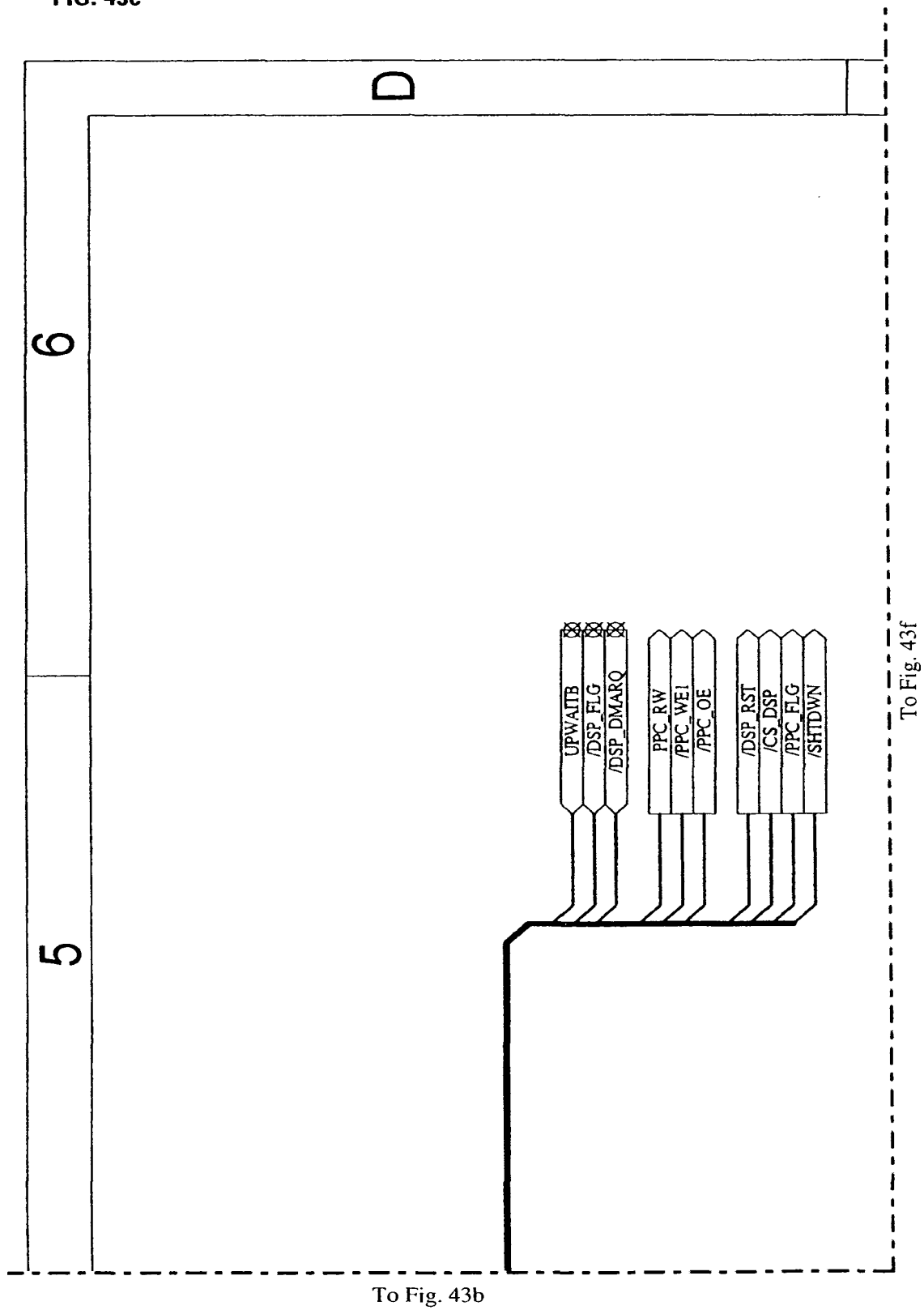


FIG. 43d

To Fig. 43e

To Fig. 43a

To Fig. 43g

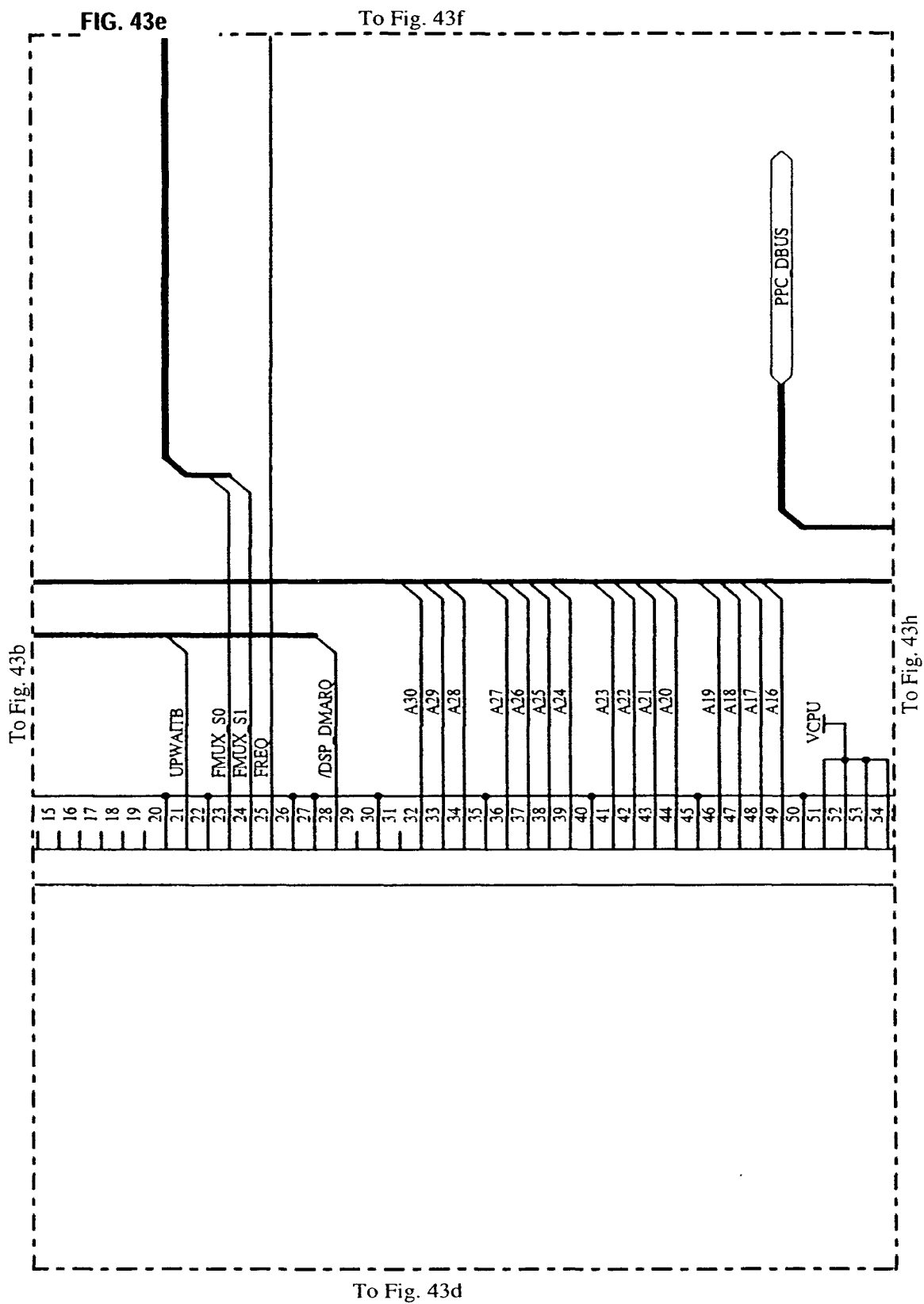


FIG. 43f

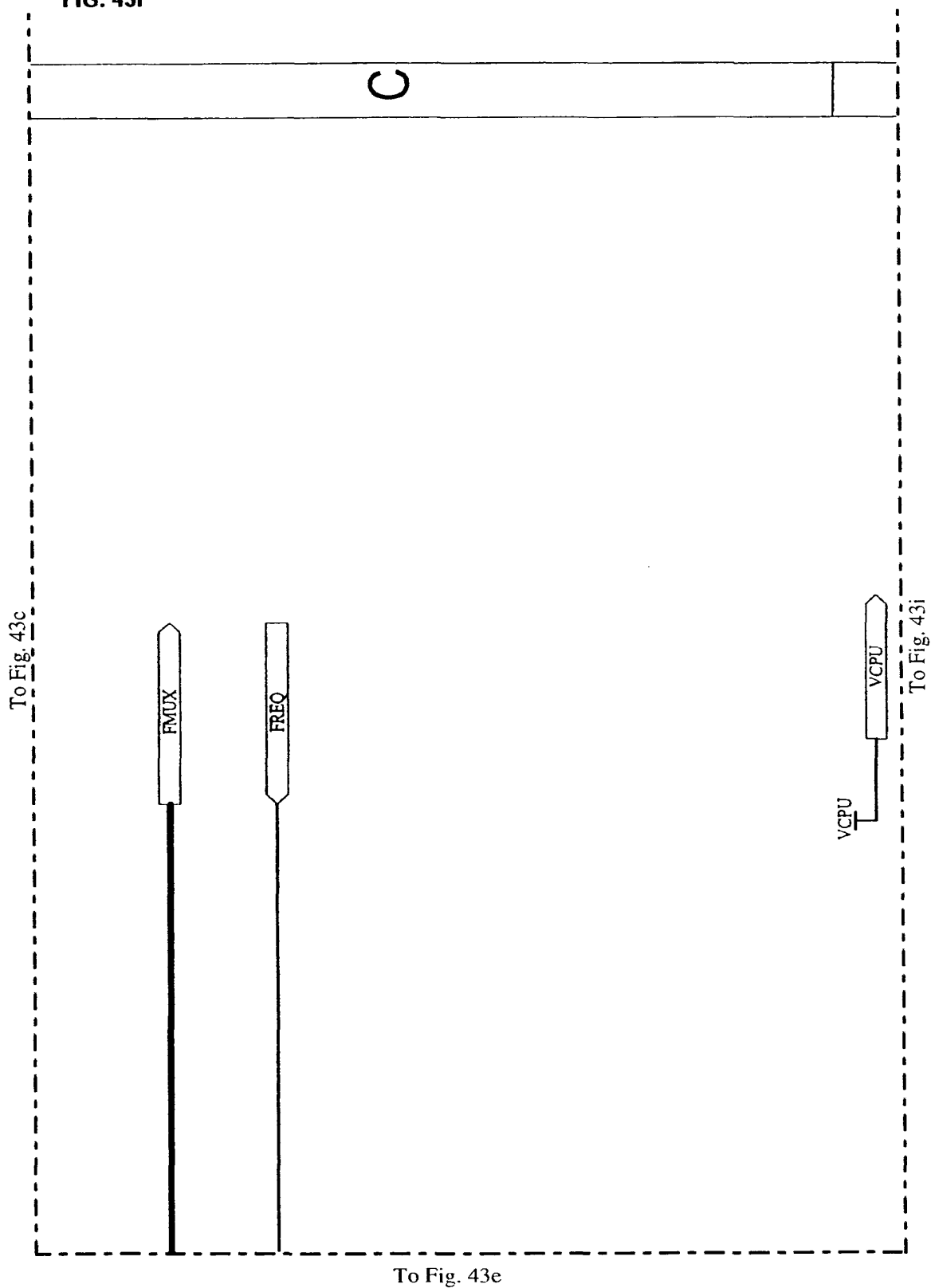


FIG. 43g

To Fig. 43h

To Fig. 43d

To Fig. 43j

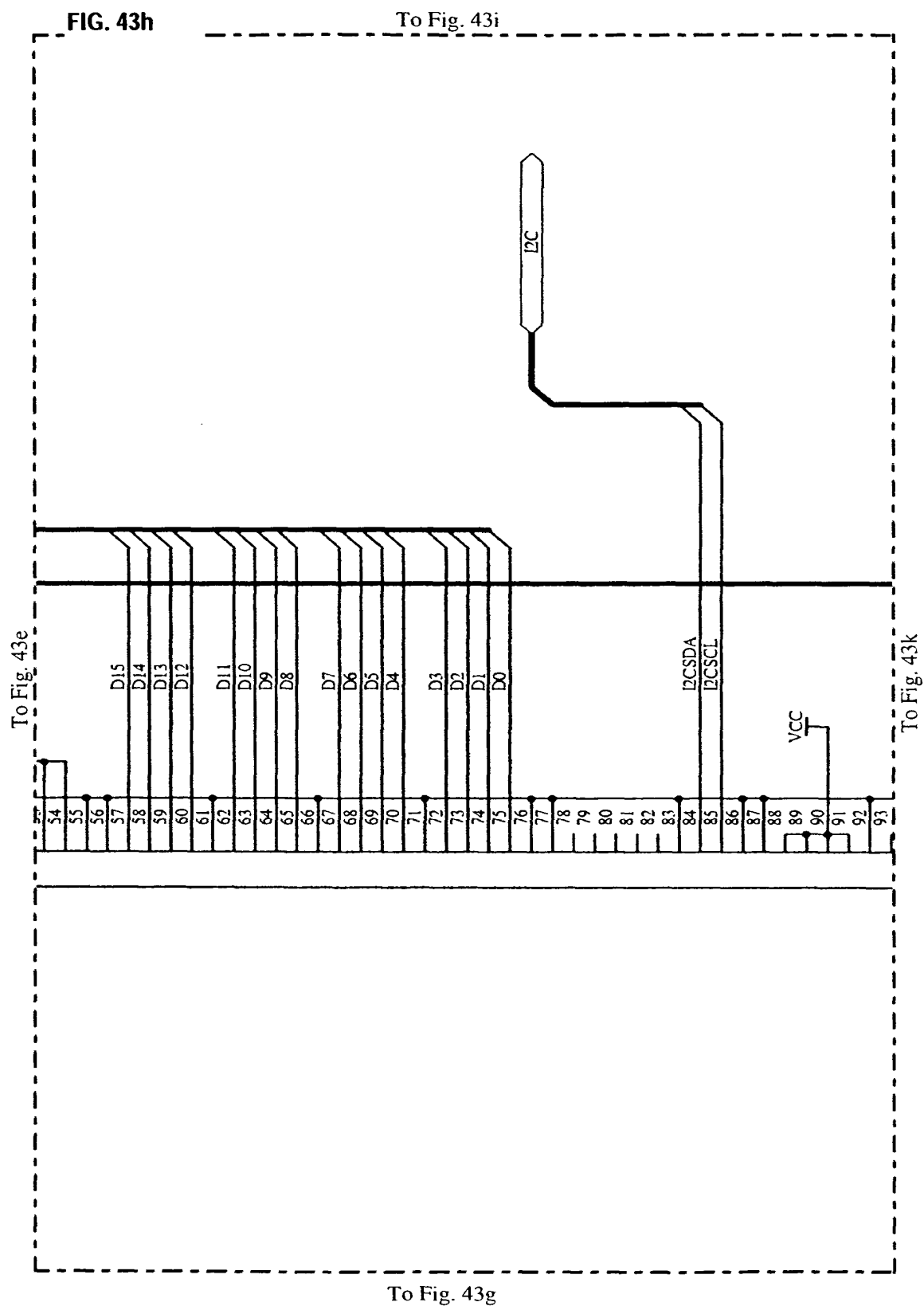
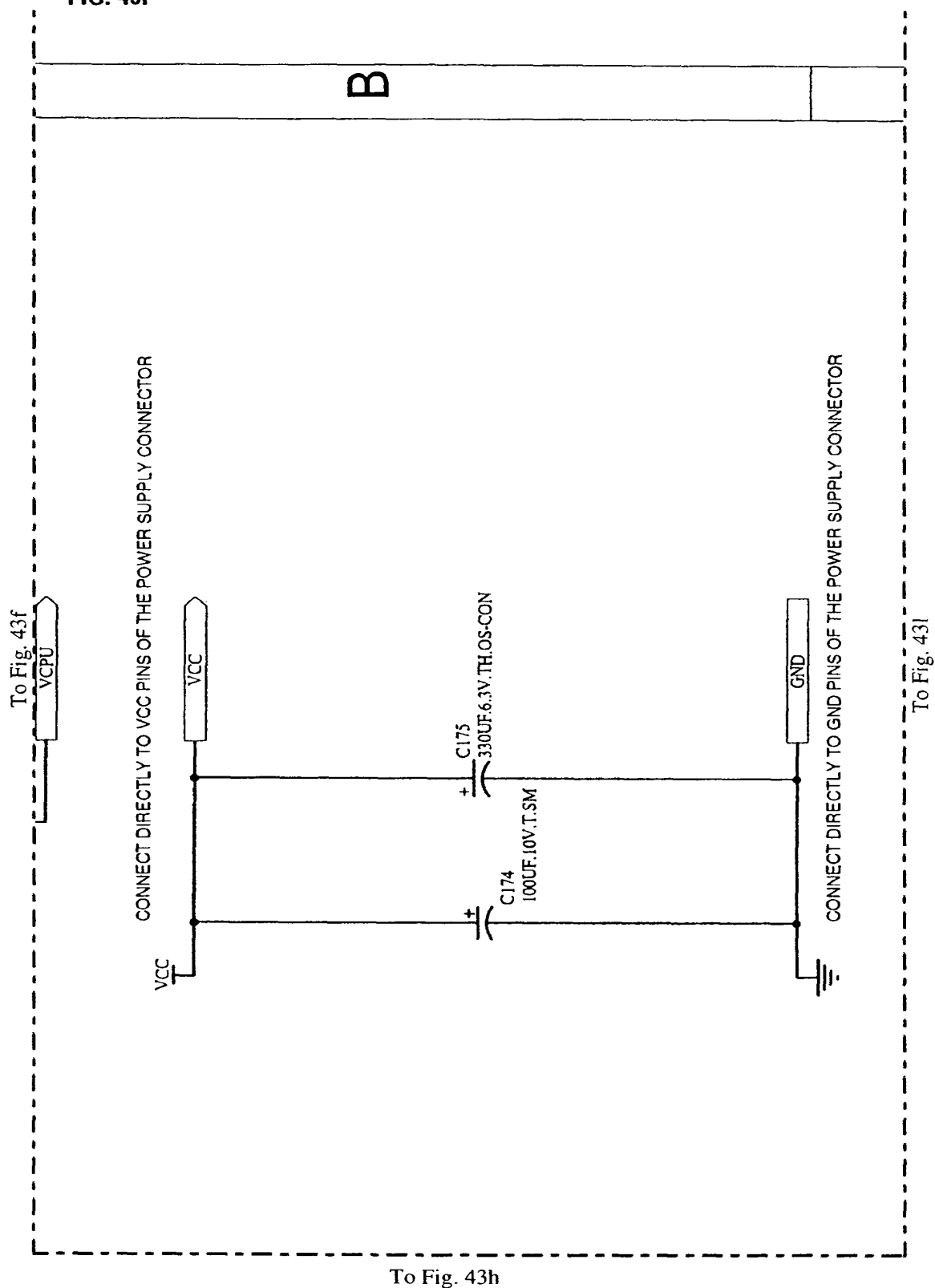
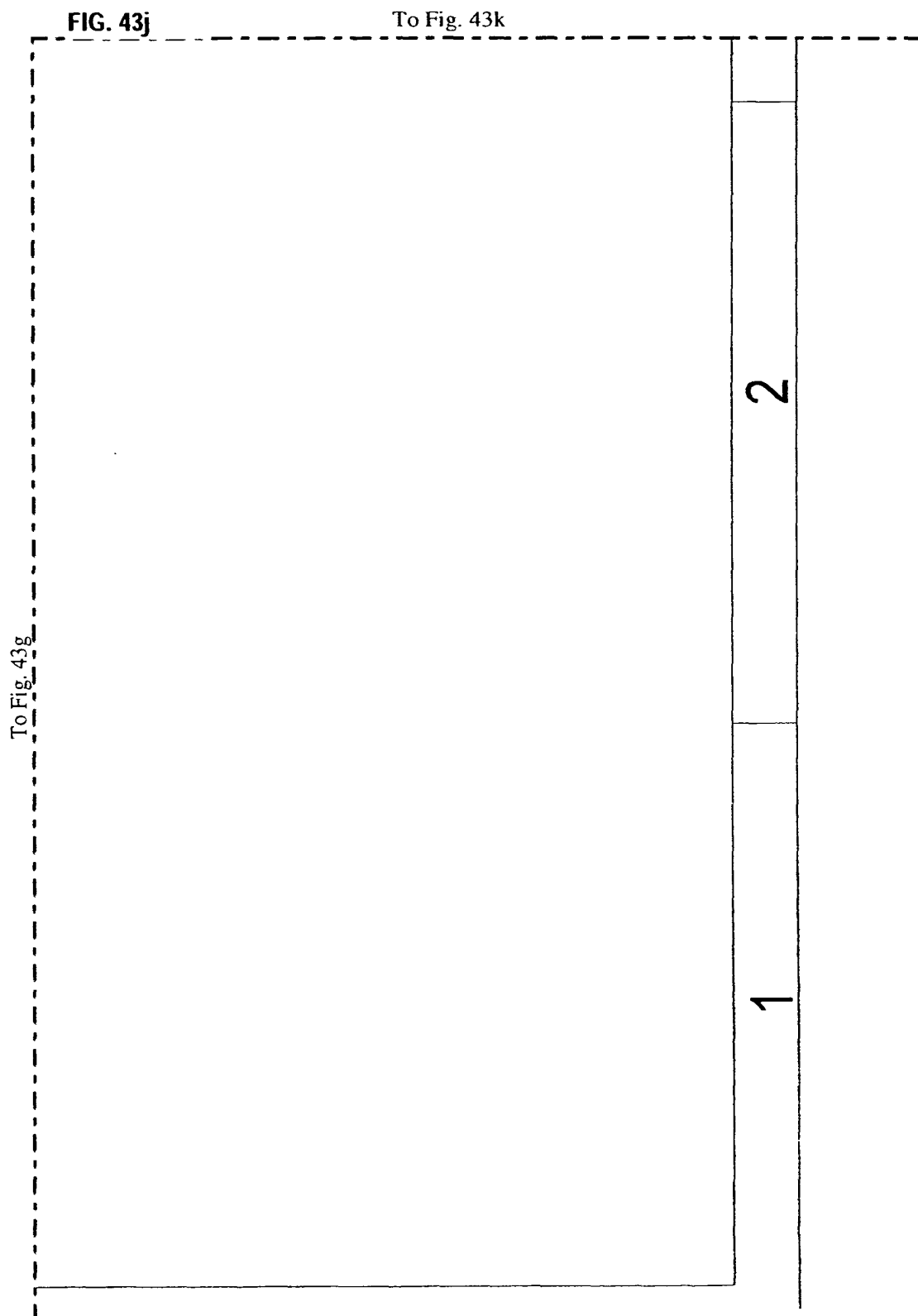


FIG. 43i





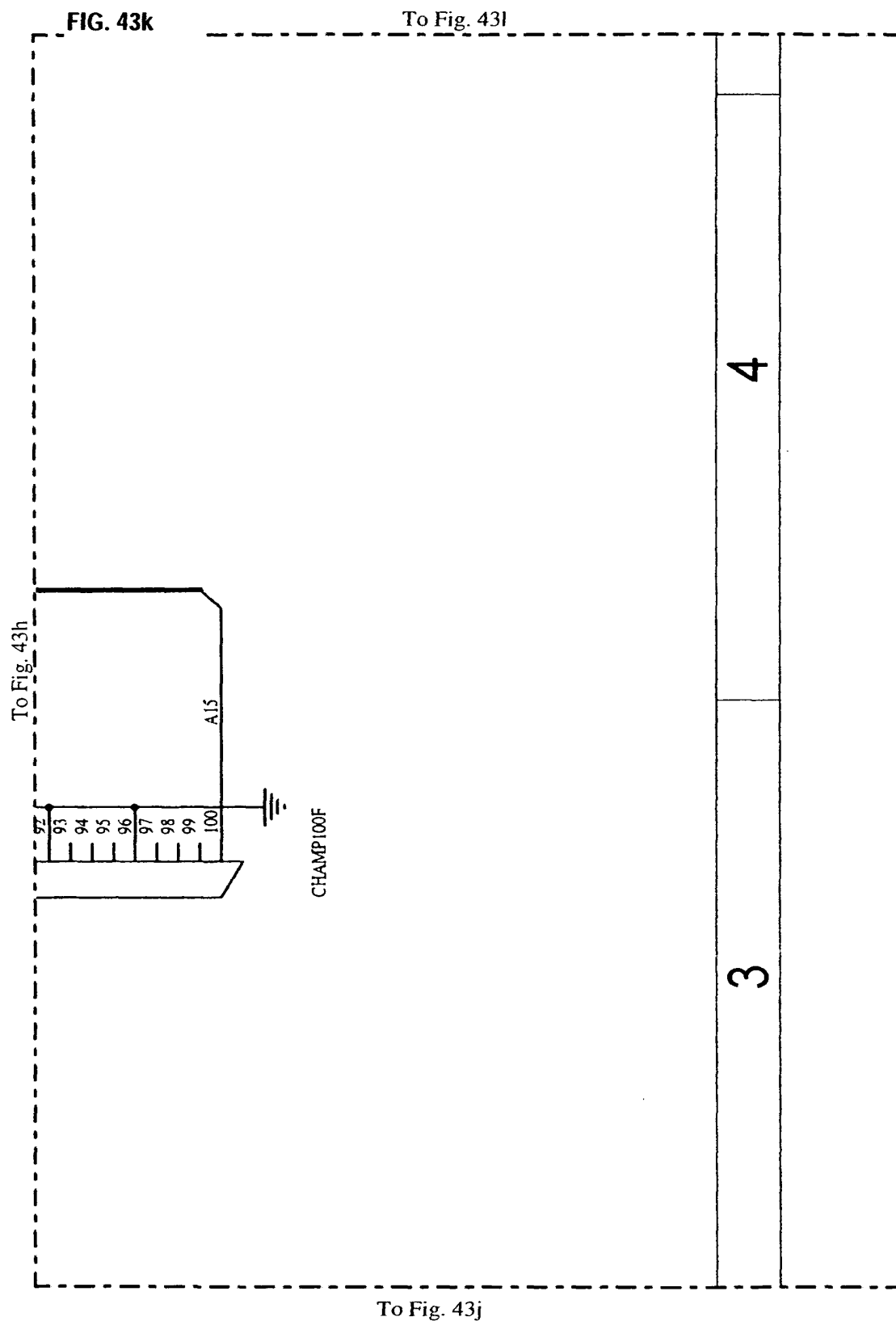
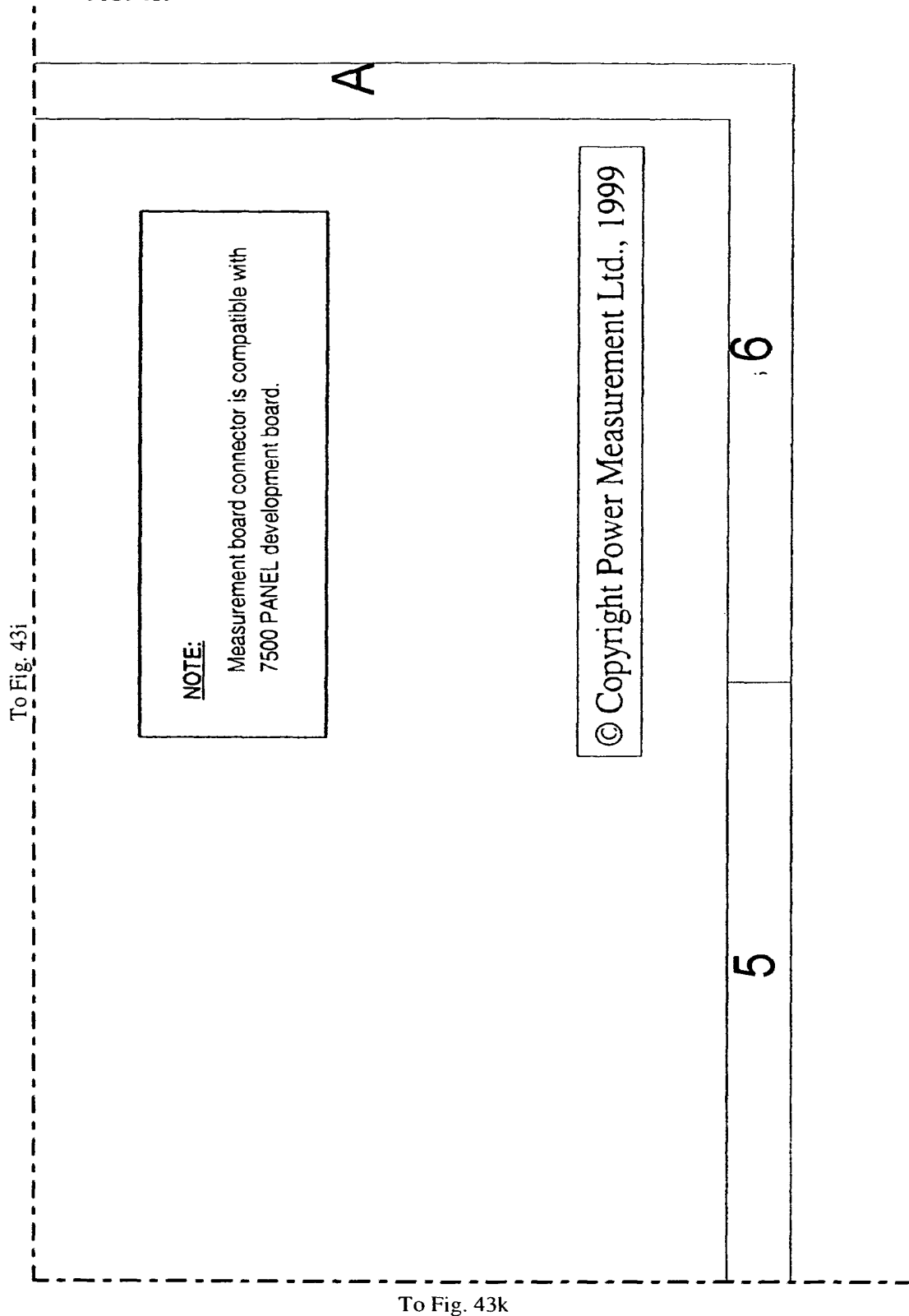
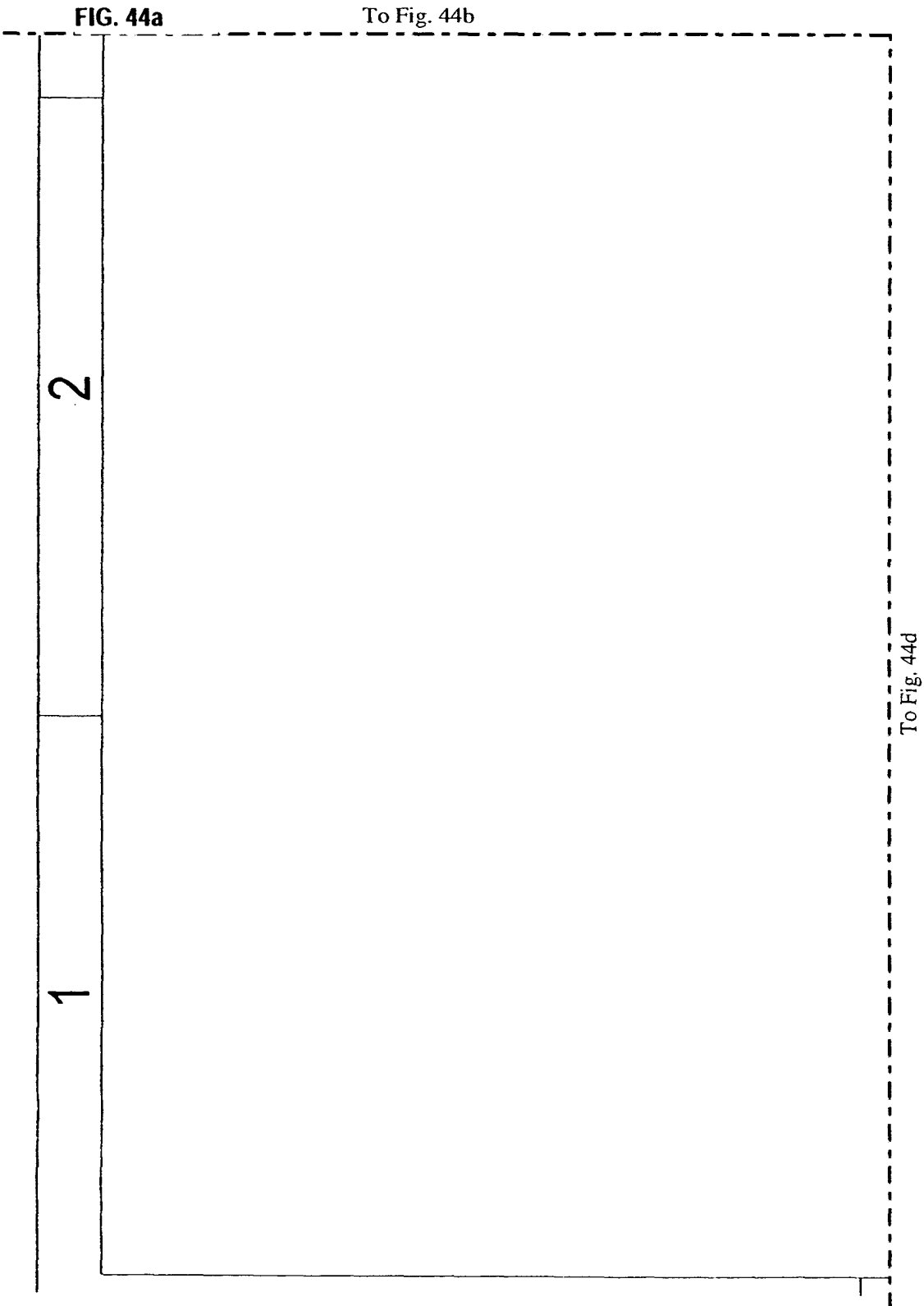


FIG. 43i





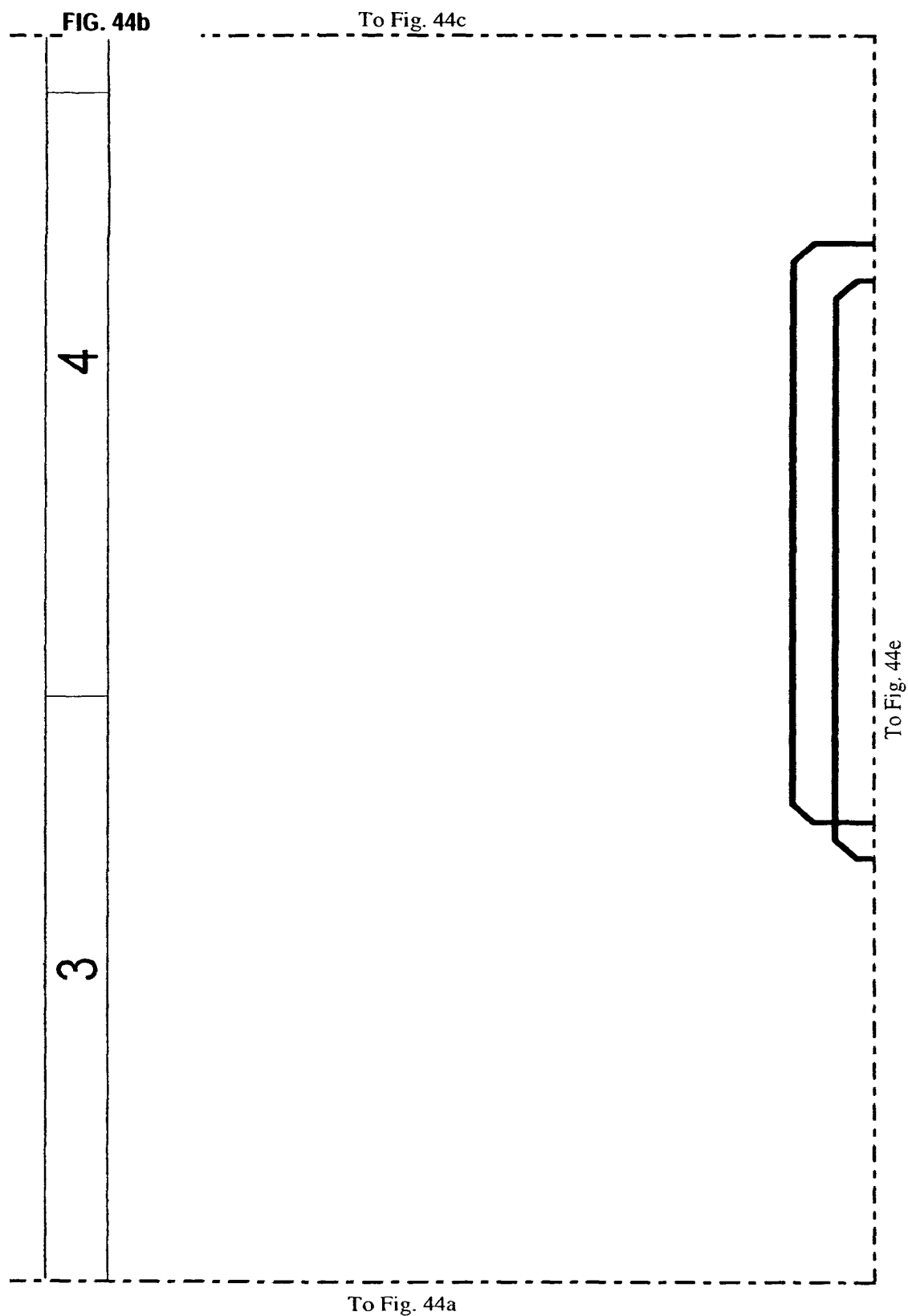


FIG. 44c

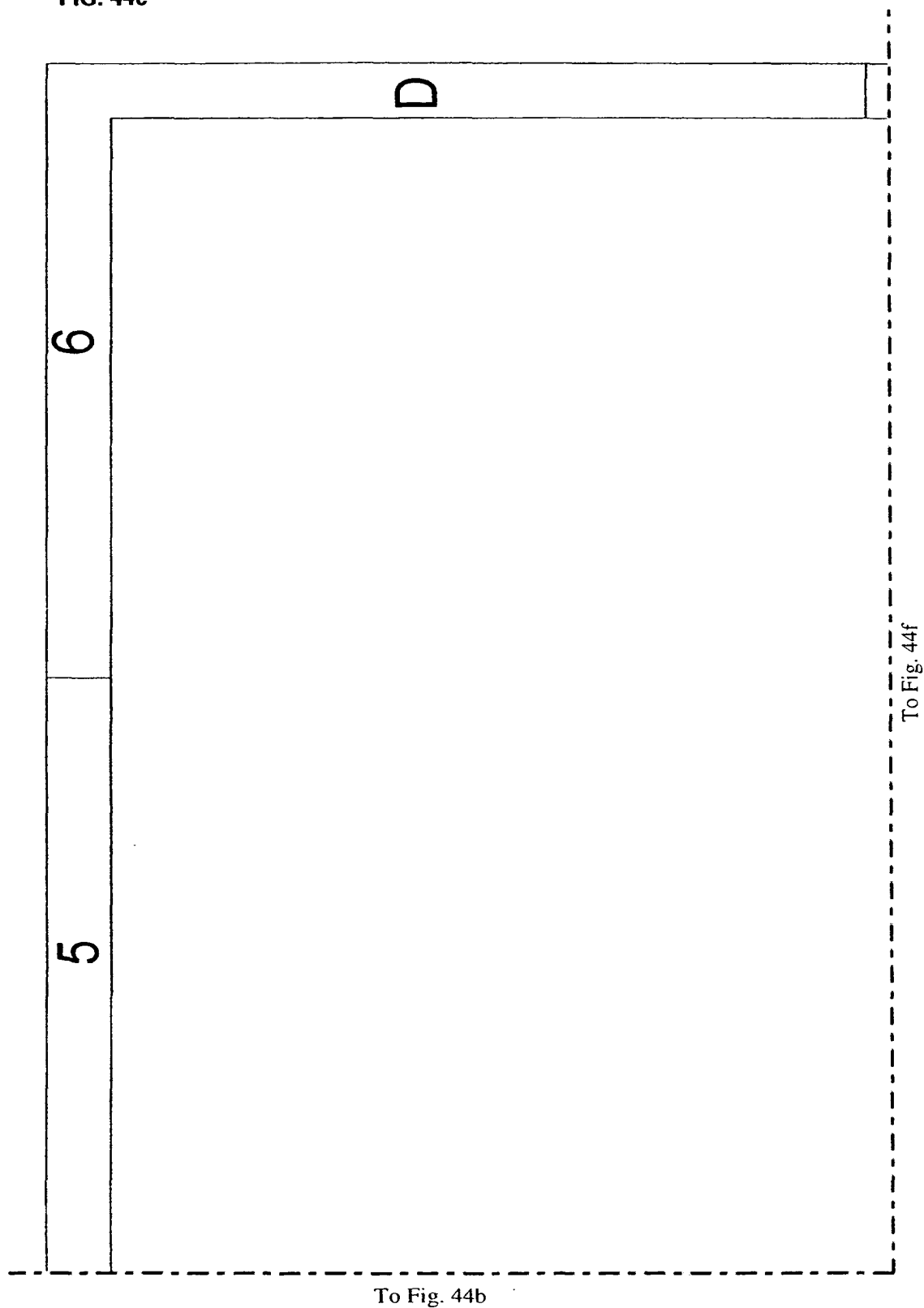


FIG. 44d

To Fig. 44e

S-053C
S-053C

To Fig. 44a

To Fig. 44g

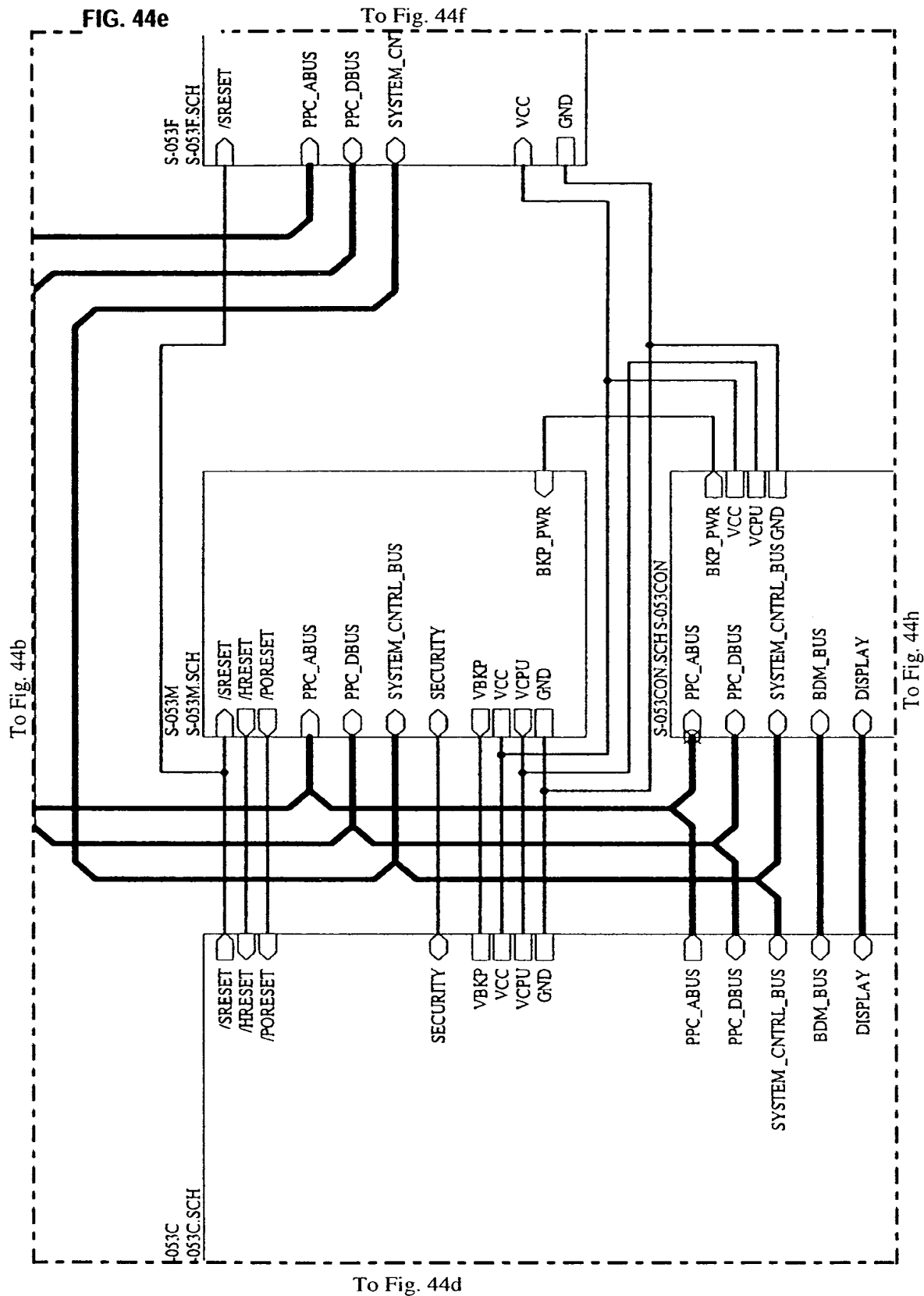
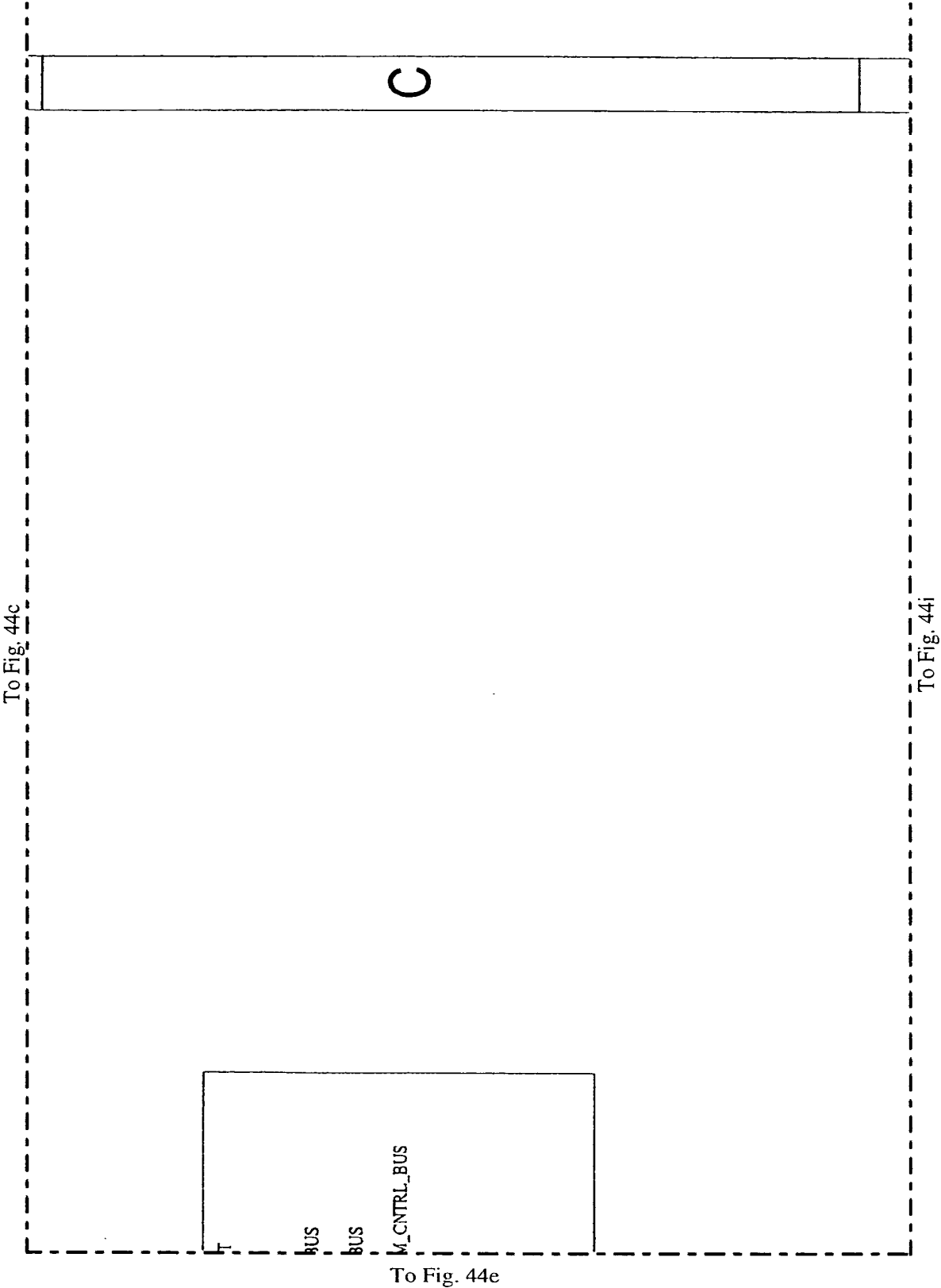
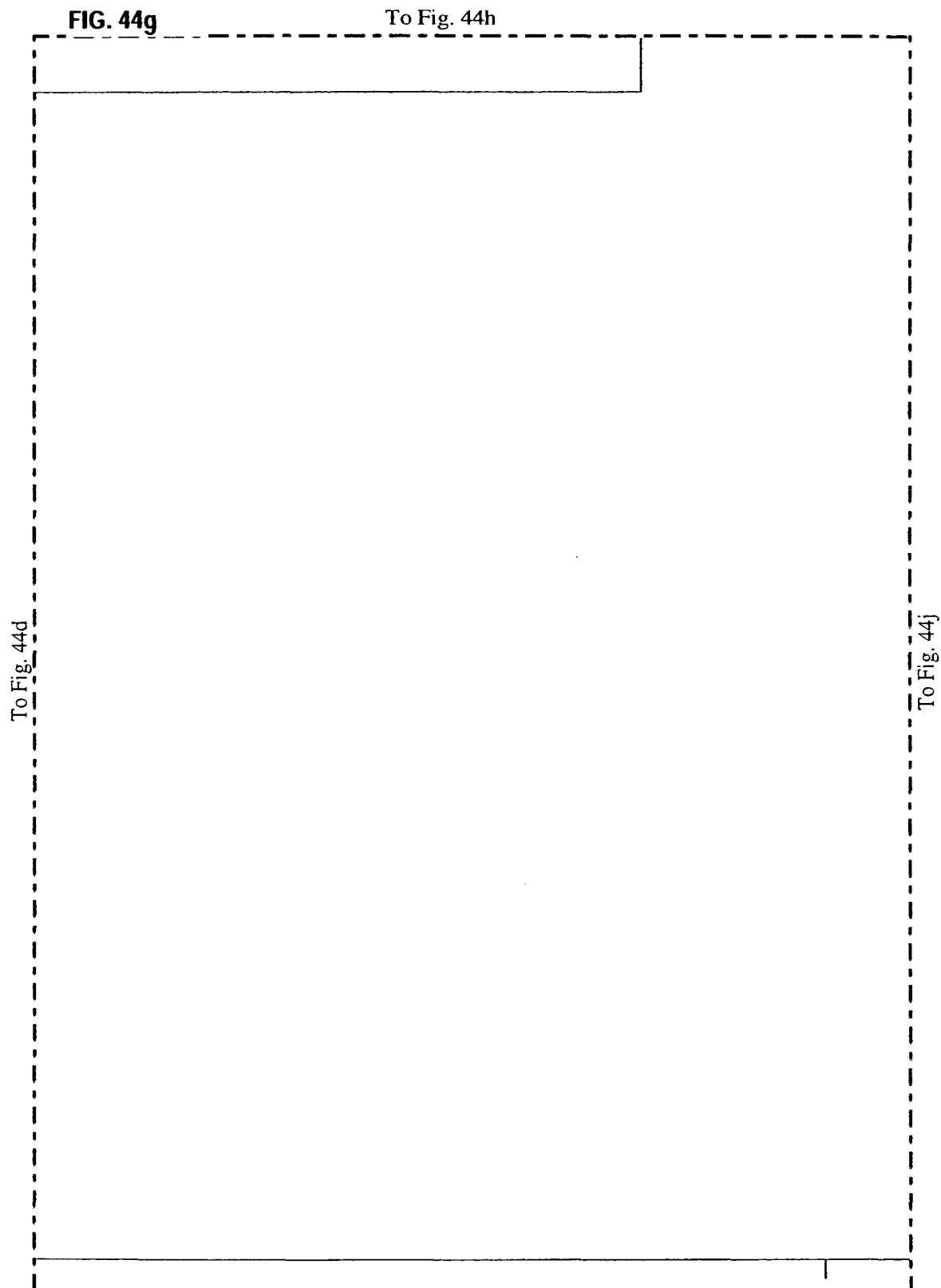


FIG. 44f





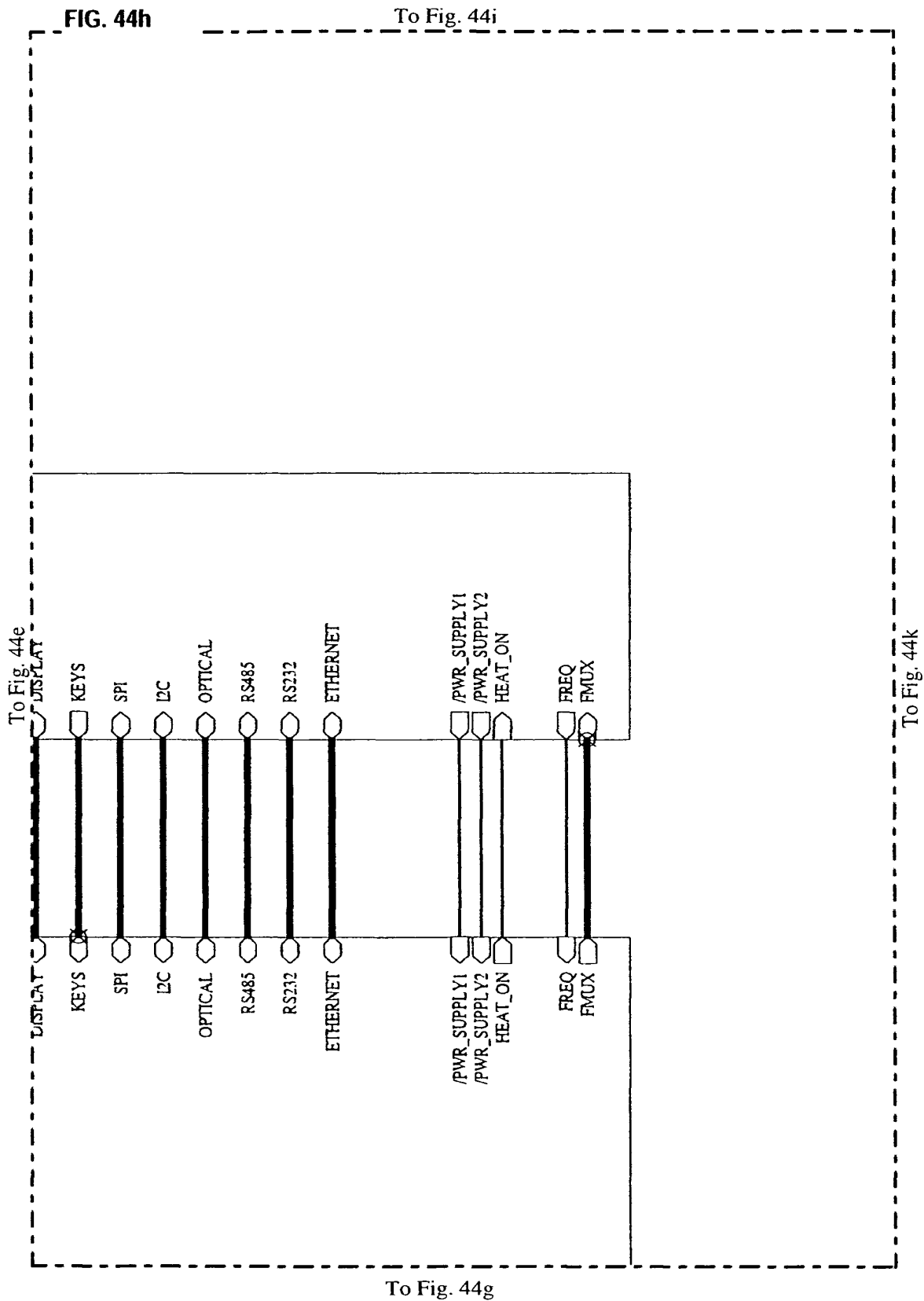


FIG. 44i

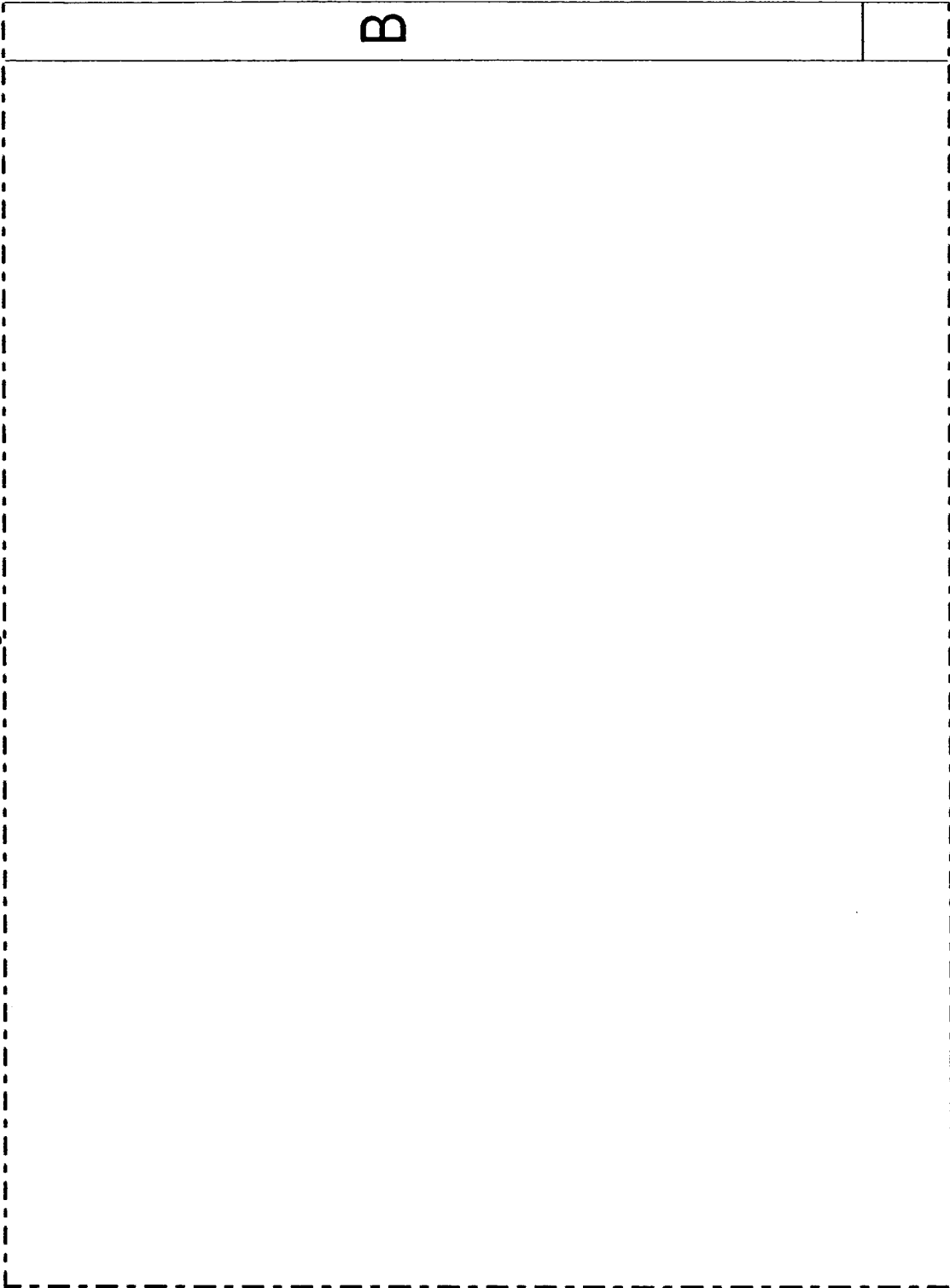


FIG. 44j

To Fig. 44k

To Fig. 44g

2

1

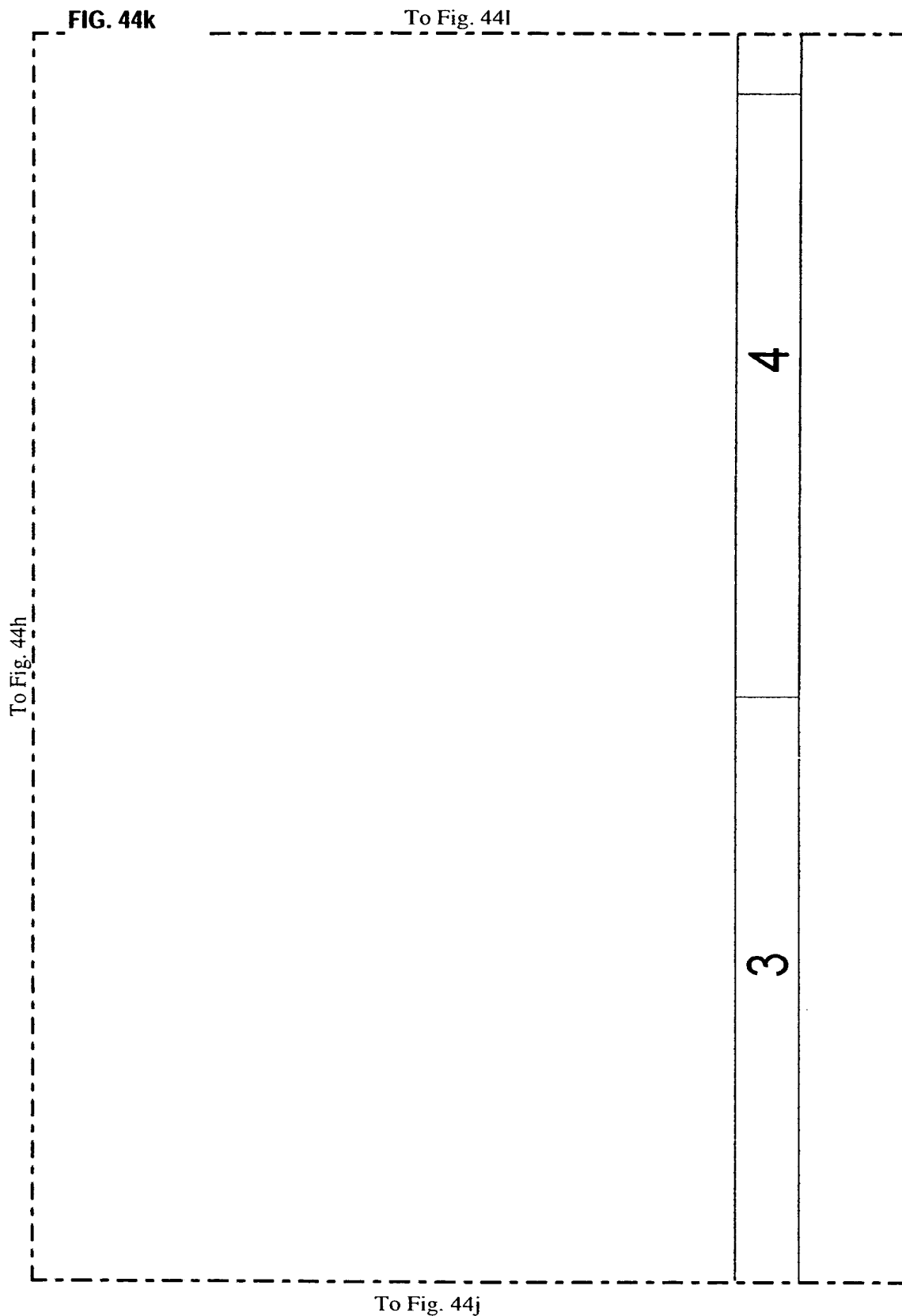
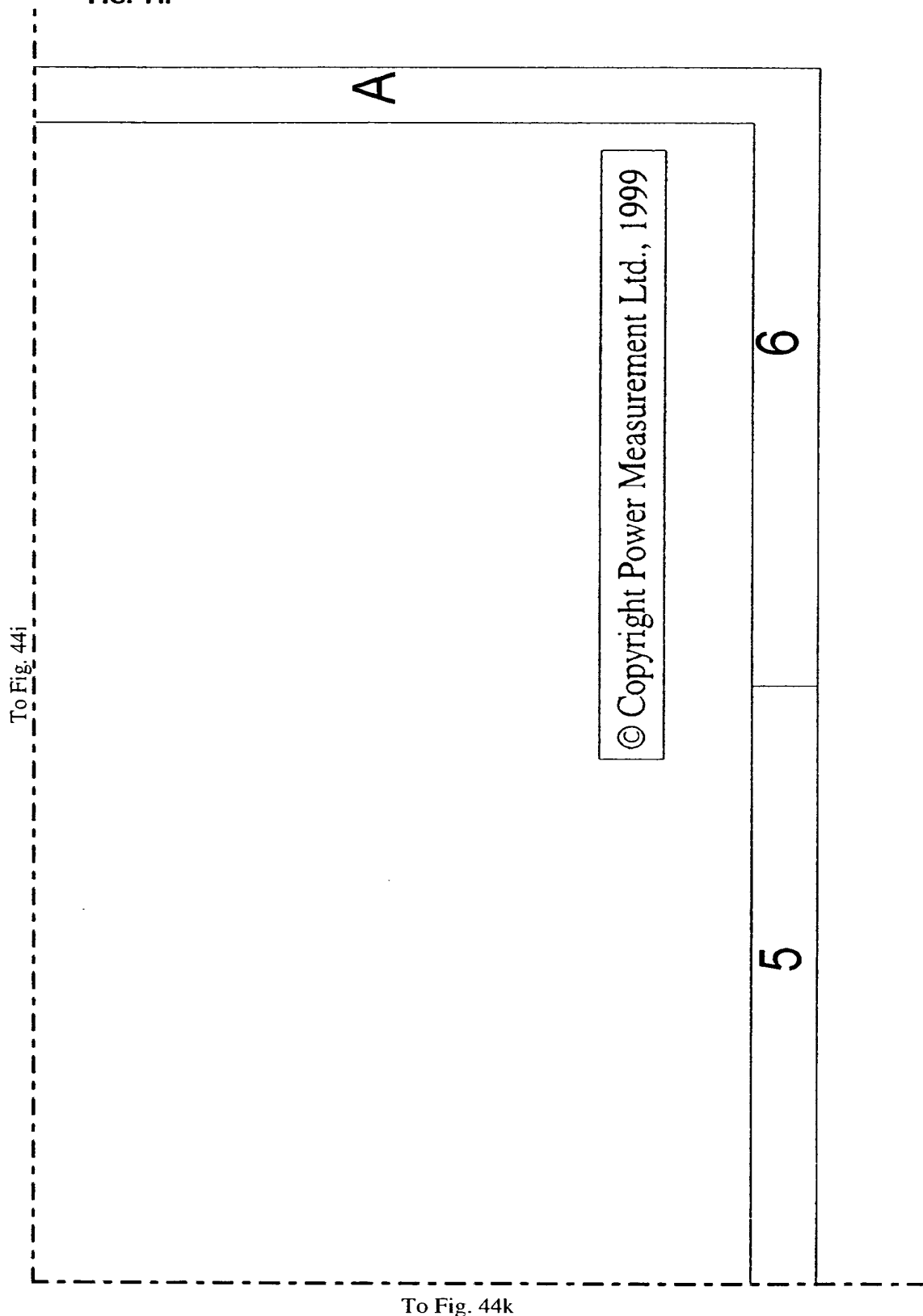
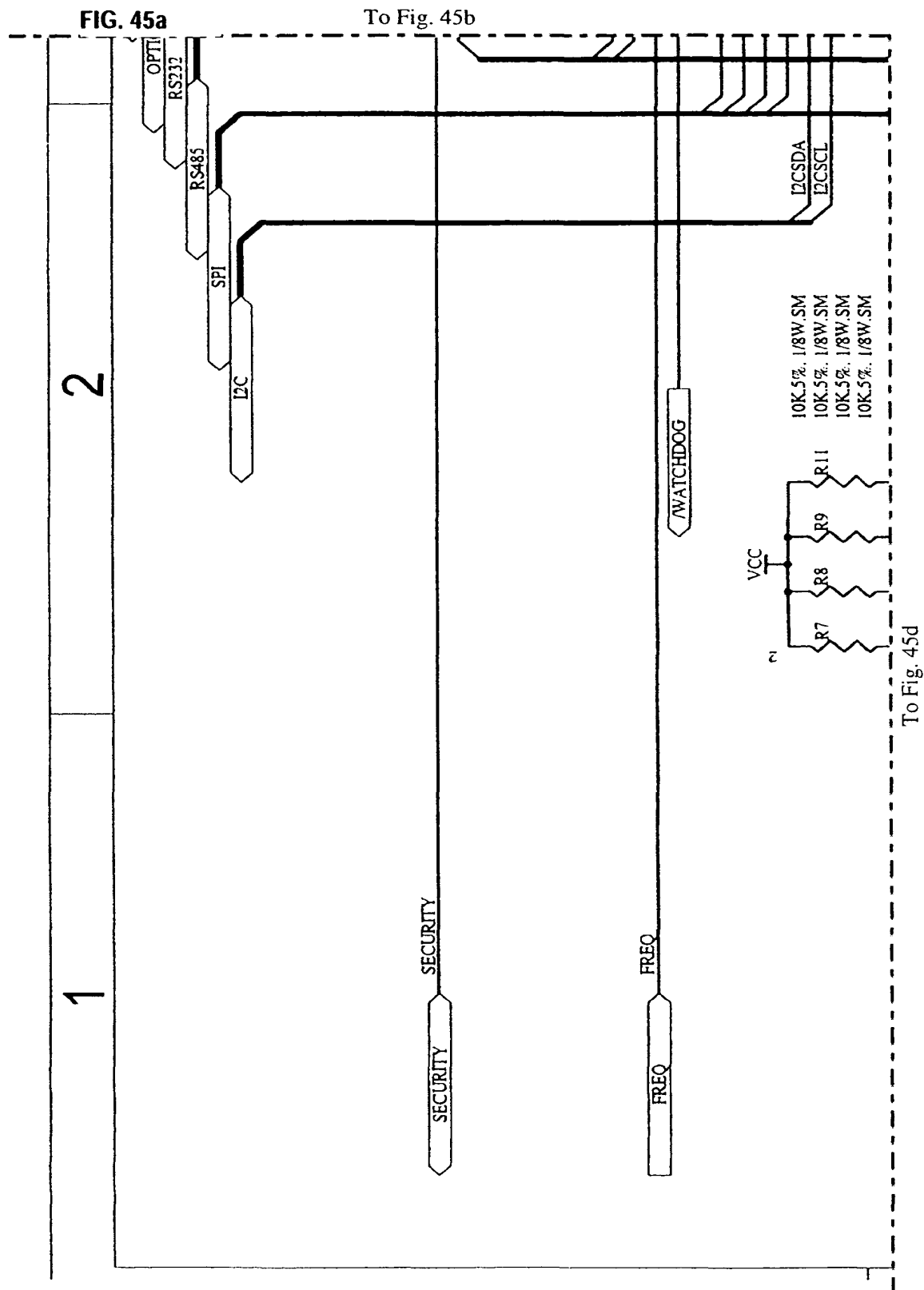
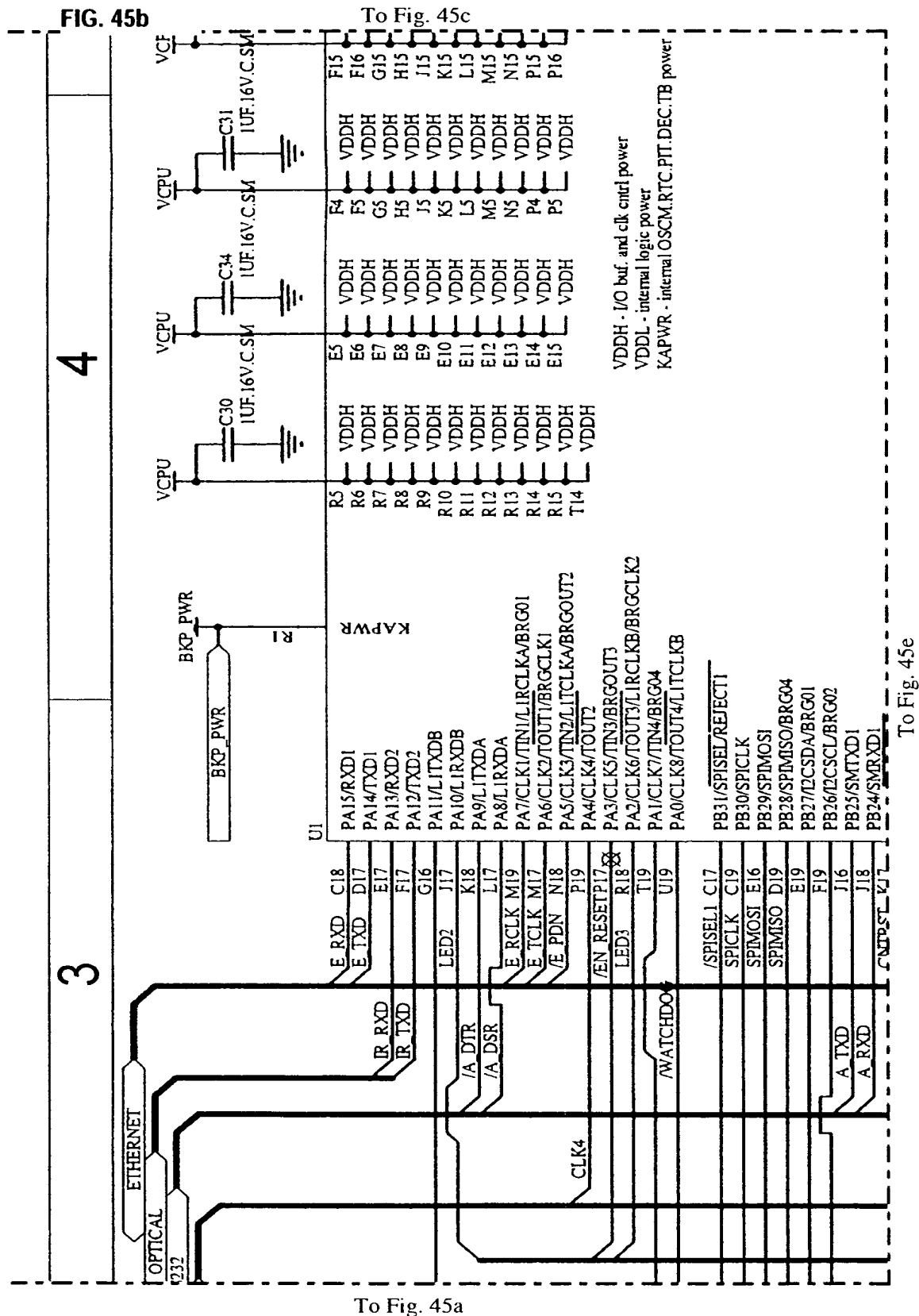


FIG. 44i

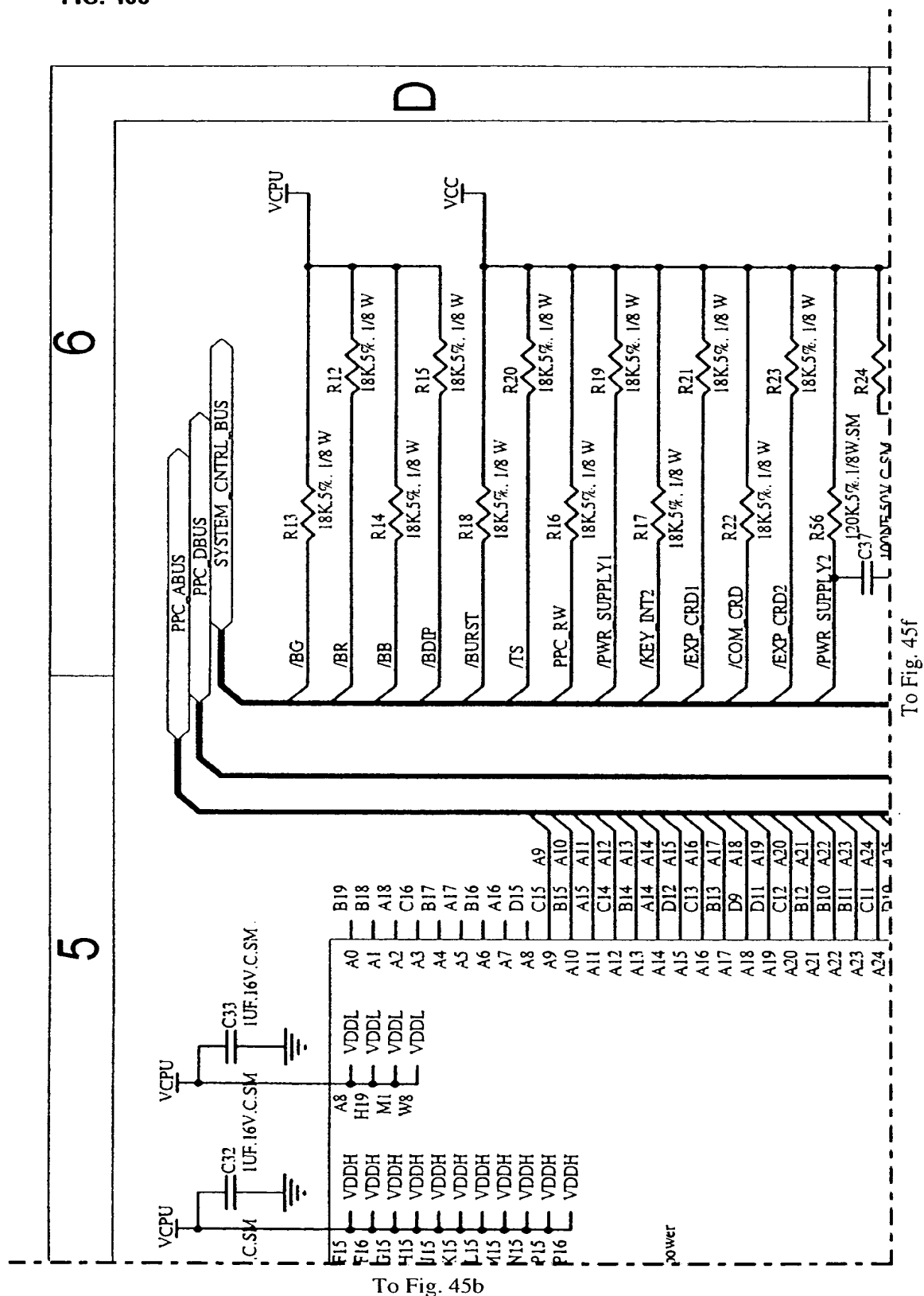






To Fig. 45e

FIG. 45c



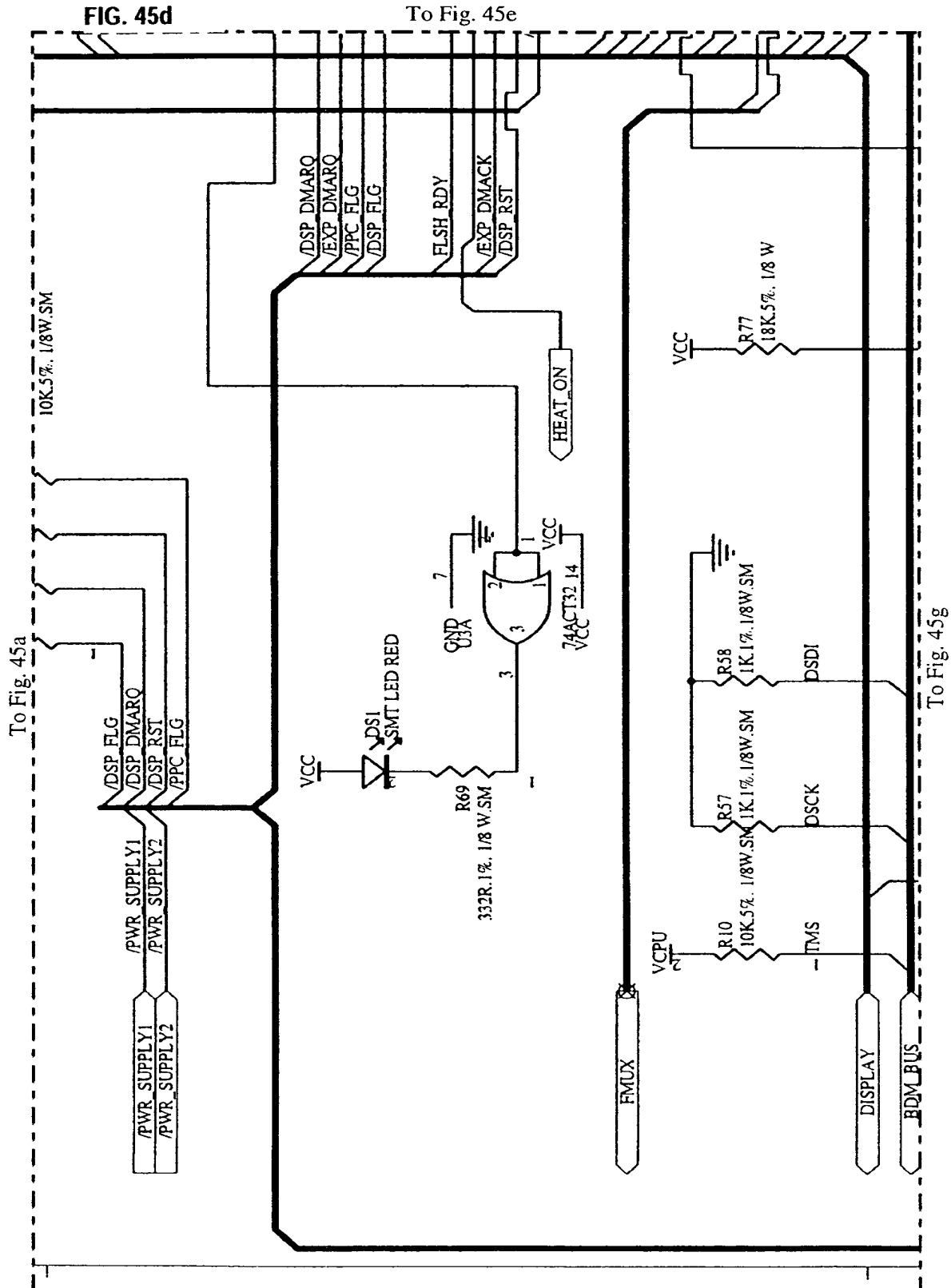


FIG. 45e

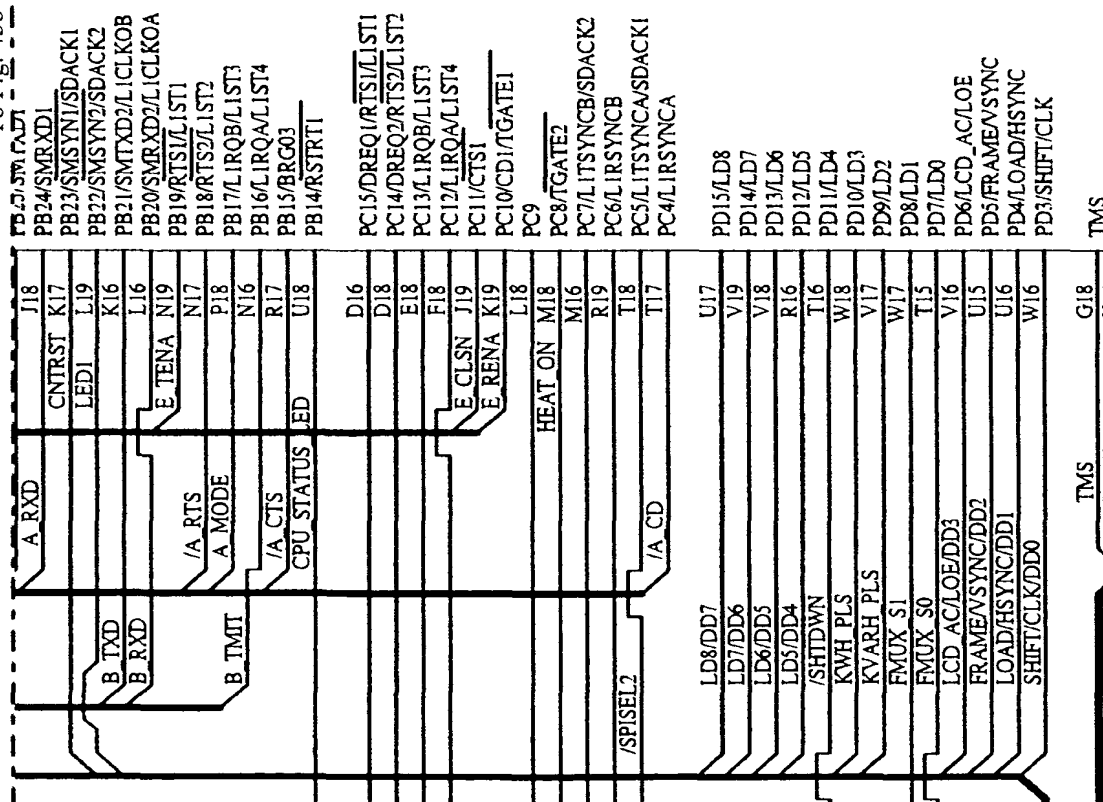
To Fig. 45f

MPC821BGA

D6 — N/C
D13 — N/C
D14 — N/C
U2 — N/C
V2 — N/C

F6 — GND
F7 — GND
F8 — GND
F9 — GND
F10 — GND
F11 — GND
F12 — GND
F13 — GND
F14 — GND
C6 — GND
G7 — GND
C8 — GND
C9 — GND
G10 — GND
G11 — GND
G12 — GND
G13 — GND
G14 — GND
H6 — GND
H7 — GND
H8 — GND
H9 — GND
H10 — GND

To Fig. 45b



To Fig. 45d

To Fig. 45h

FIG. 45f

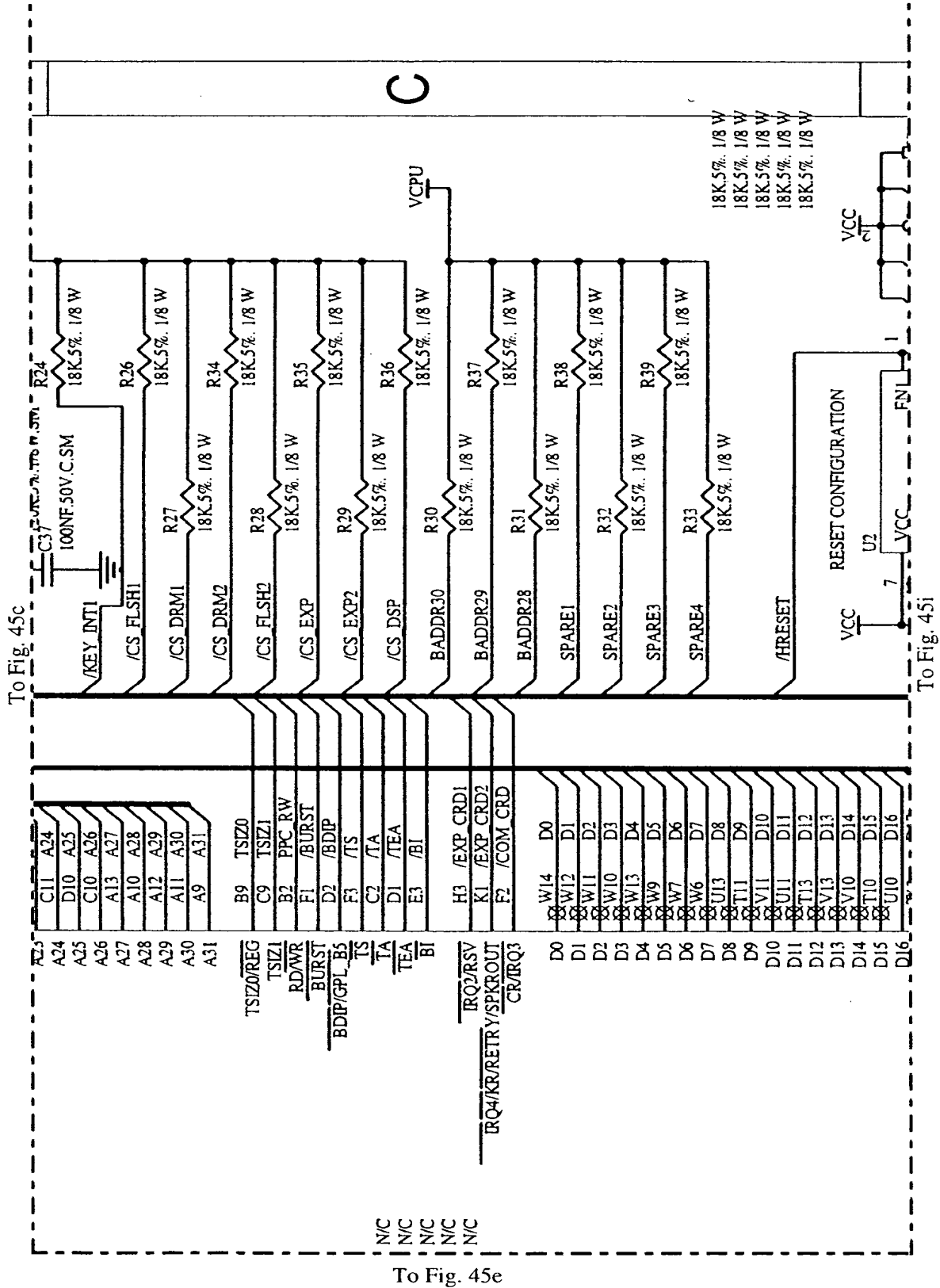
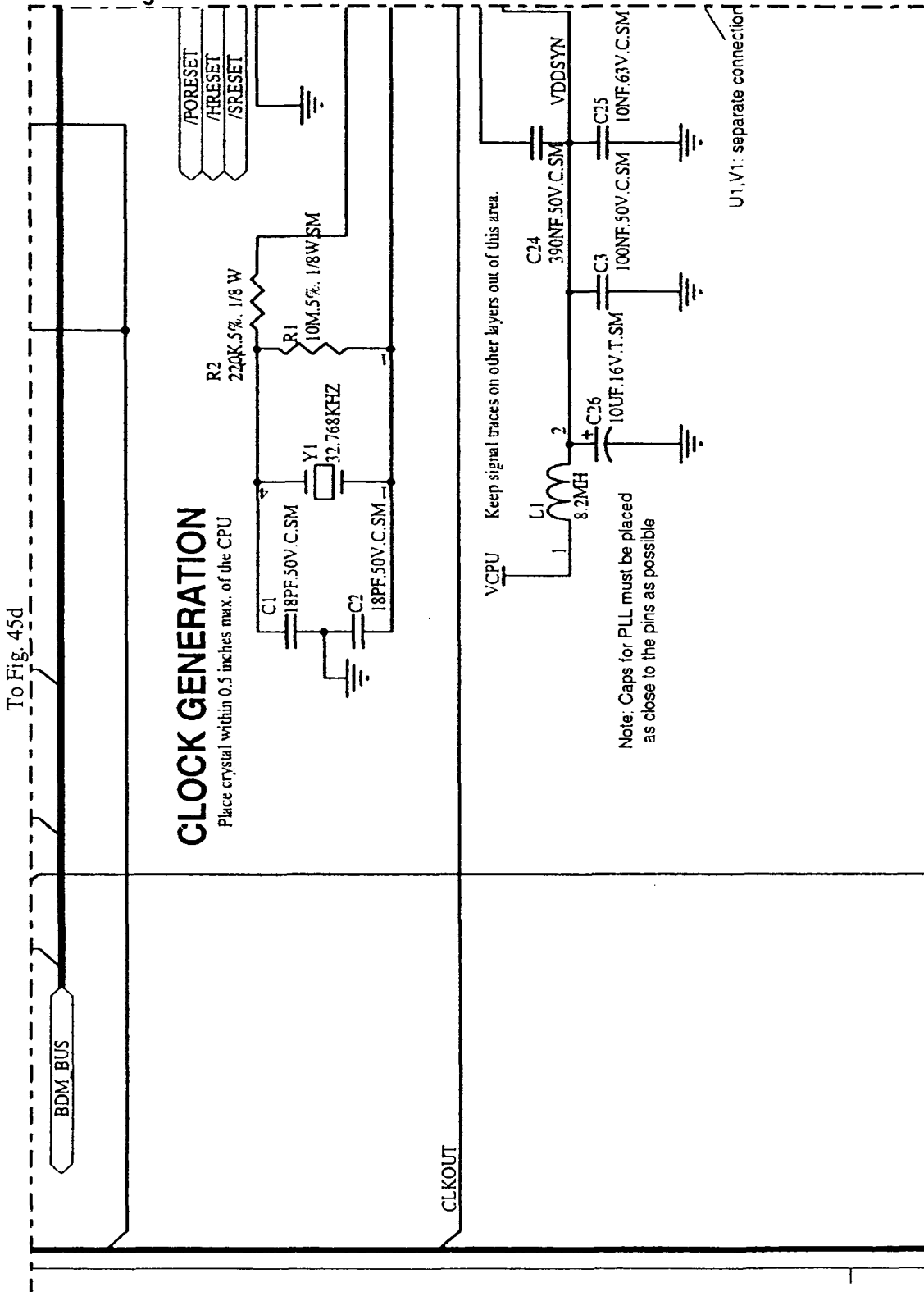
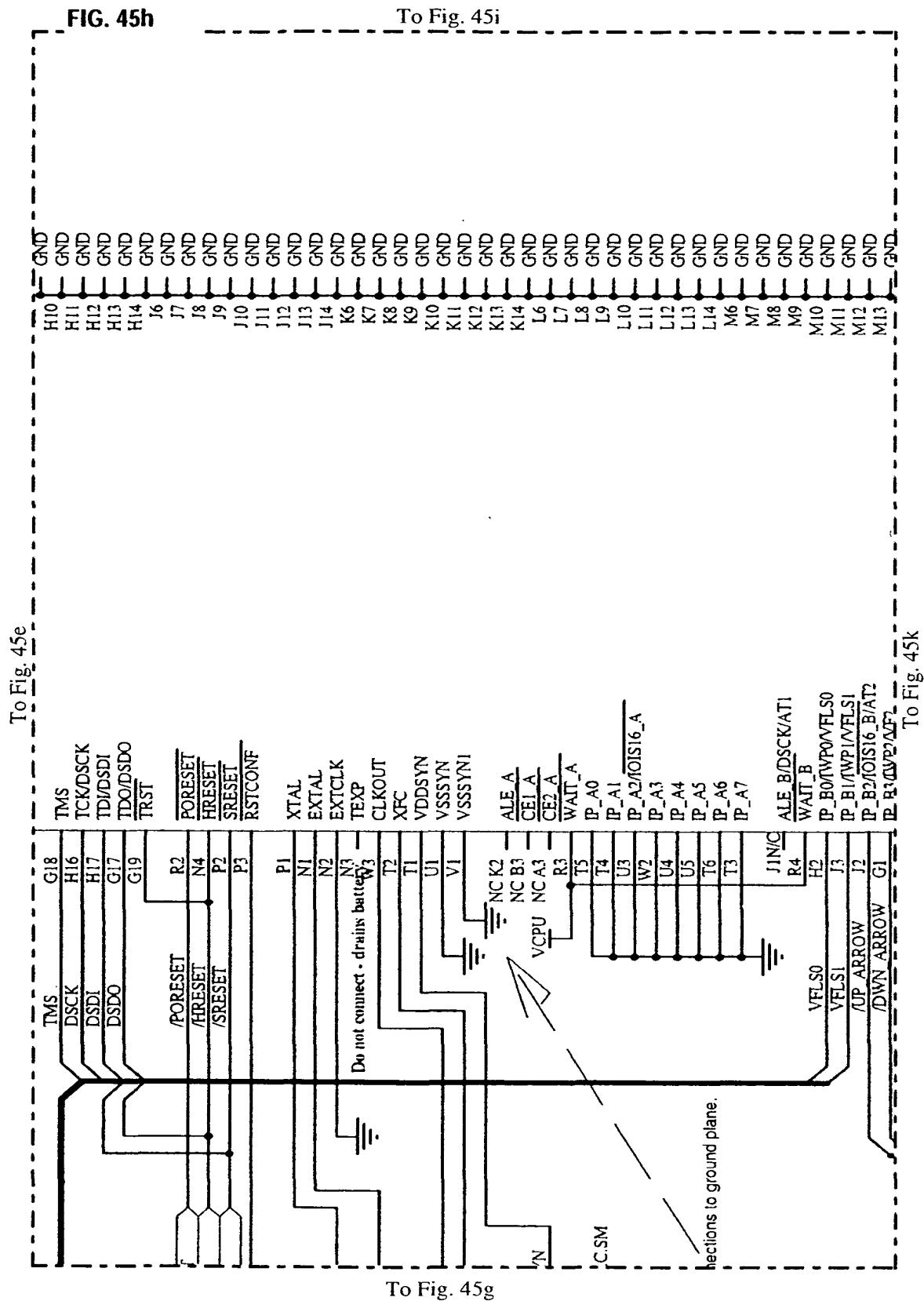


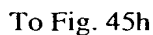
FIG. 45g

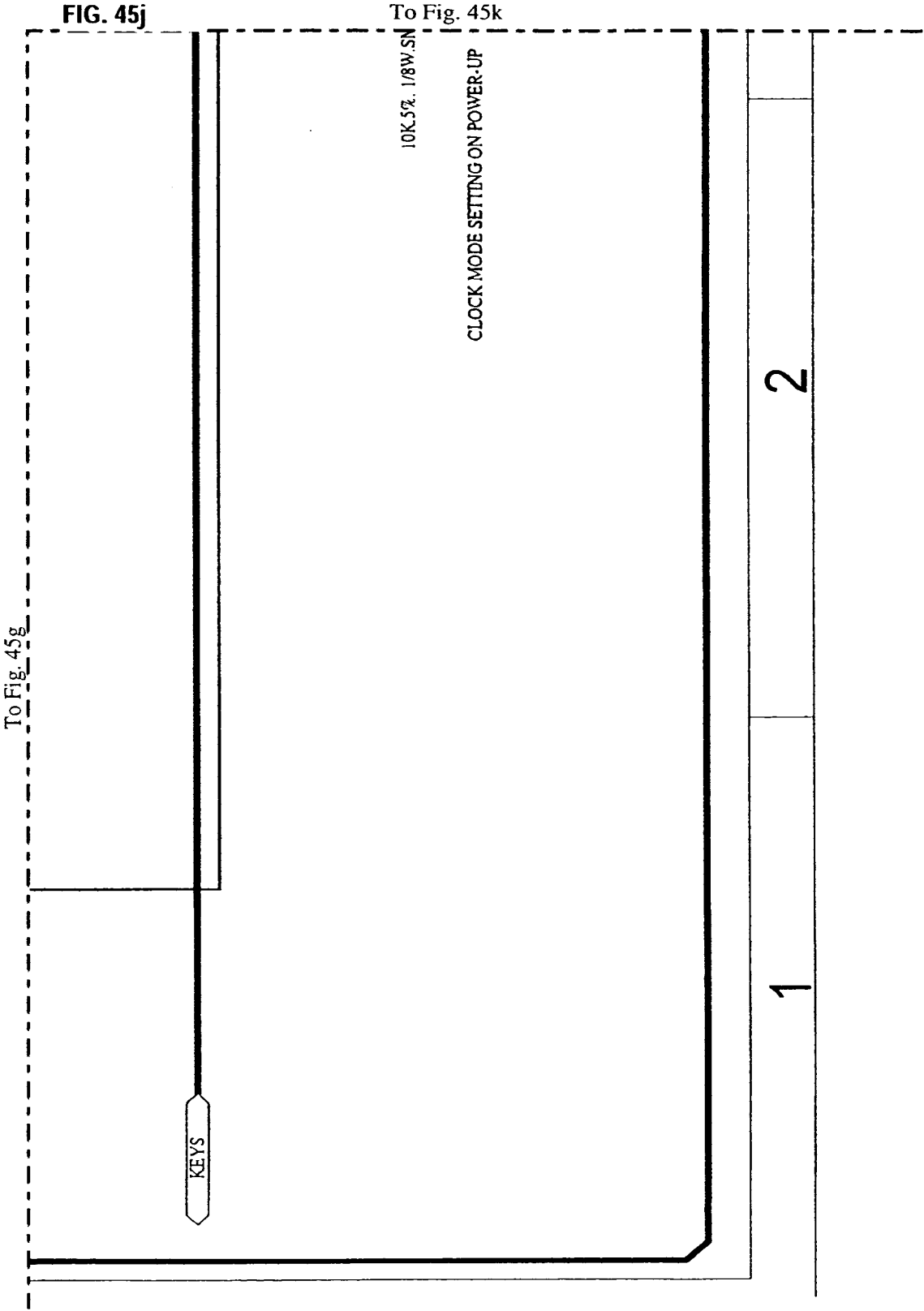
To Fig. 45h



To Fig. 45j







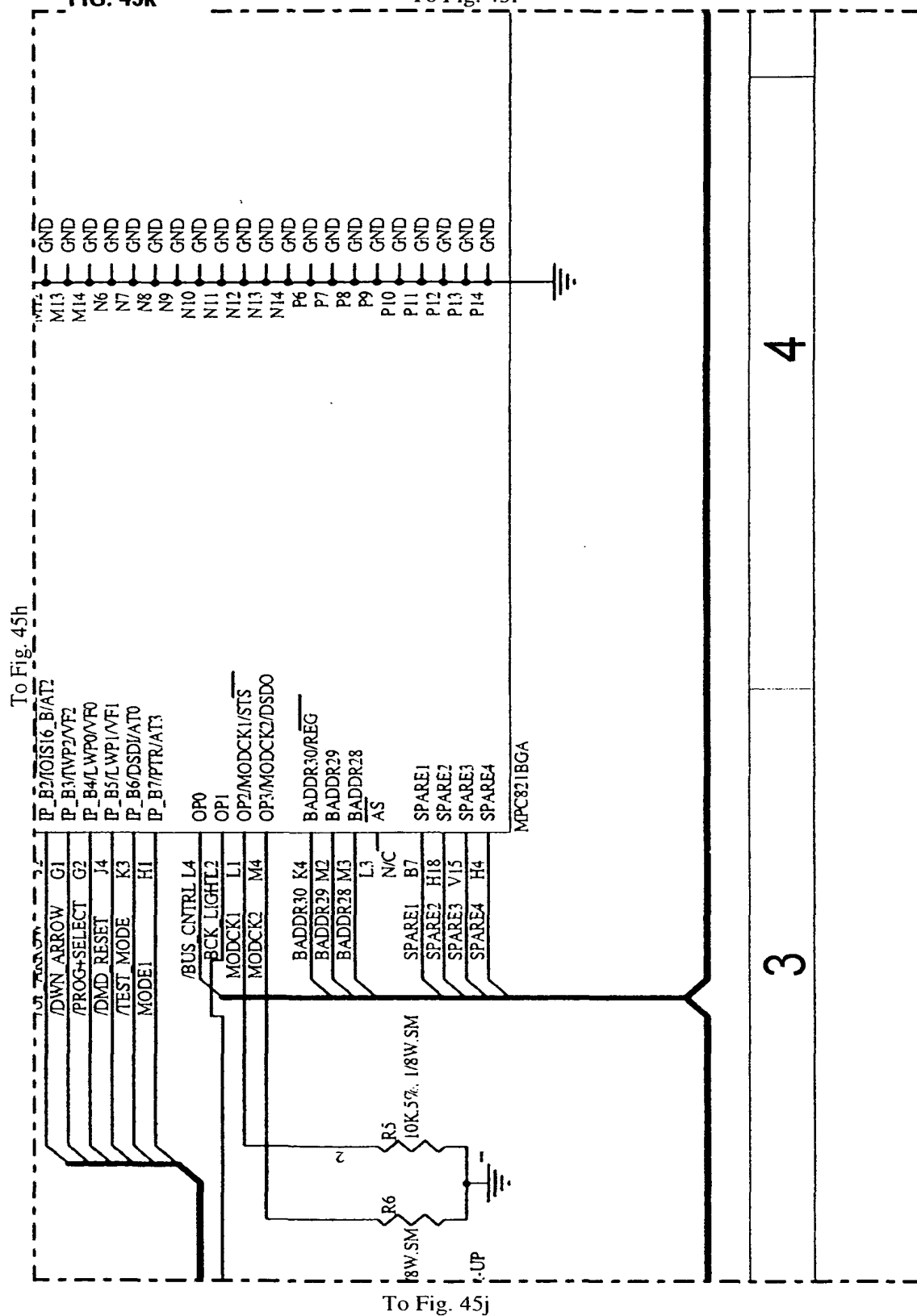


FIG. 45I

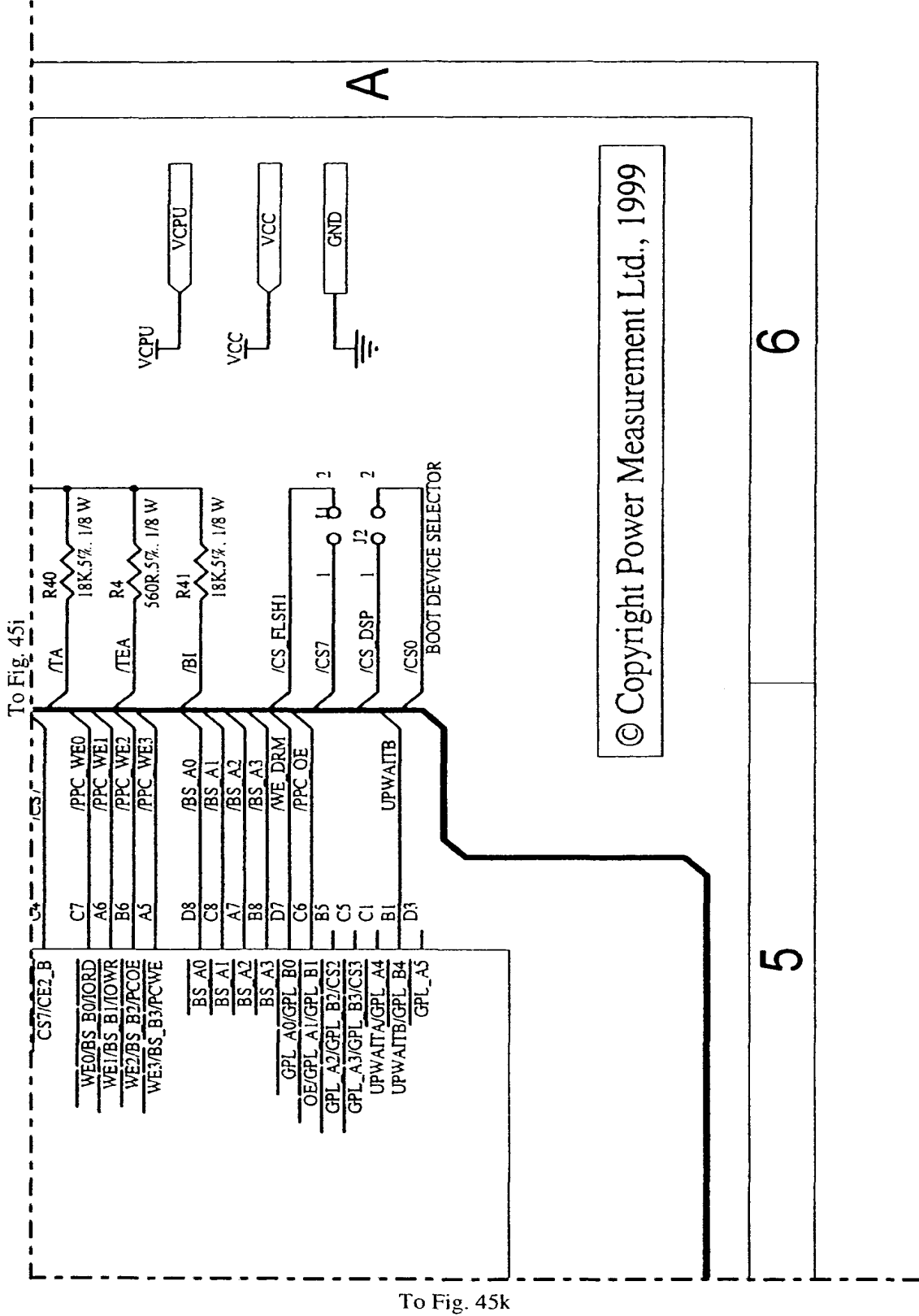
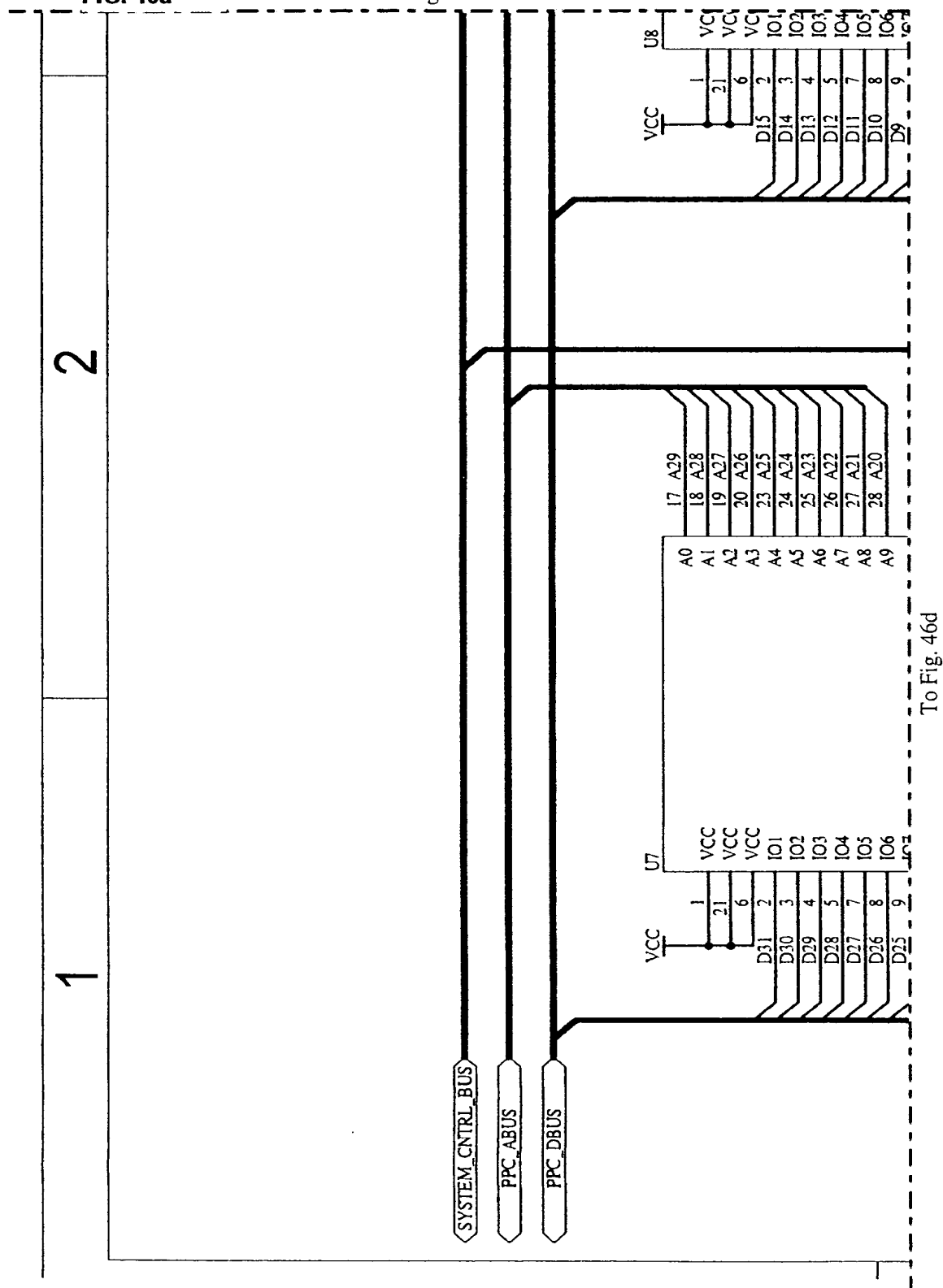


FIG. 46a

To Fig. 46b



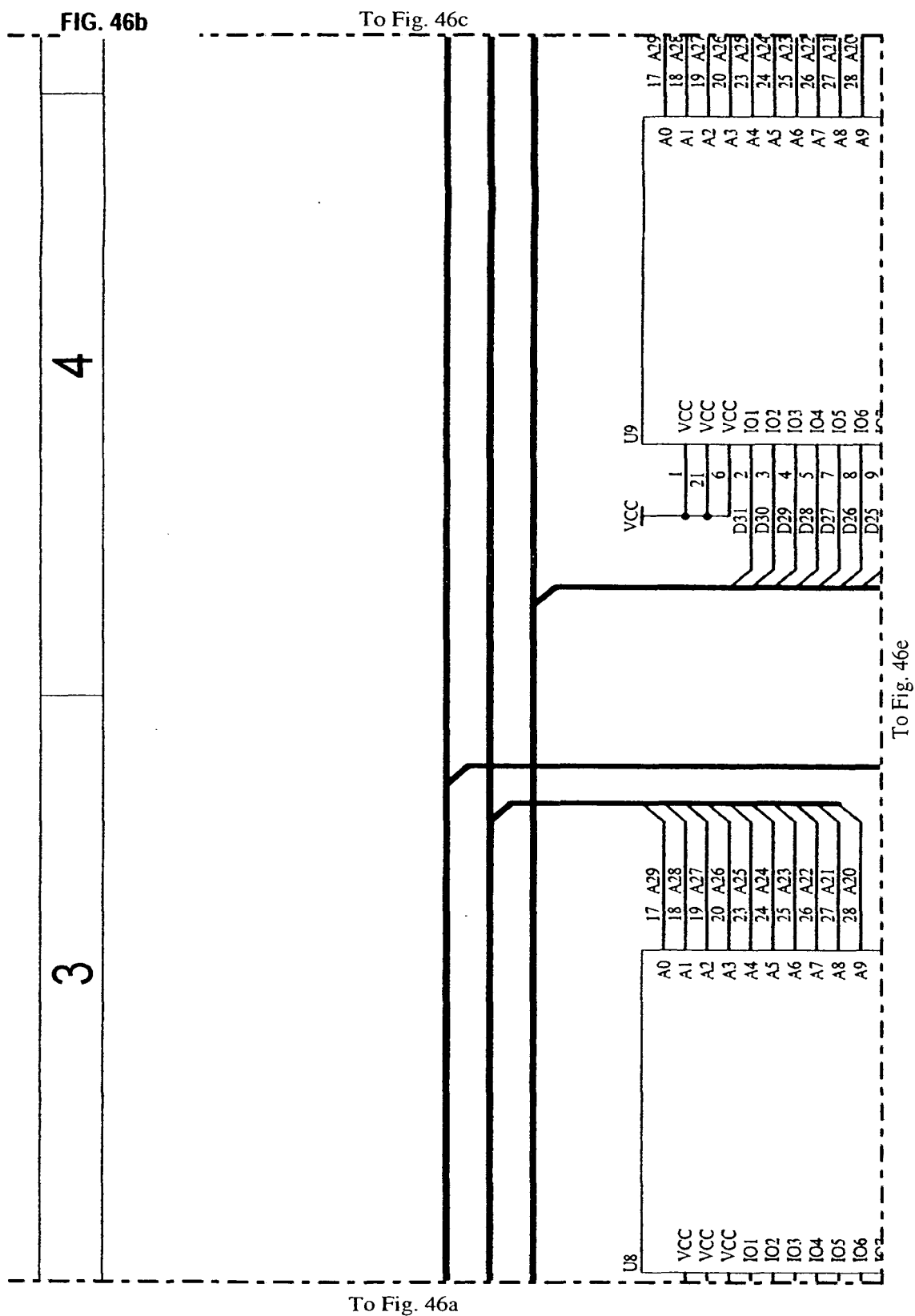


FIG. 46c

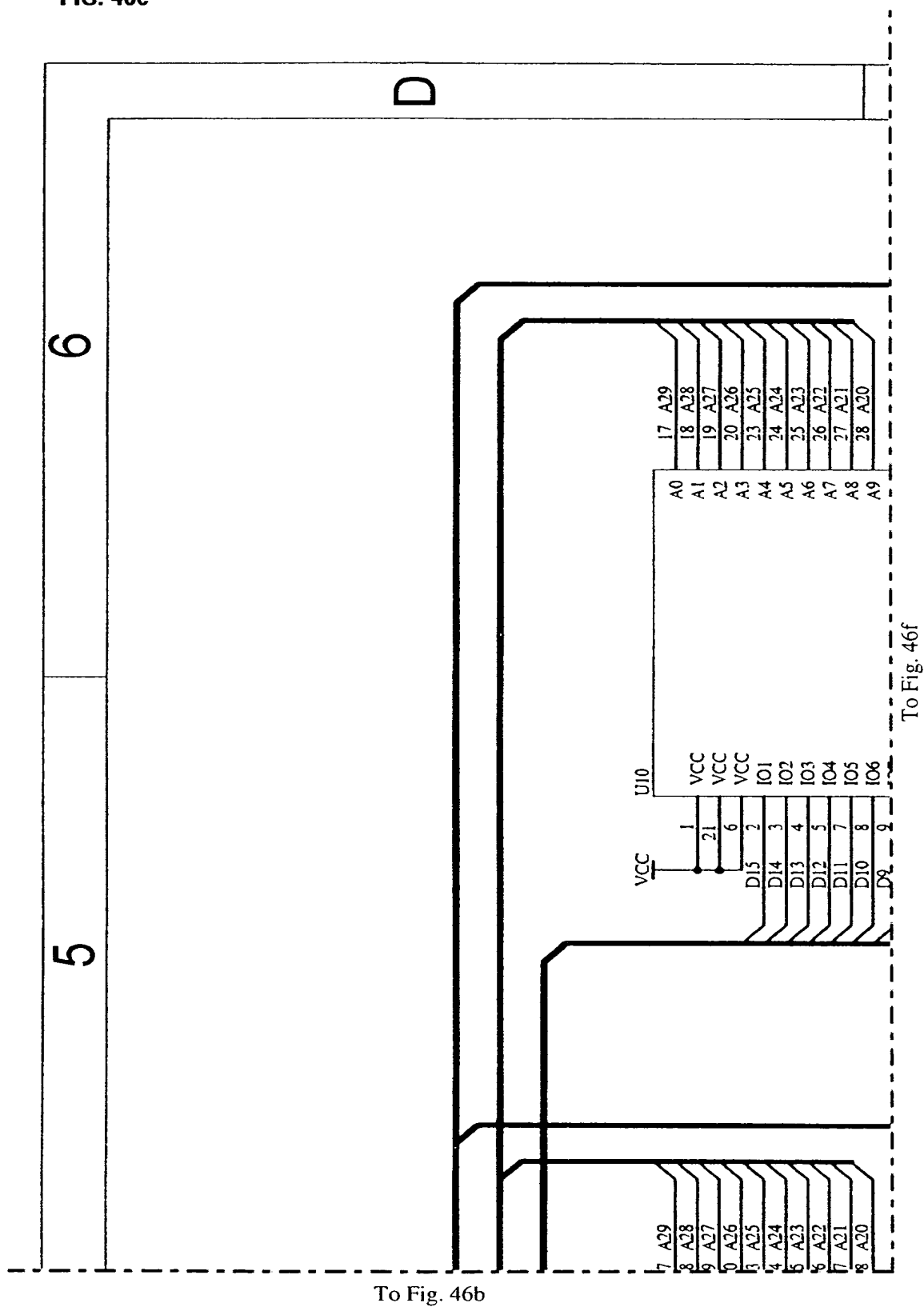
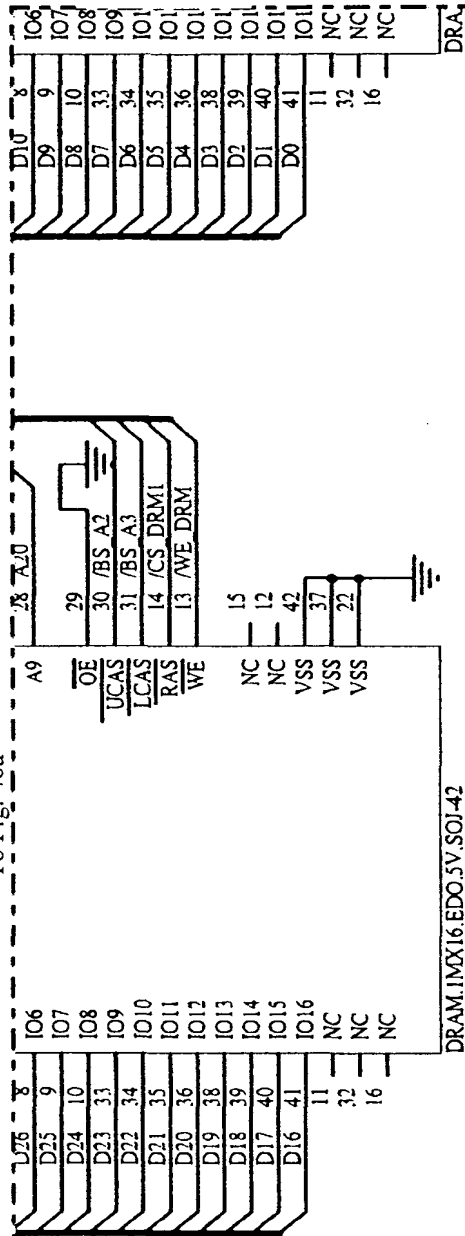


FIG. 46d



To Fig. 46e



Bypass caps. One per power pin

DRAM BANK 1 (MAX 4MB)

To Fig. 46g

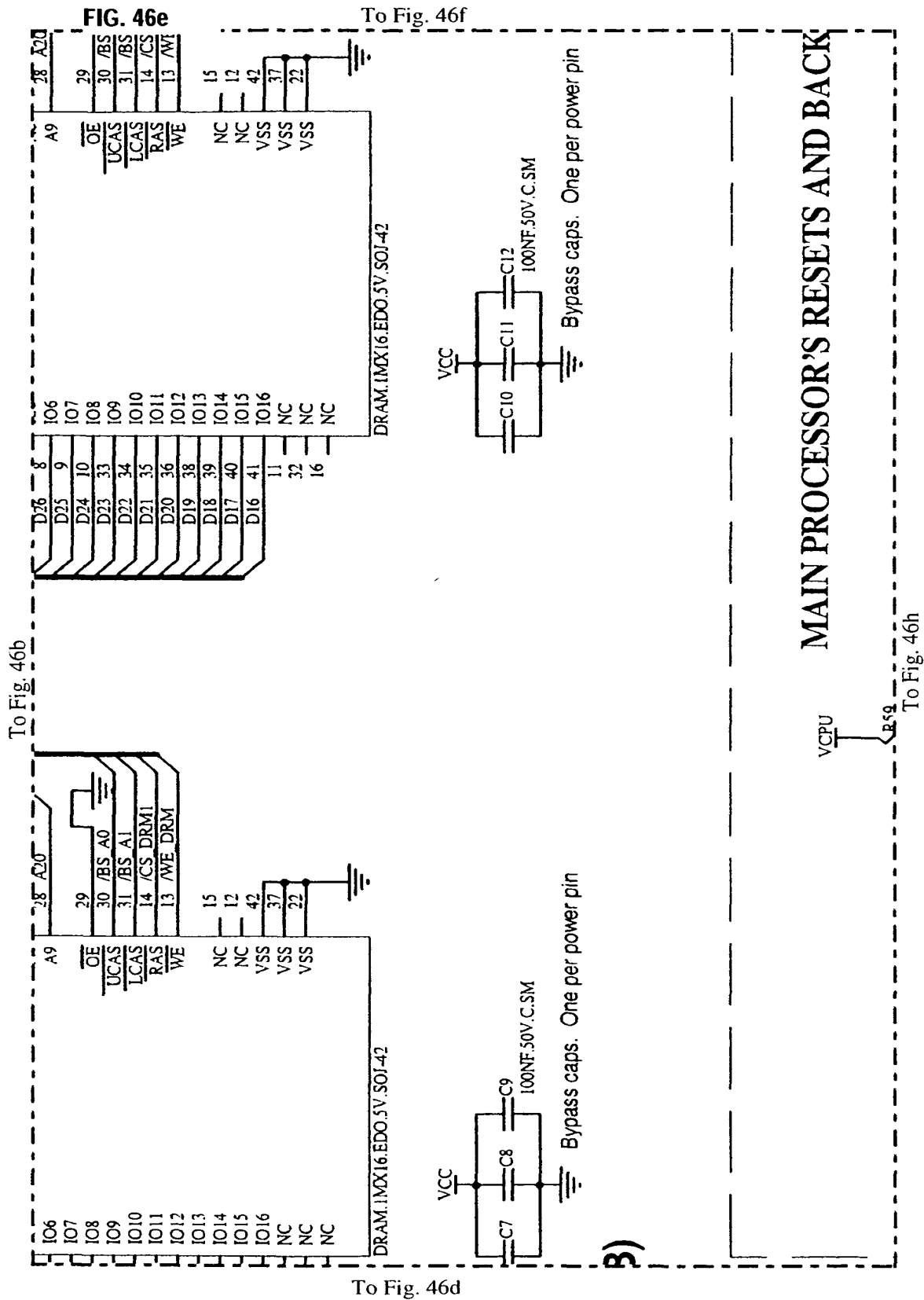


FIG. 46f

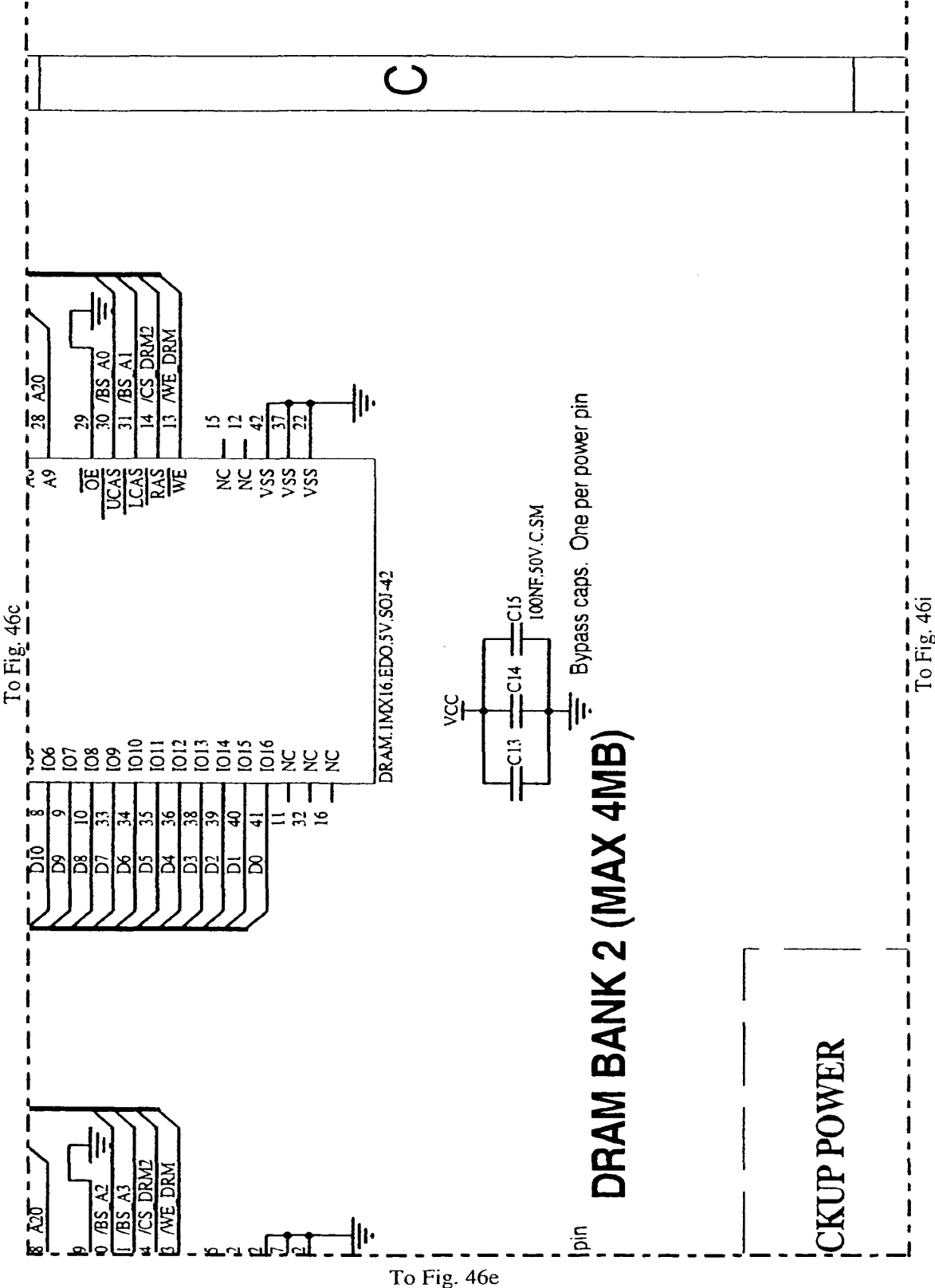
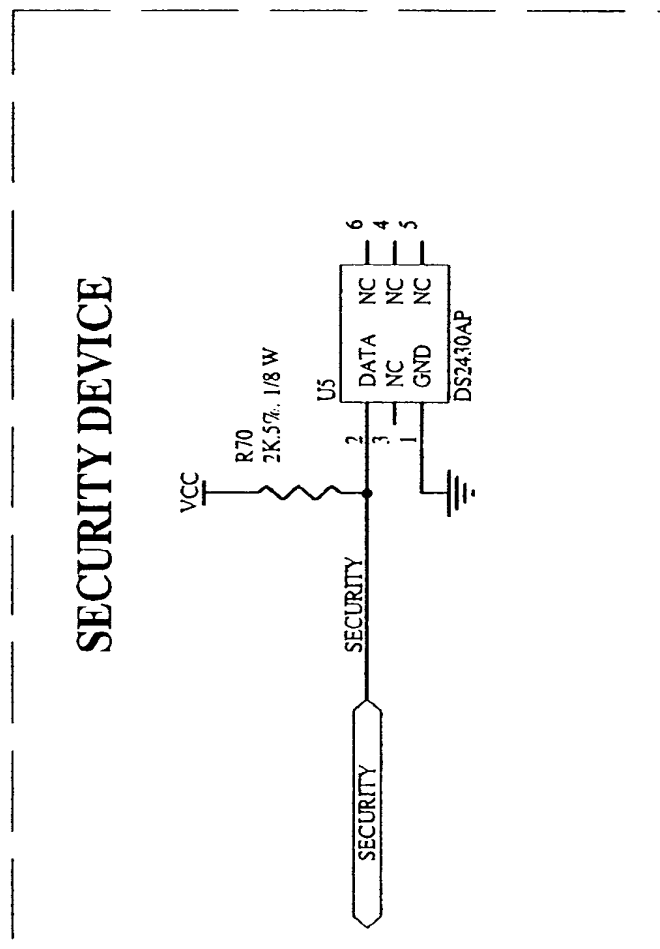


FIG. 46g

To Fig. 46h



To Fig. 46d

To Fig. 46j

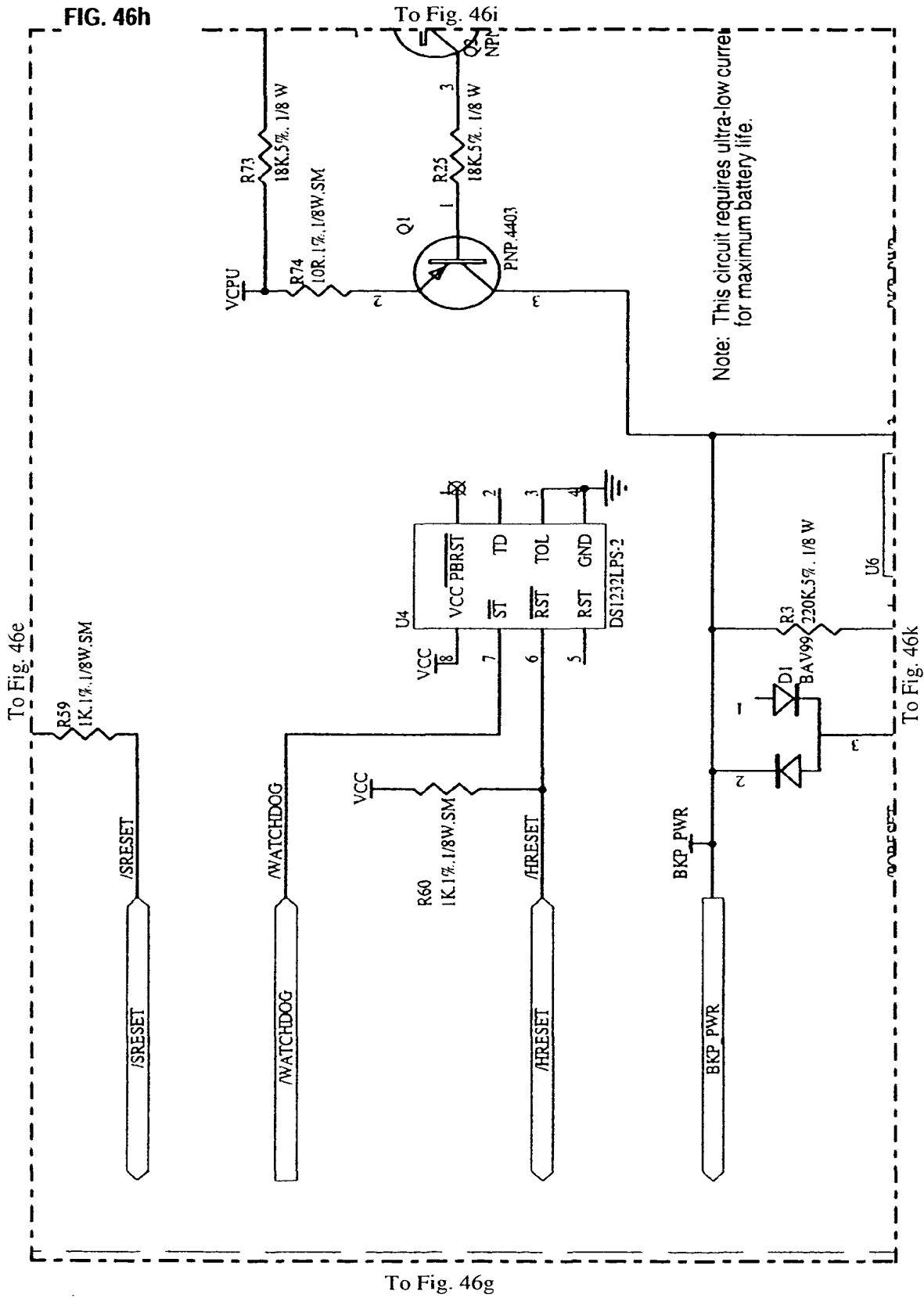


FIG. 46i

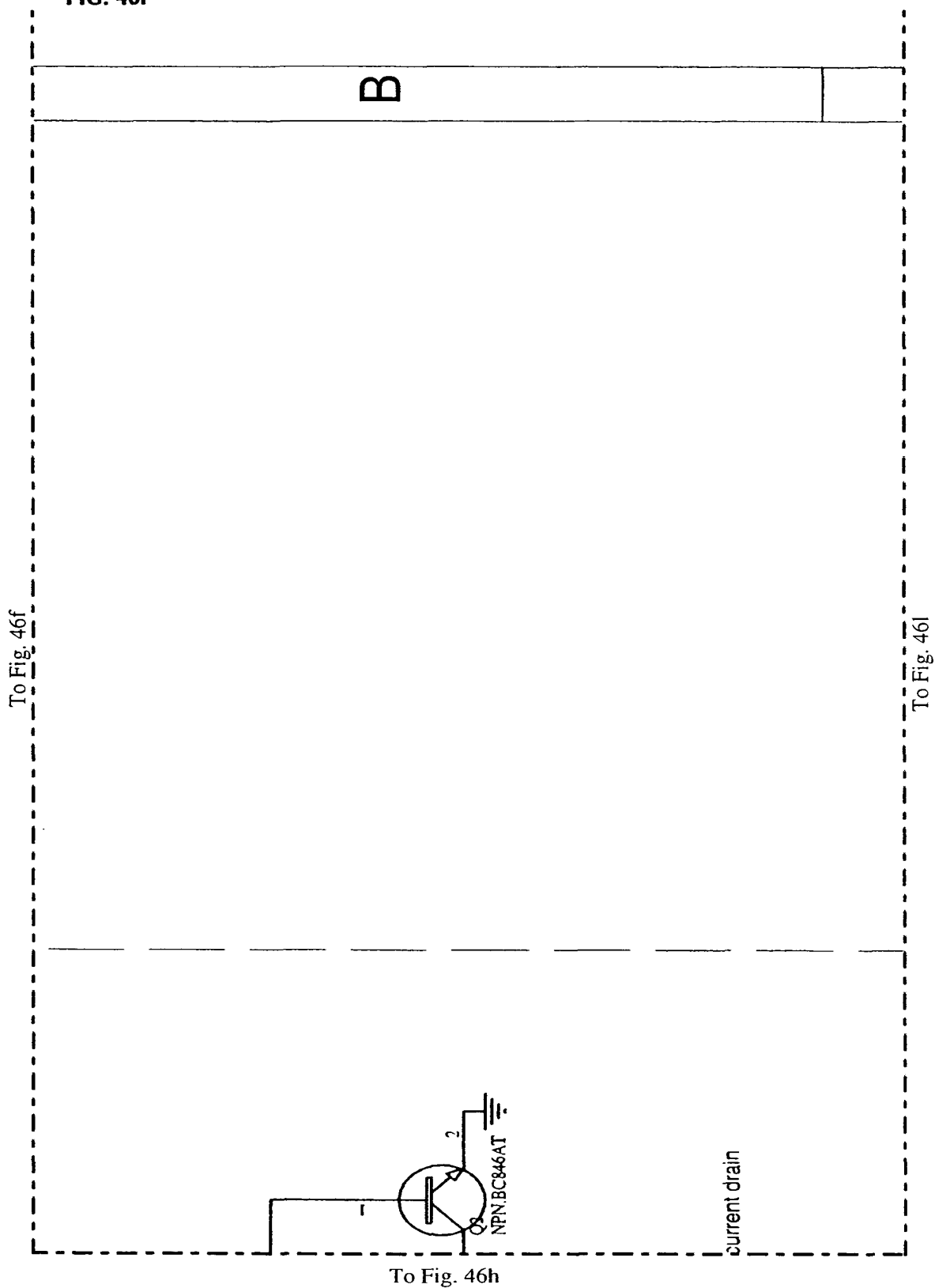
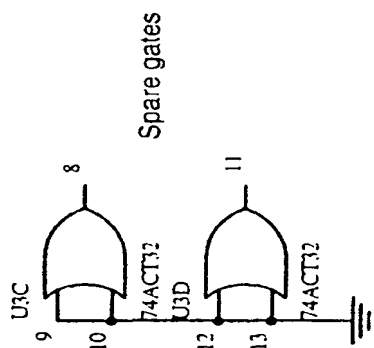


FIG. 46j

To Fig. 46k

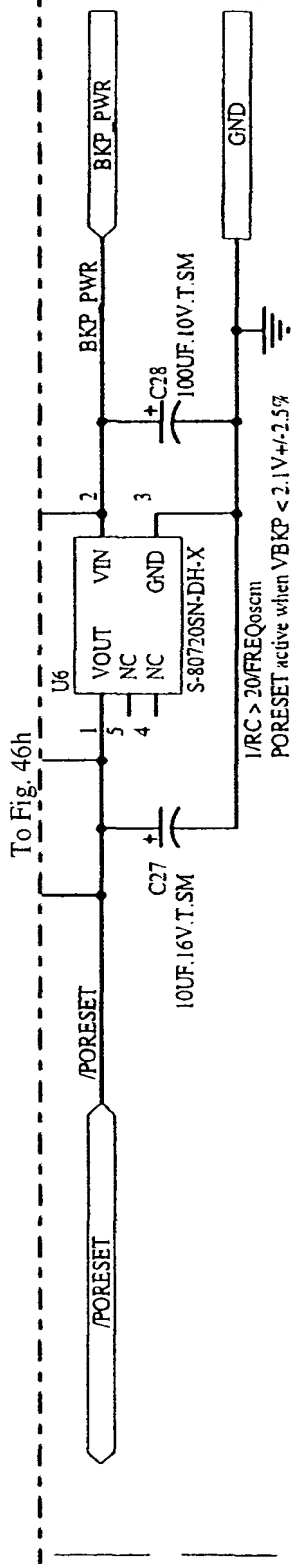
To Fig. 46g



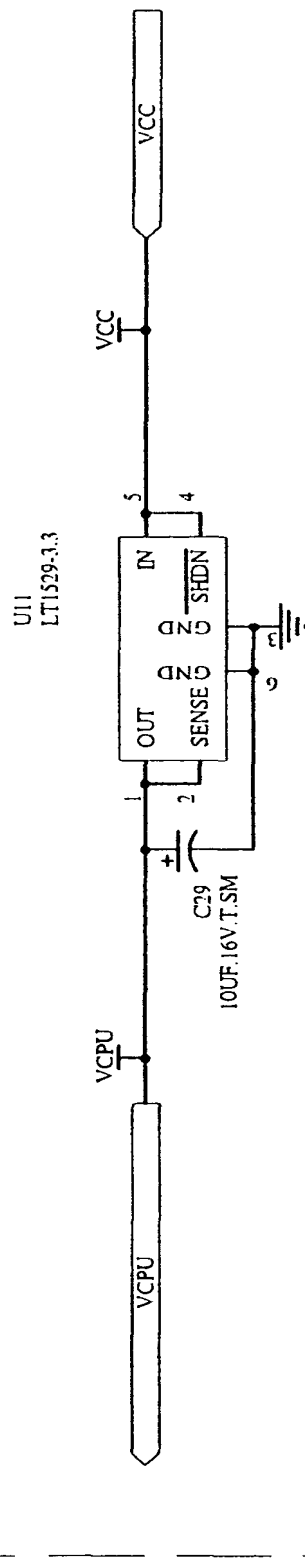
2

1

FIG. 46k



To Fig. 46l



To Fig. 46j

4

3

FIG. 46i

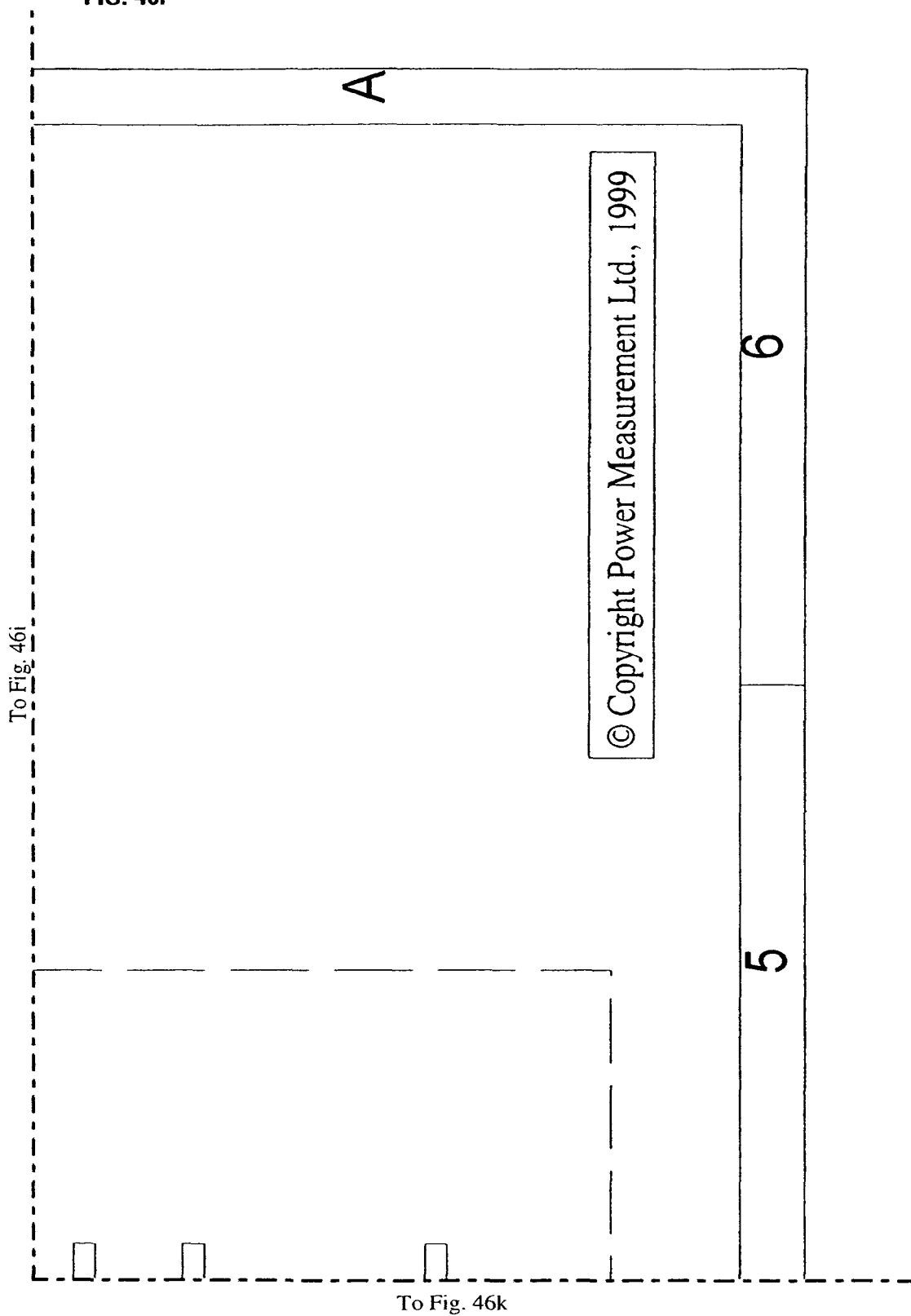
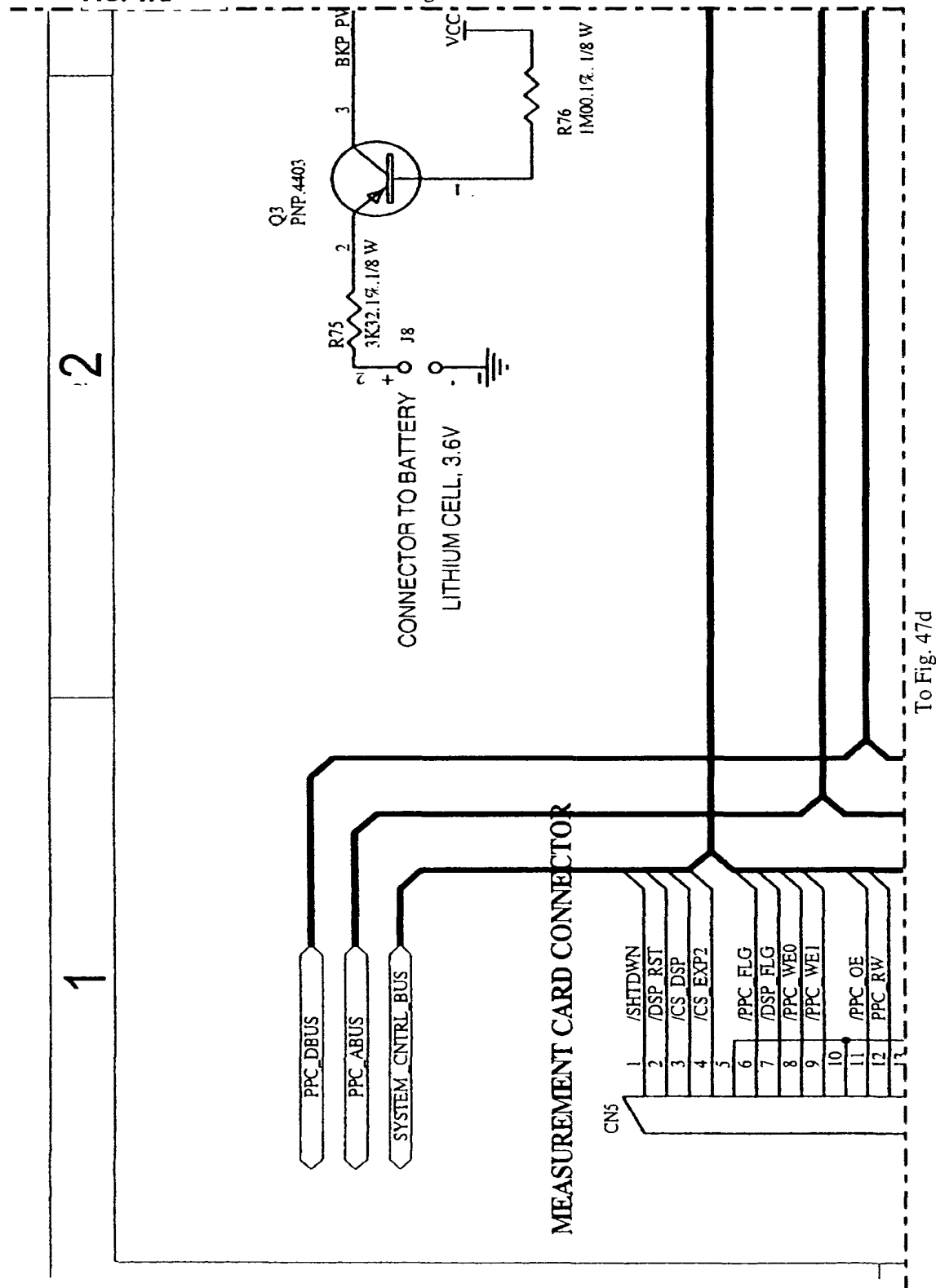
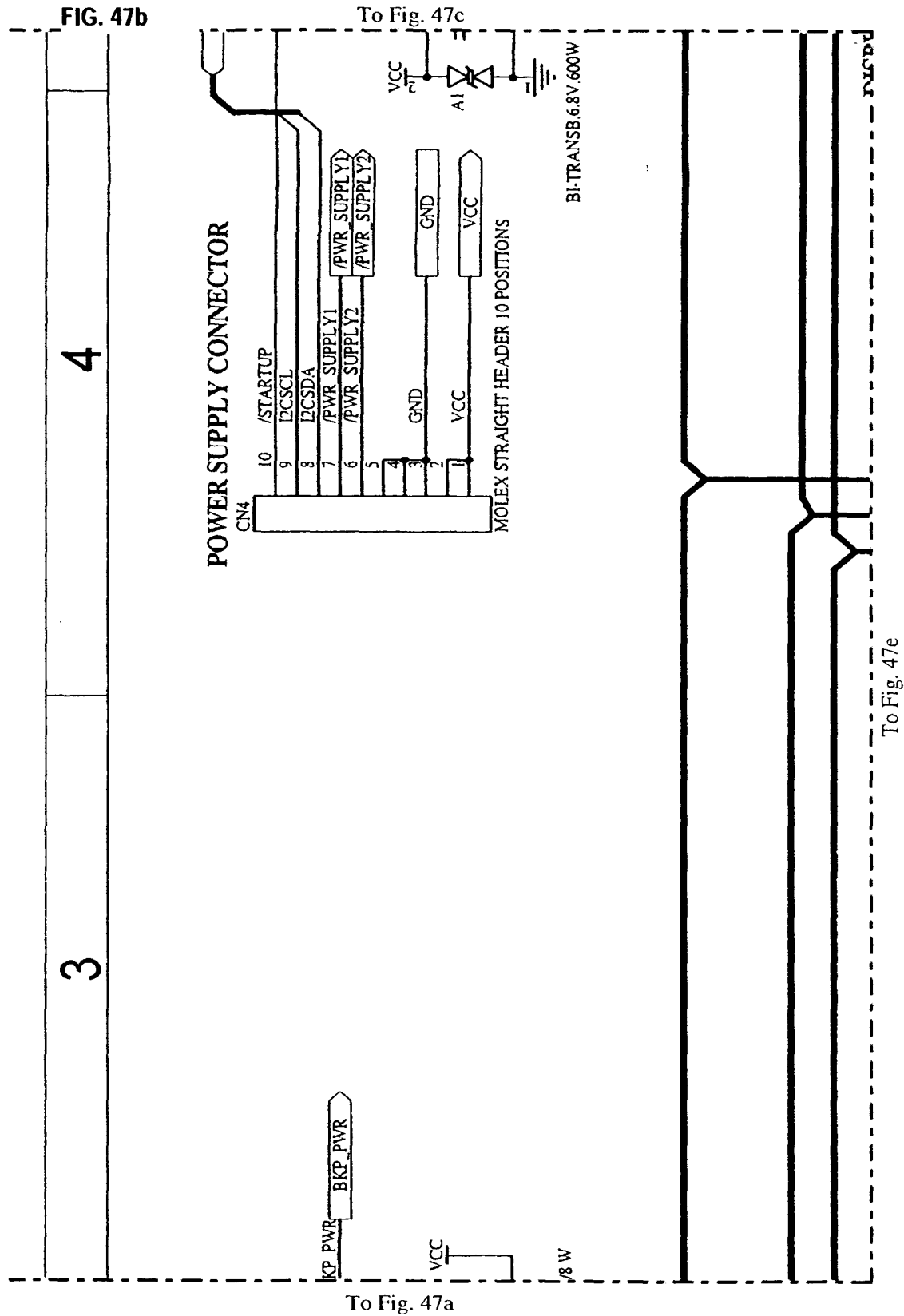


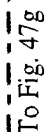
FIG. 47a

To Fig. 47b



To Fig. 47d





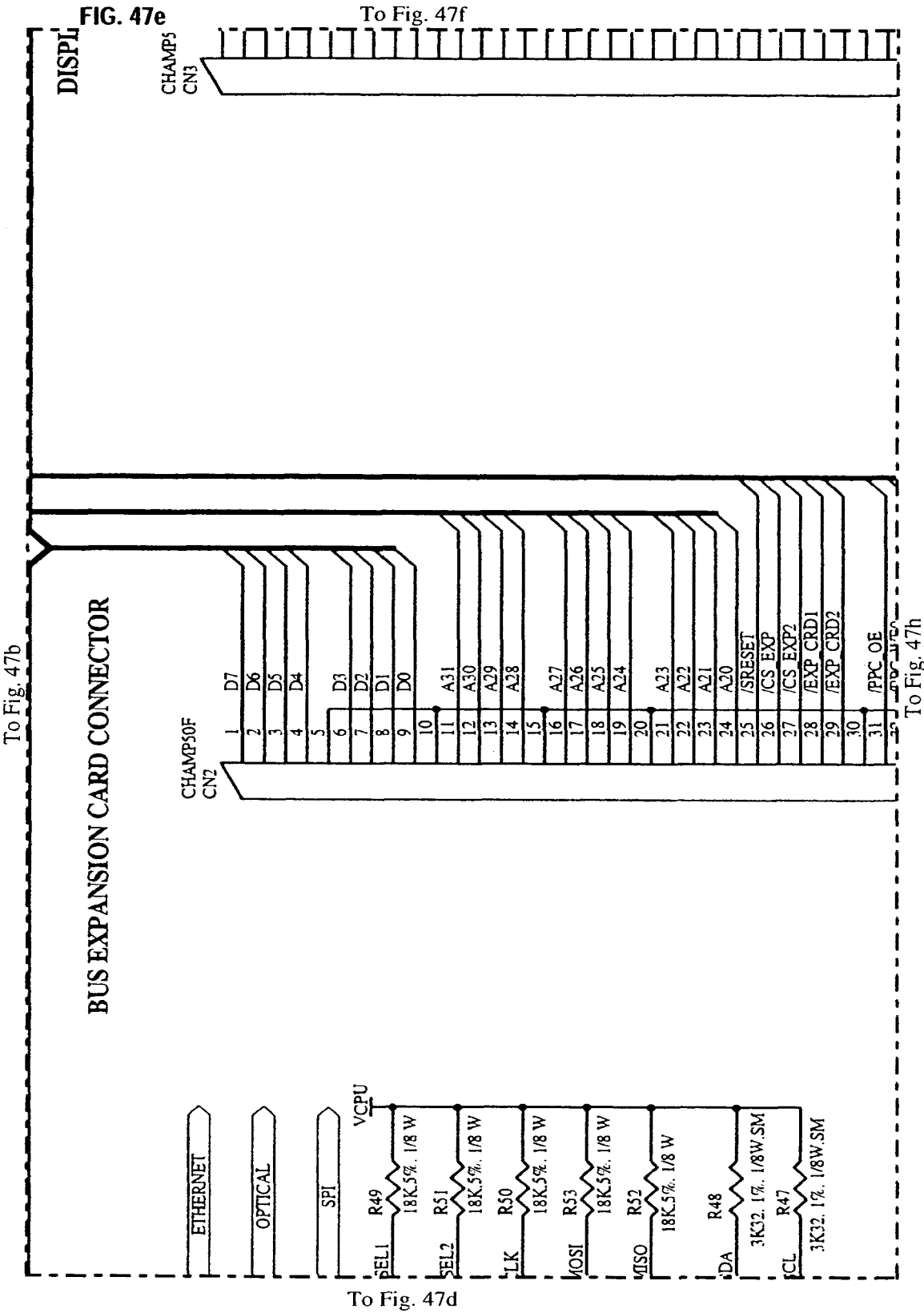
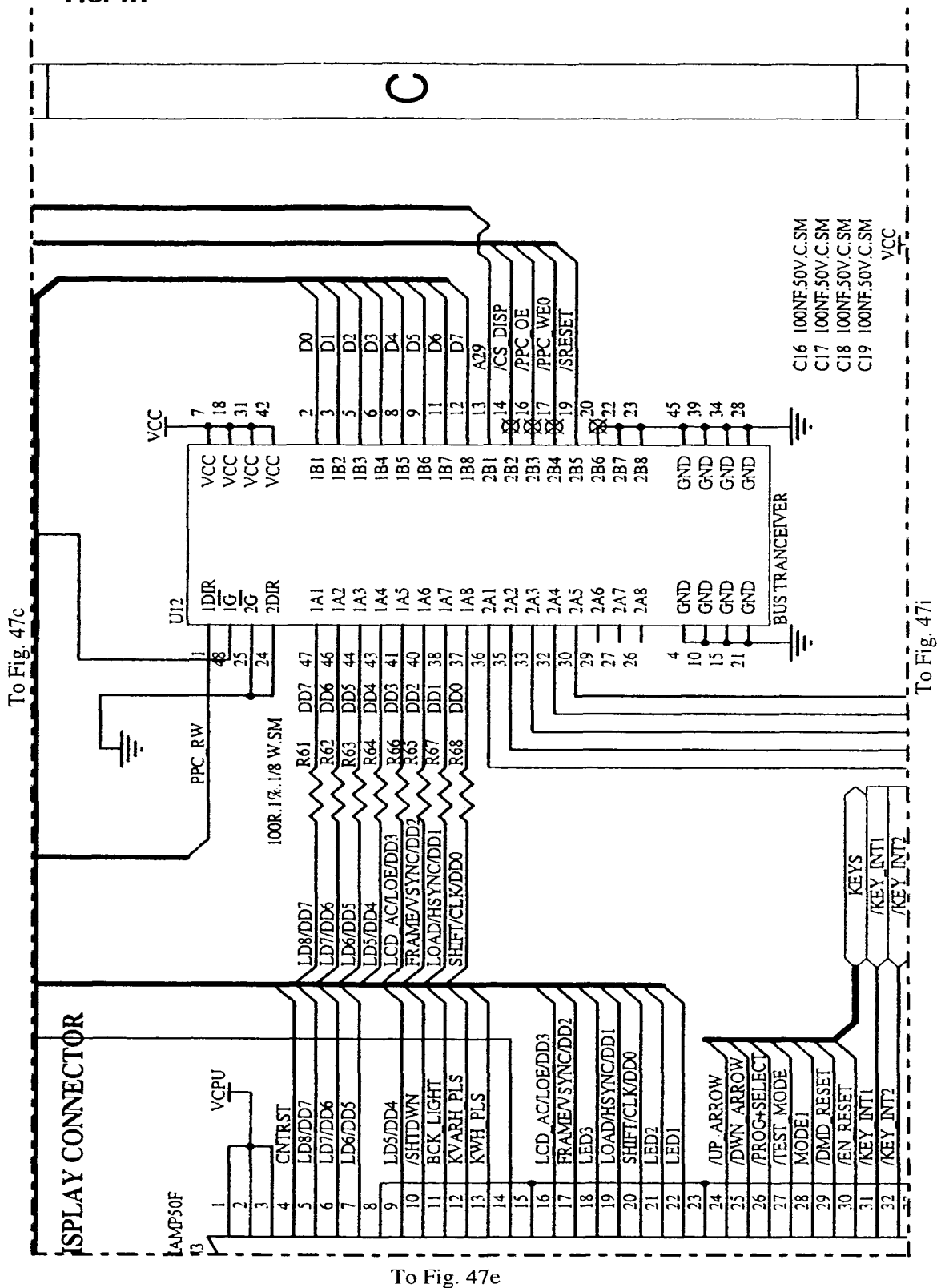
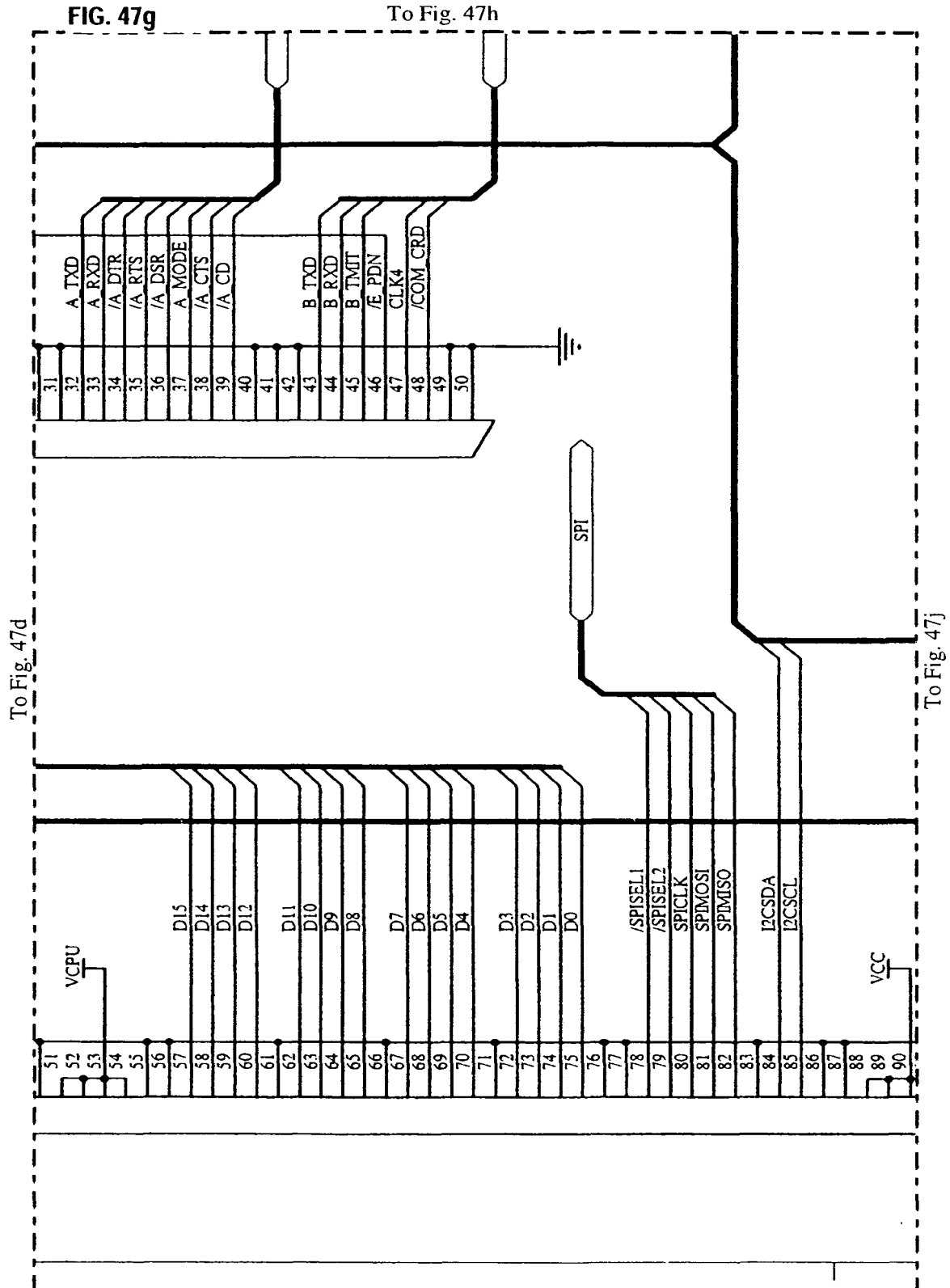


FIG. 47f





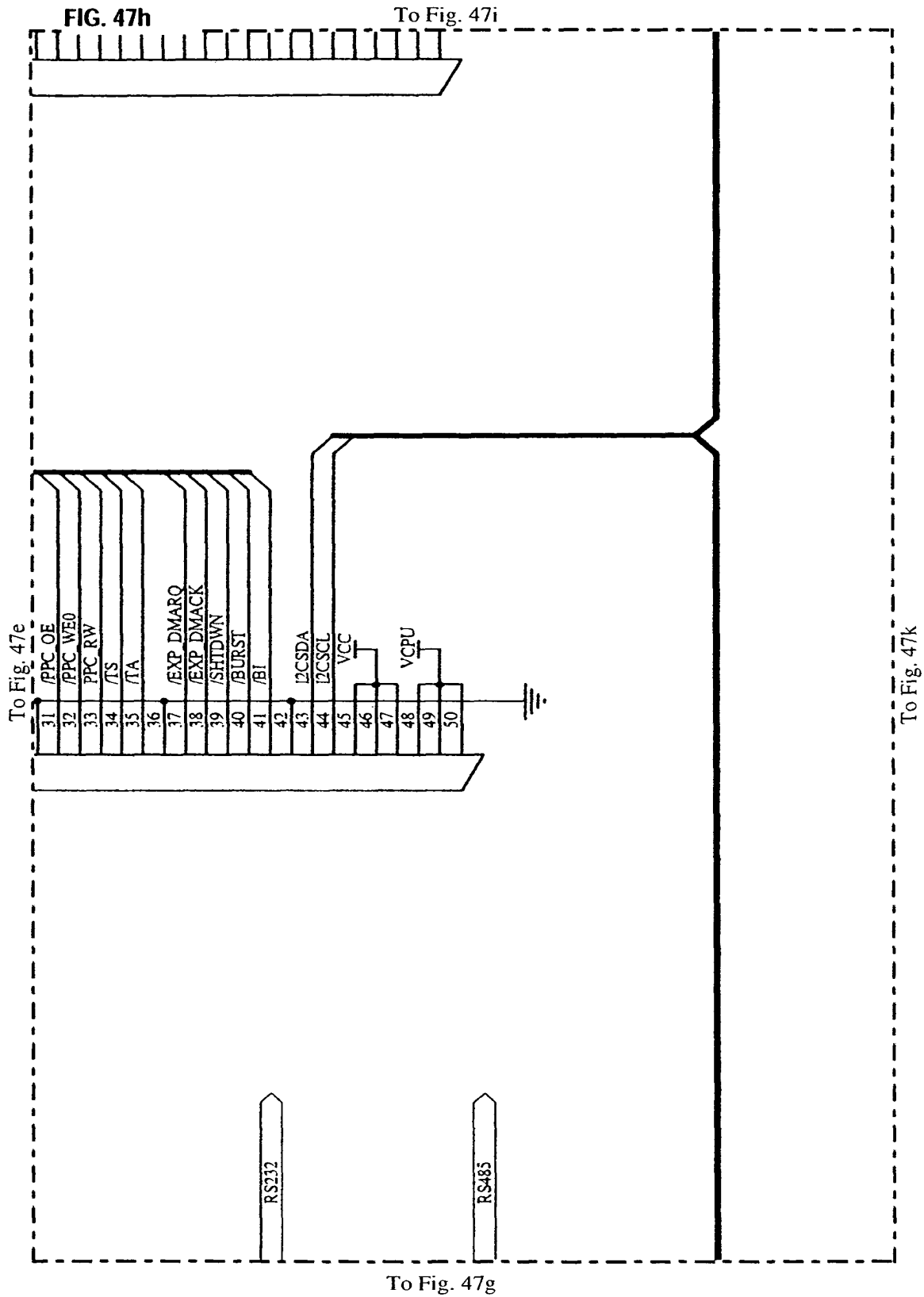


FIG. 47i

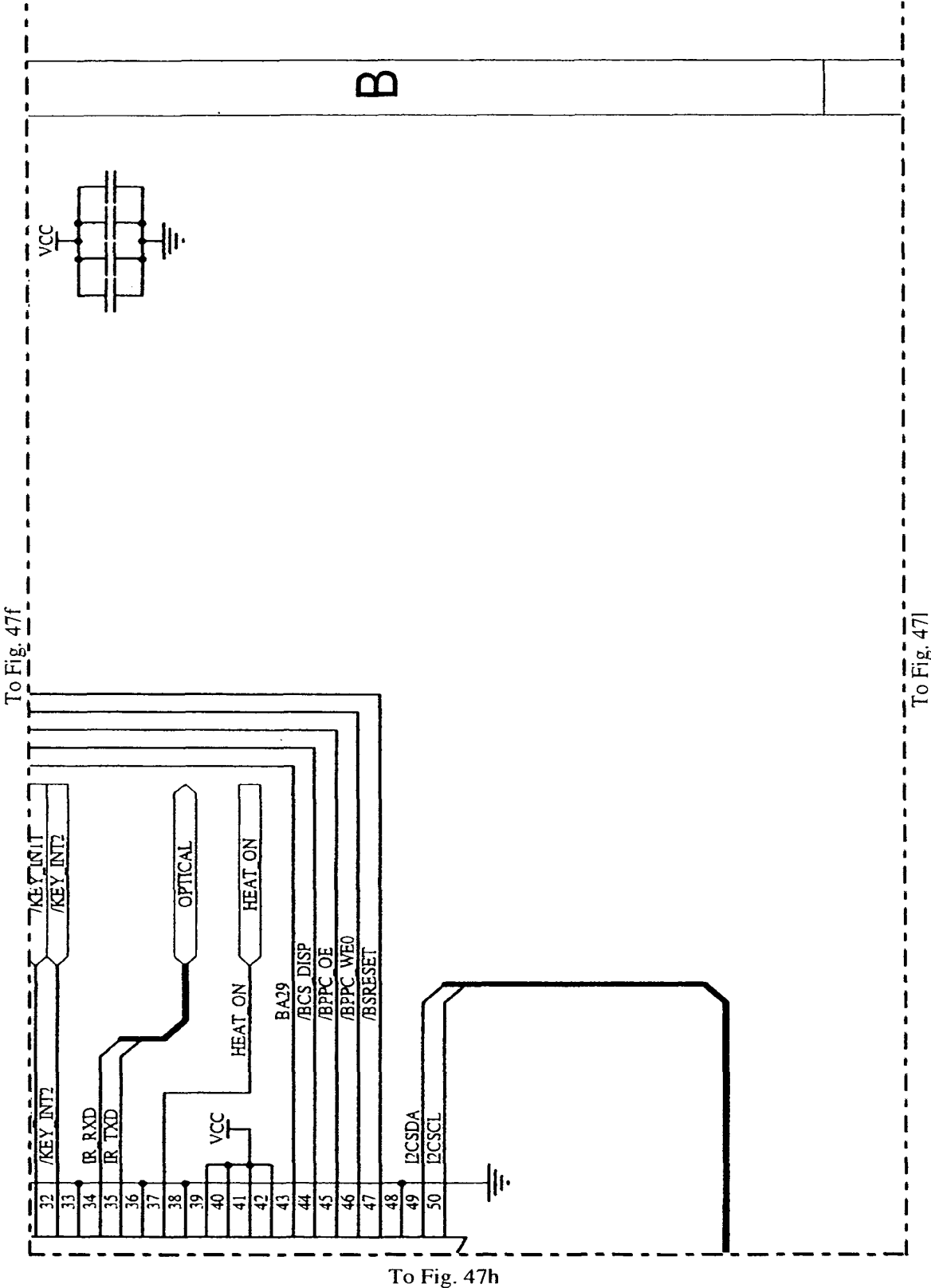


FIG. 47j

To Fig. 47k

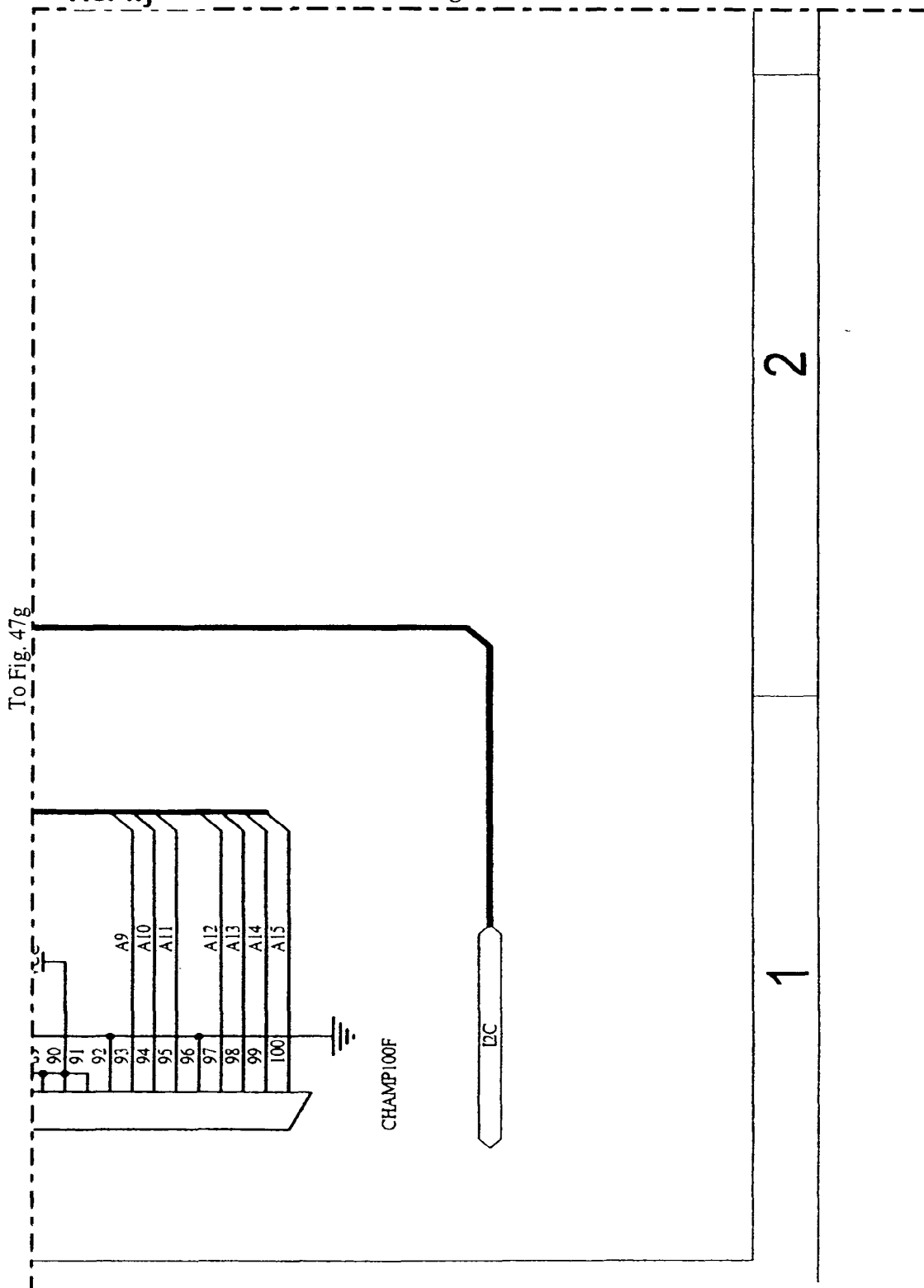


FIG. 47k

To Fig. 47l

To Fig. 47h

4

3

To Fig. 47j

FIG. 47i

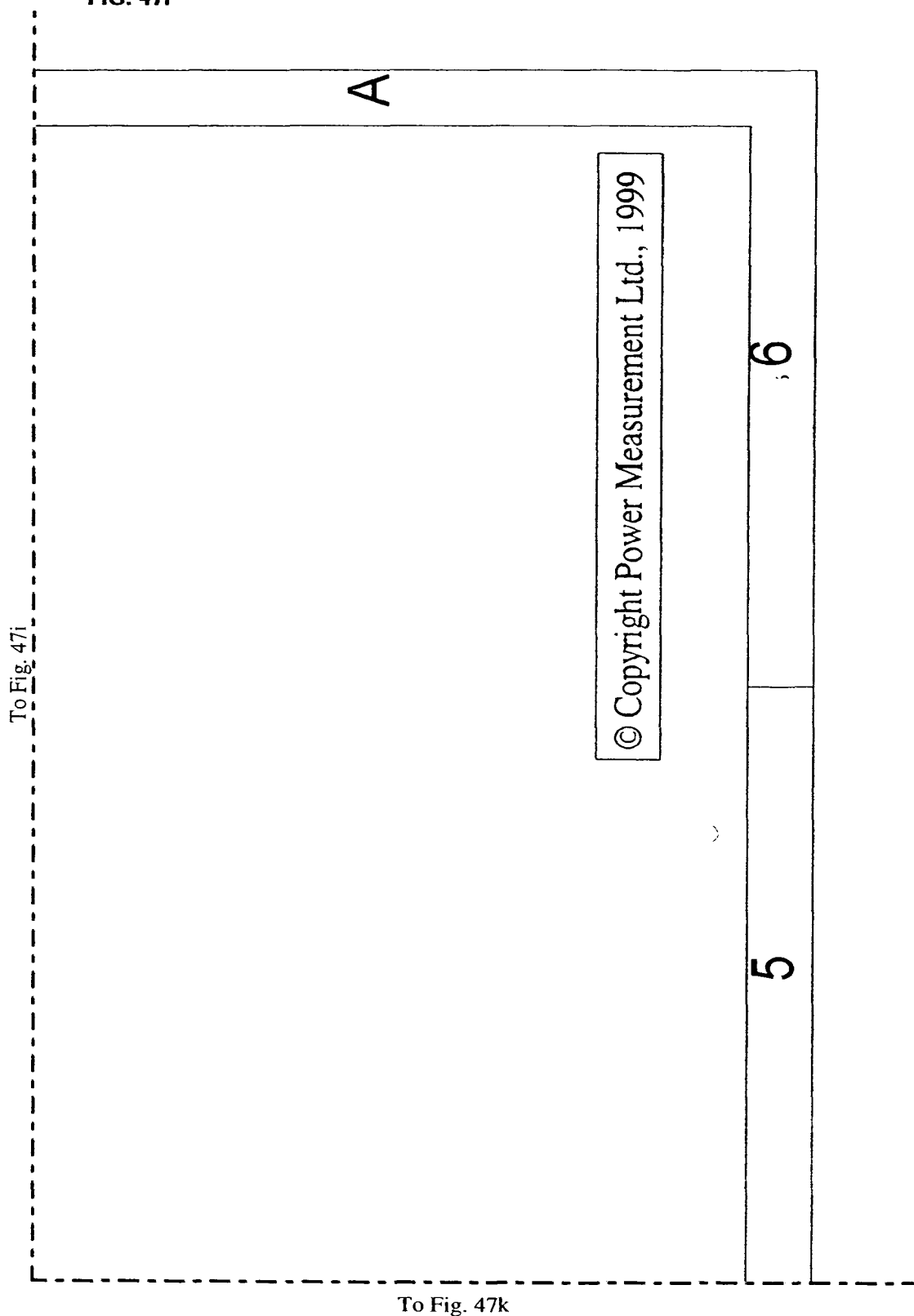
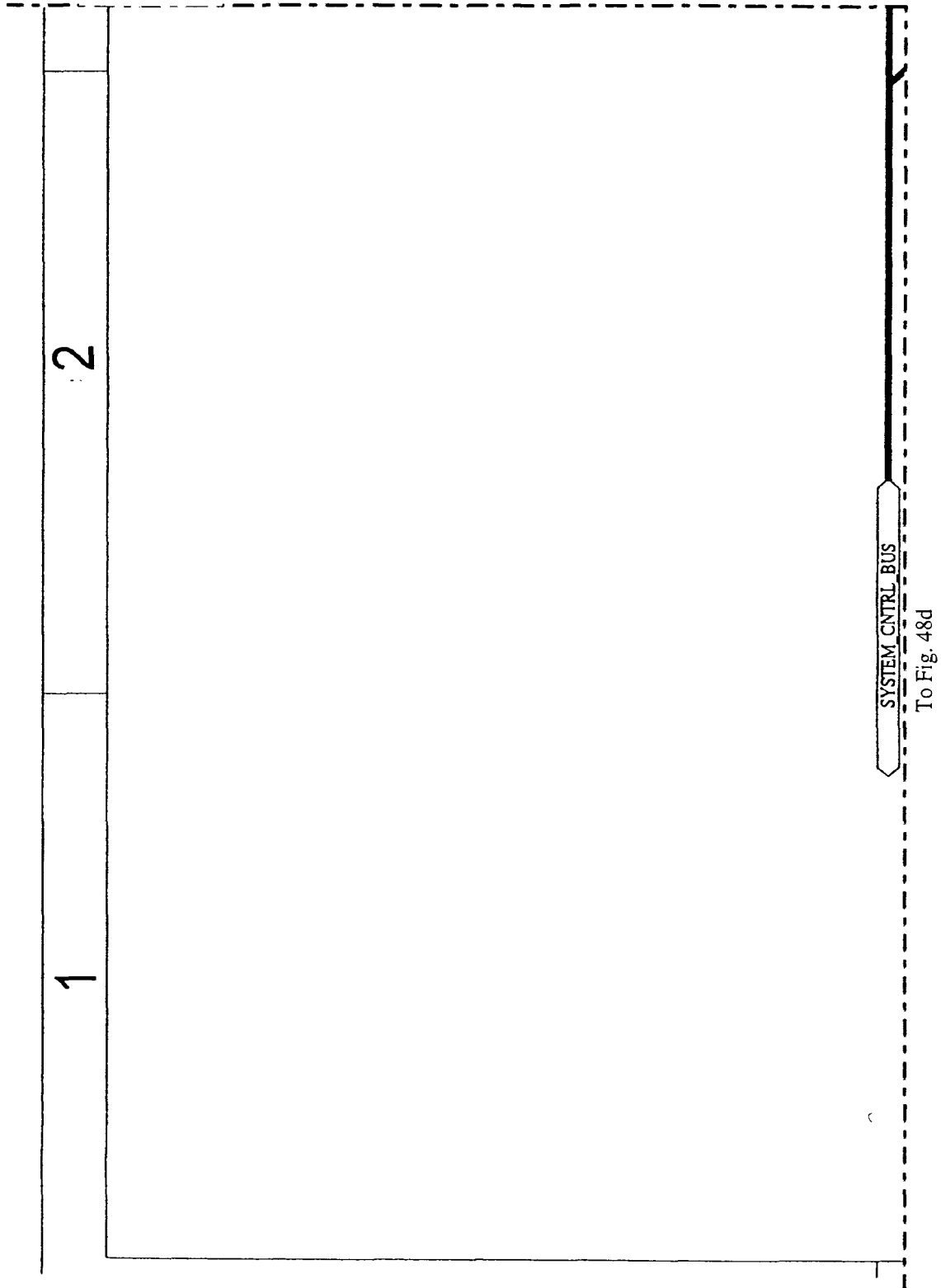


FIG. 48a

To Fig. 48b



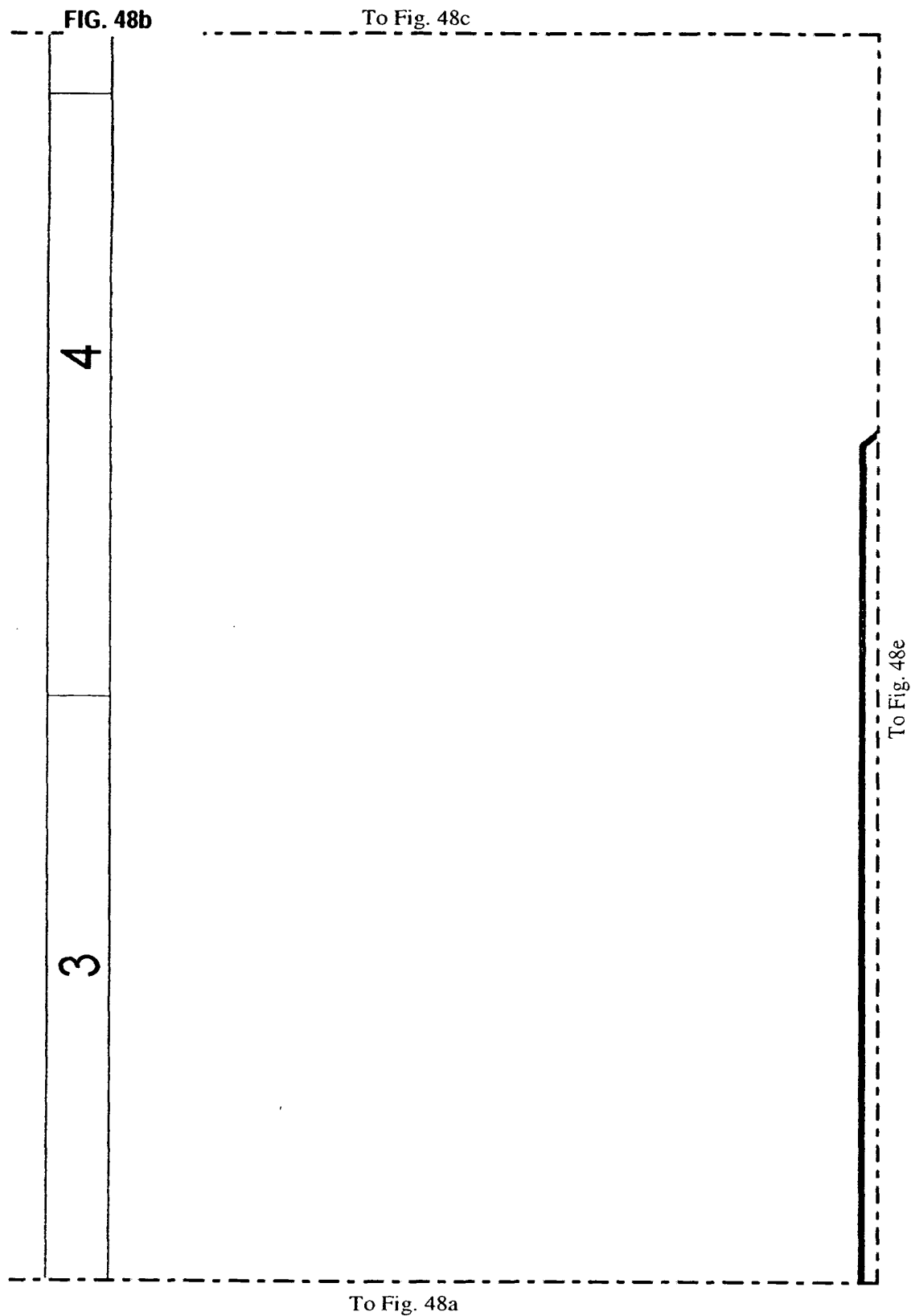
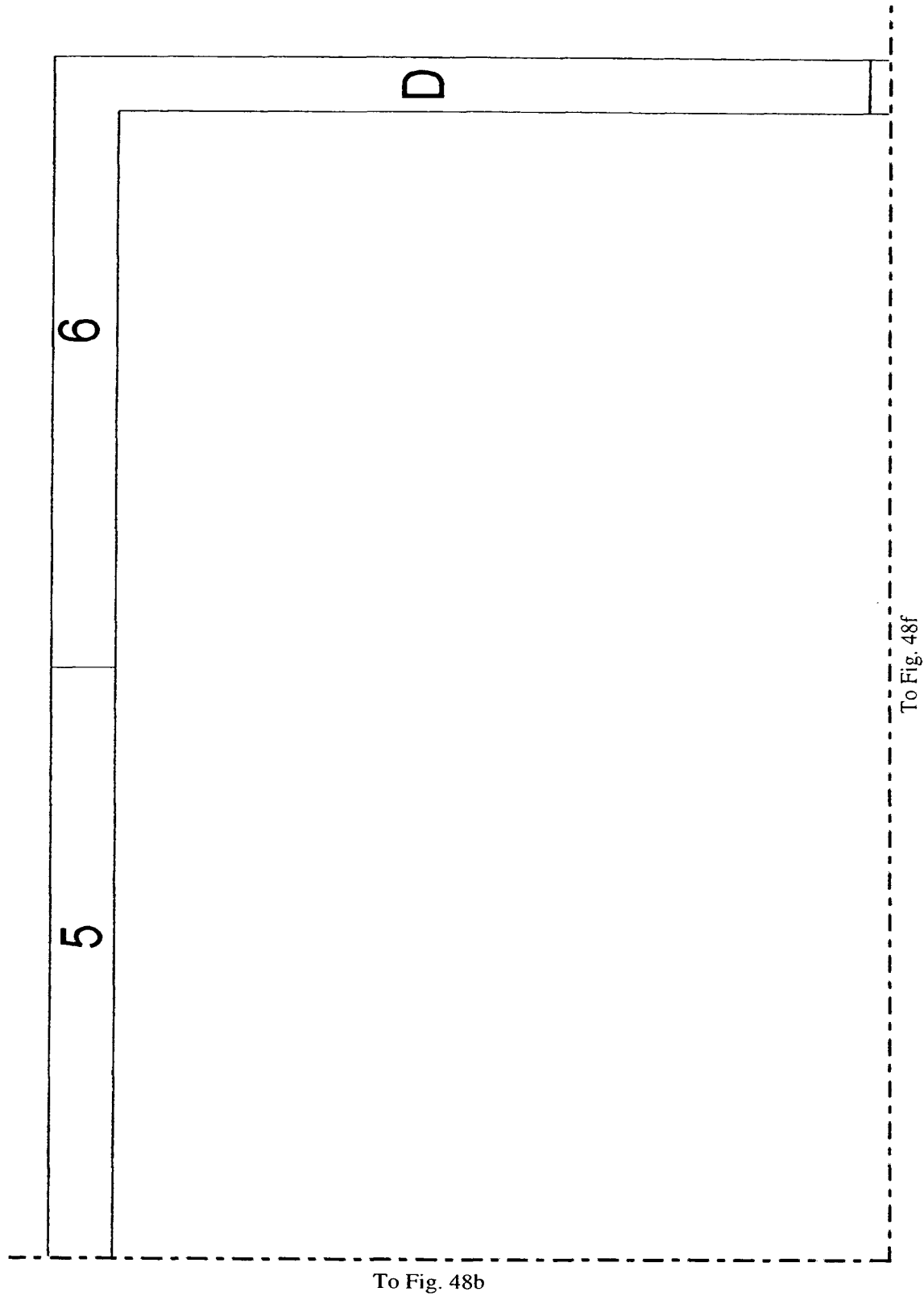
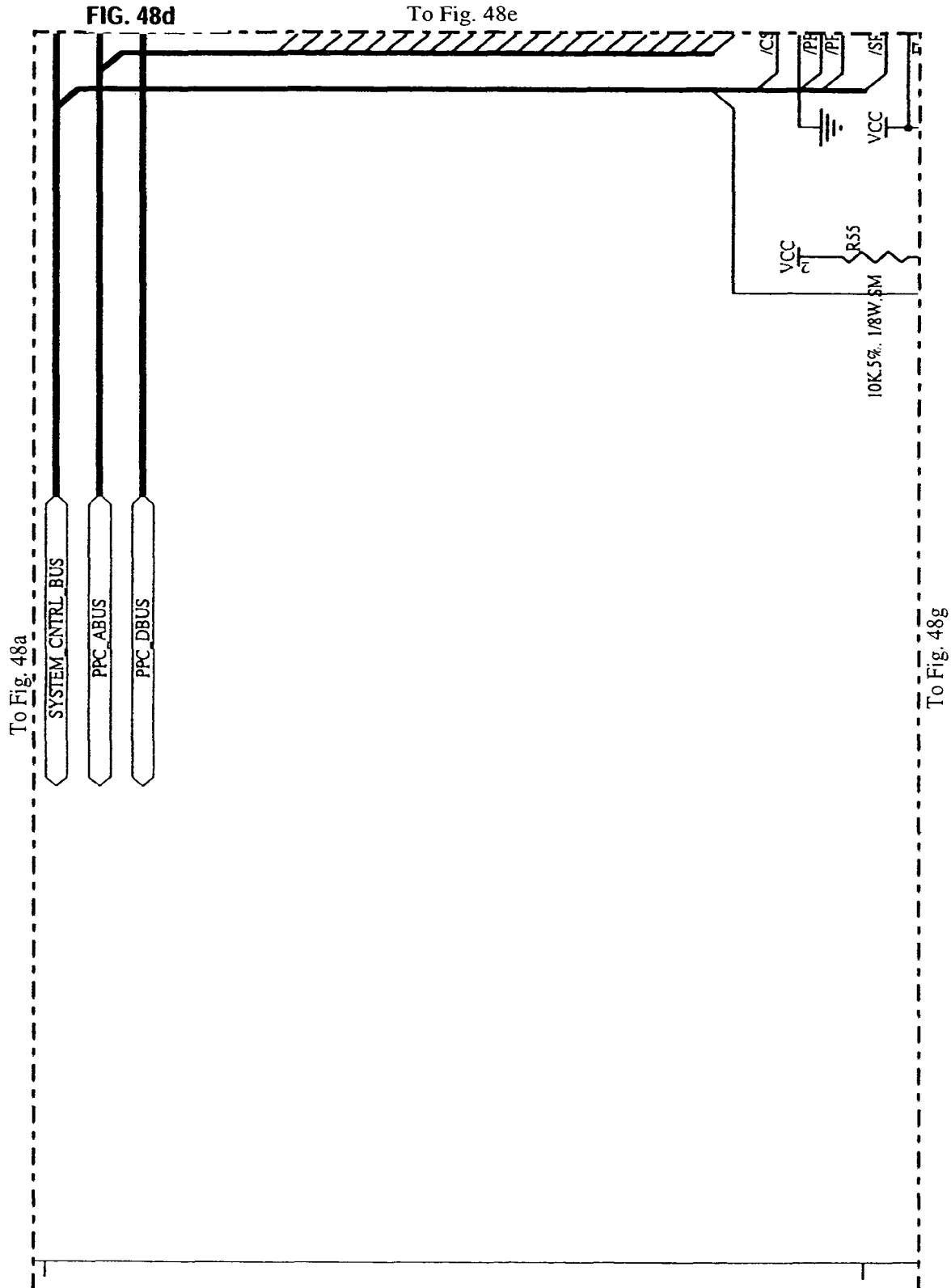


FIG. 48c





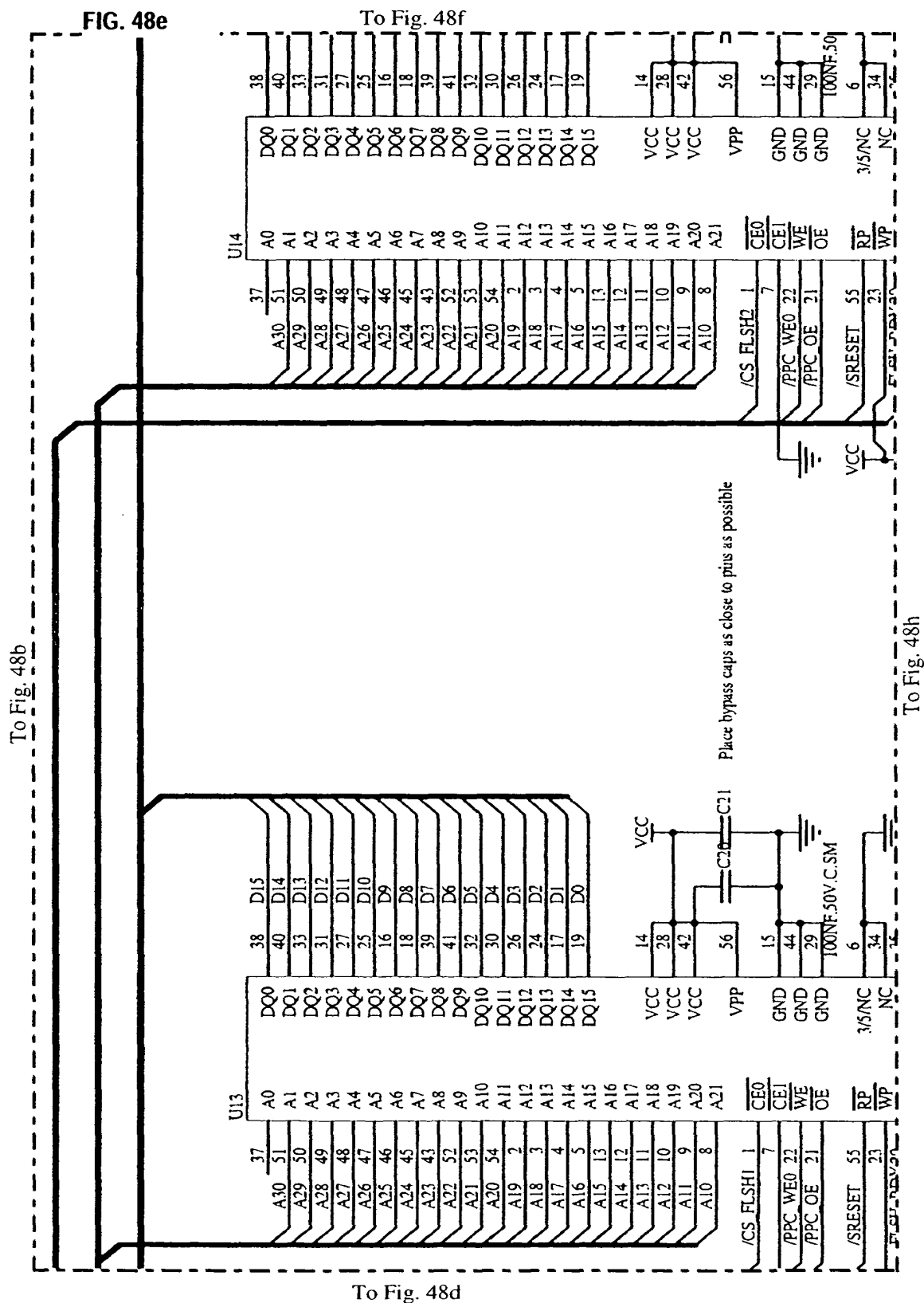


FIG. 48f

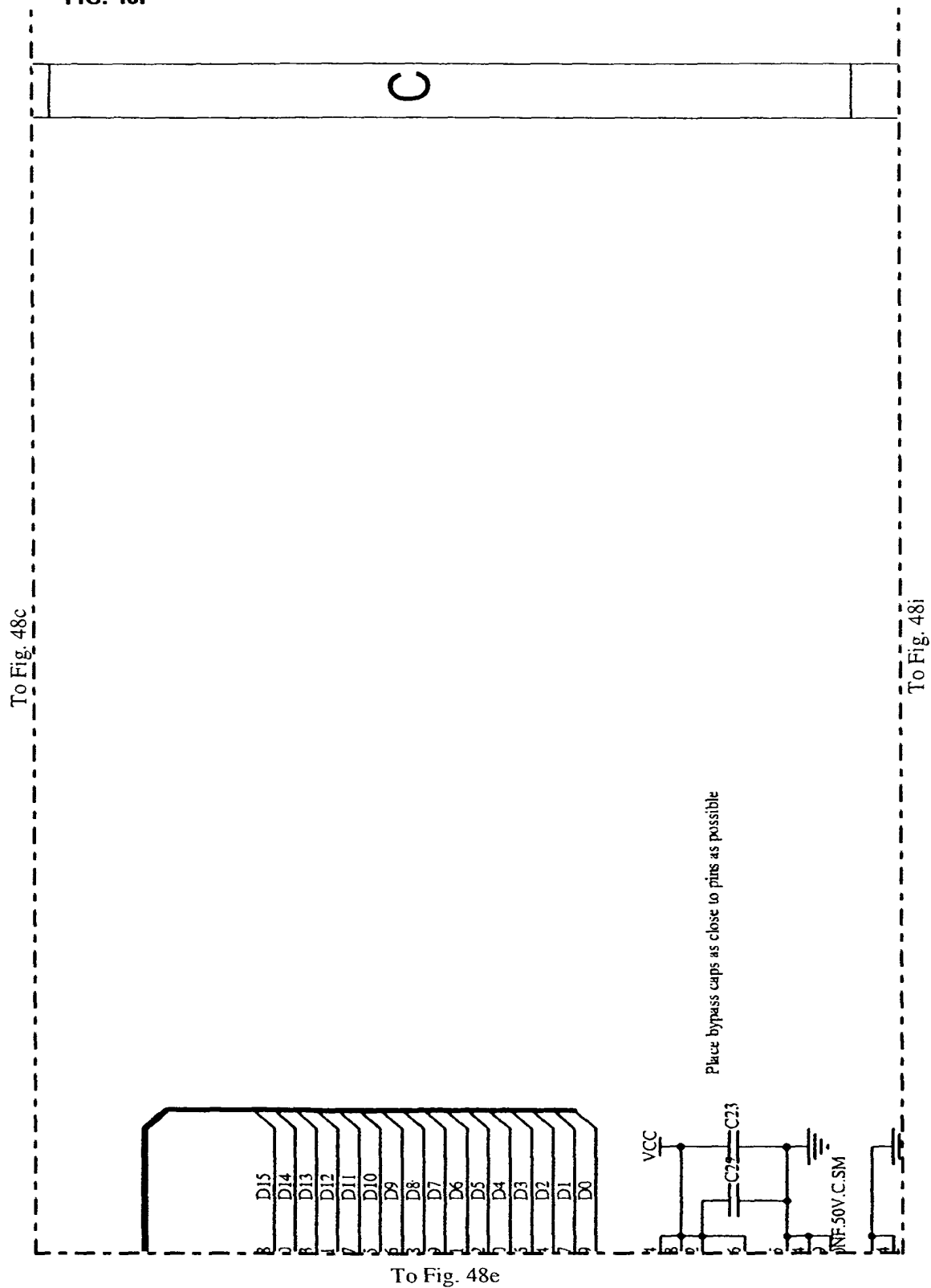
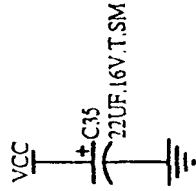


FIG. 48g

To Fig. 48h

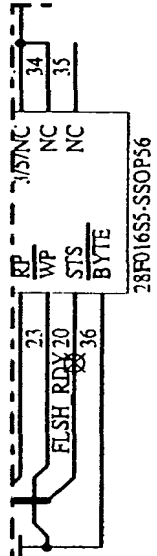


Bypass cap. for both banks.
Place close to FLASH components

To Fig. 48d

To Fig. 48j

FIG. 48h



To Fig. 48i

Supp
Intel
Intel

NOTES:

1. 2 Banks of 2/4 MB each. Total of 8 MB
2. BOOT bank must be populated. FLSH2 bank is for expansion

To Fig. 48k

To Fig. 48g

FIG. 48i

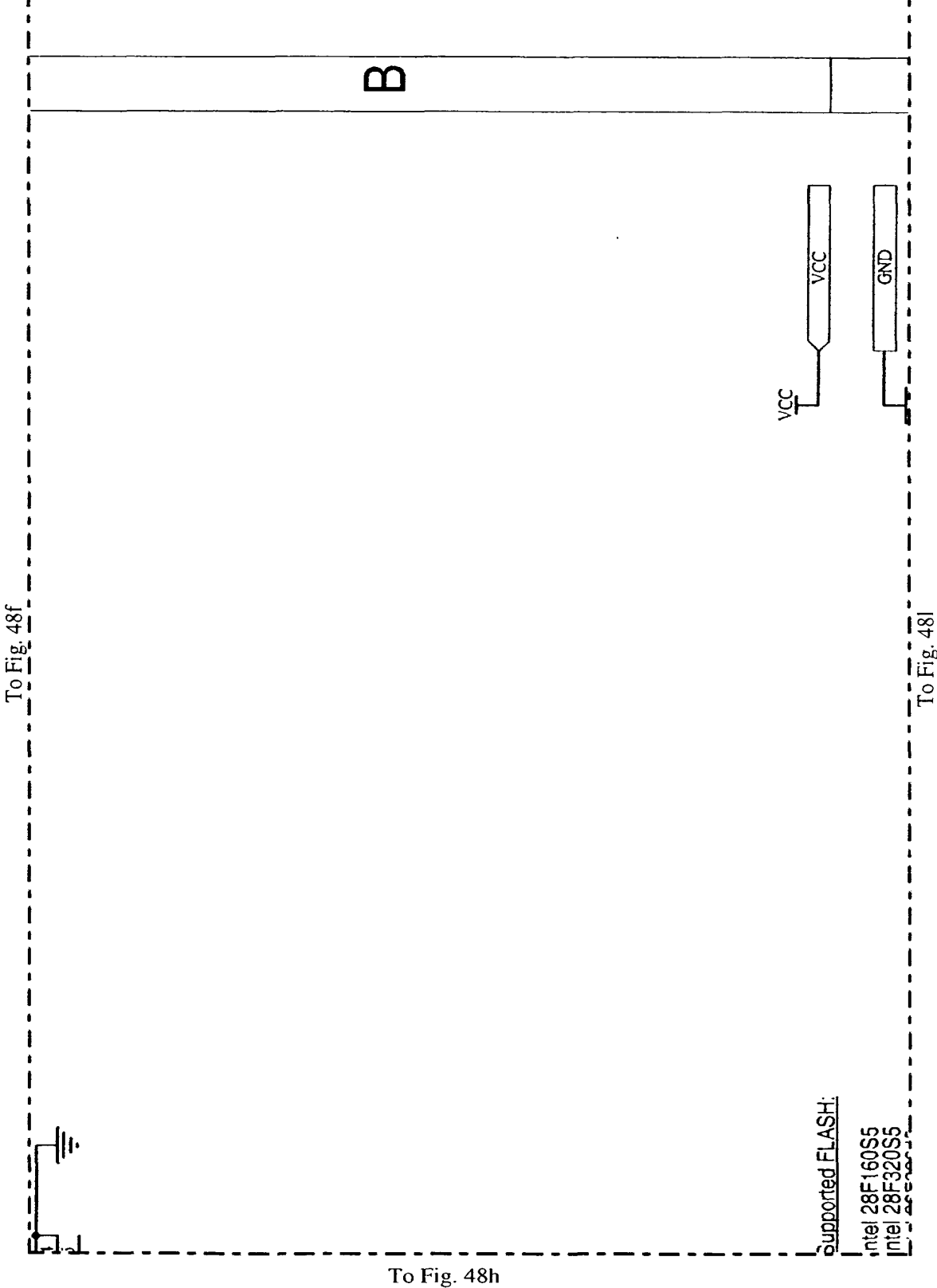


FIG. 48j

To Fig. 48k

To Fig. 48g

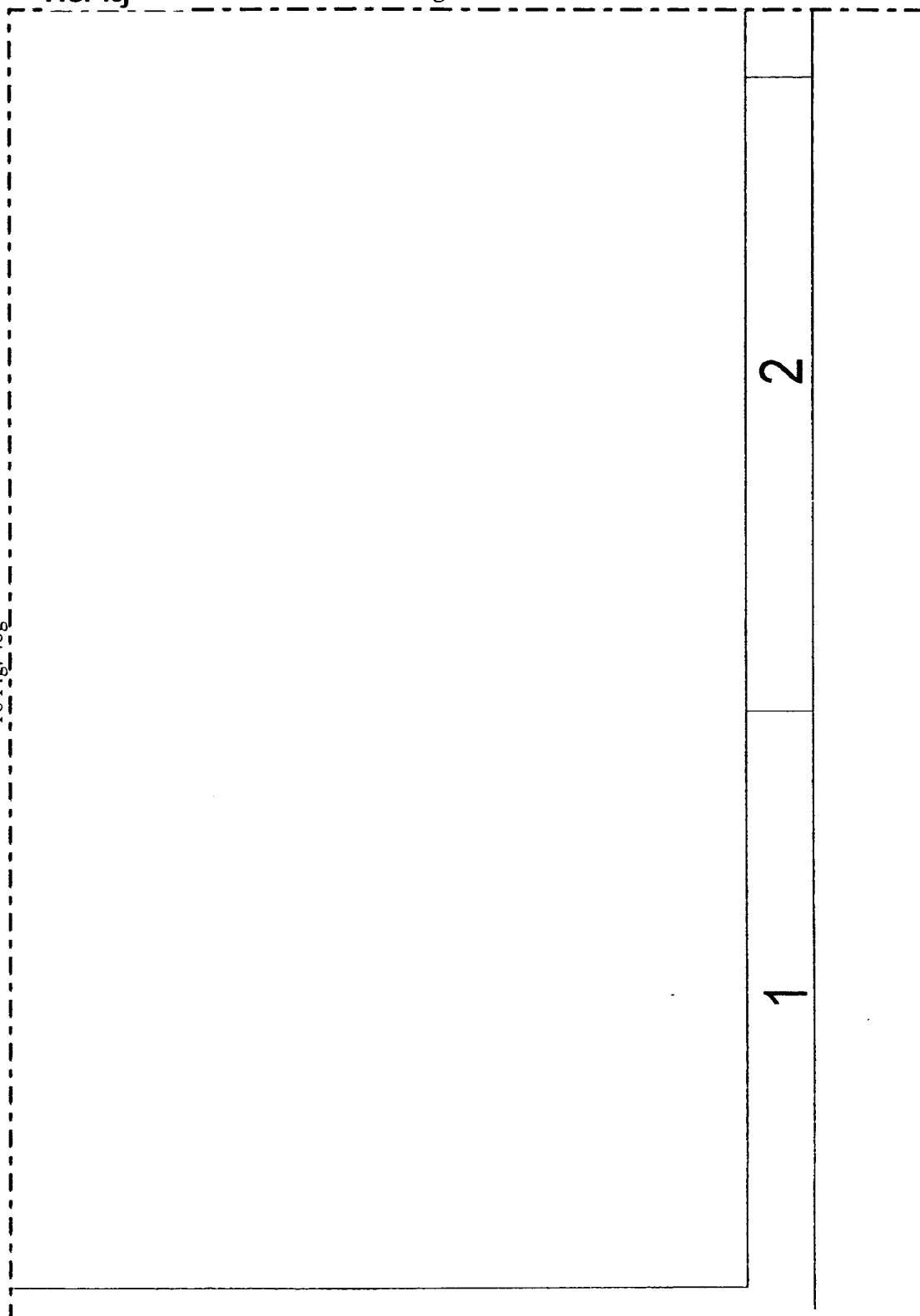


FIG. 48k

To Fig. 48l

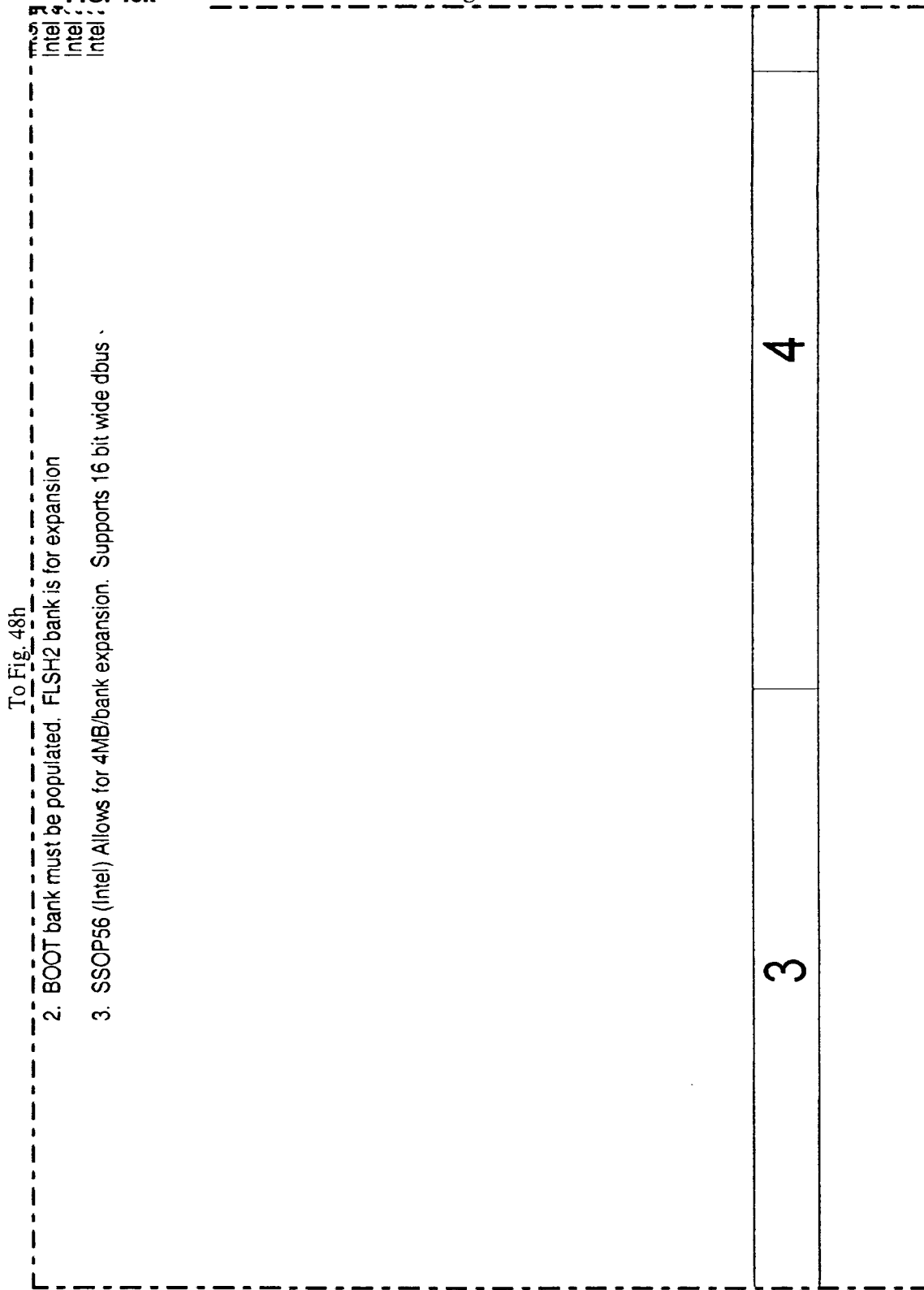
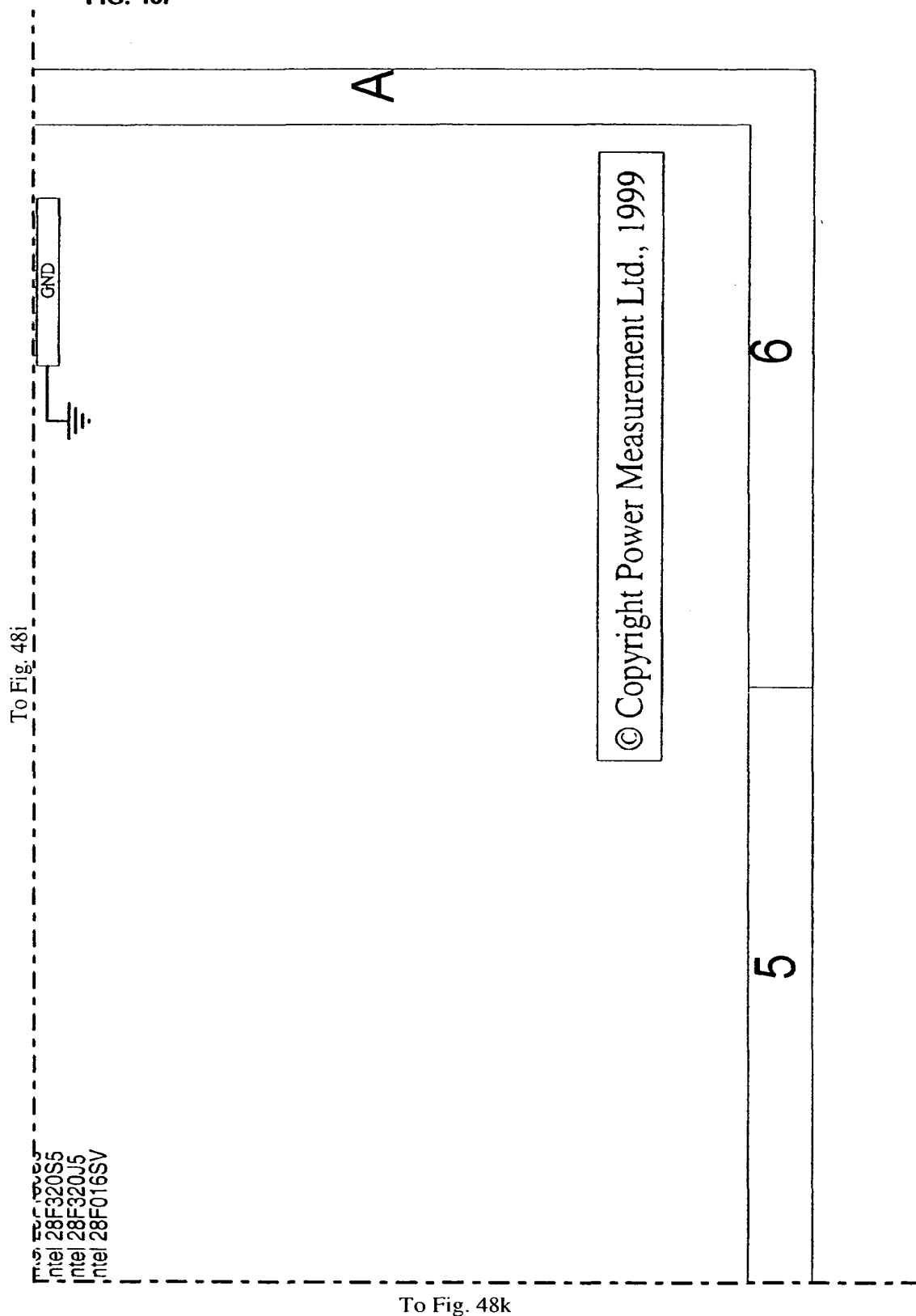
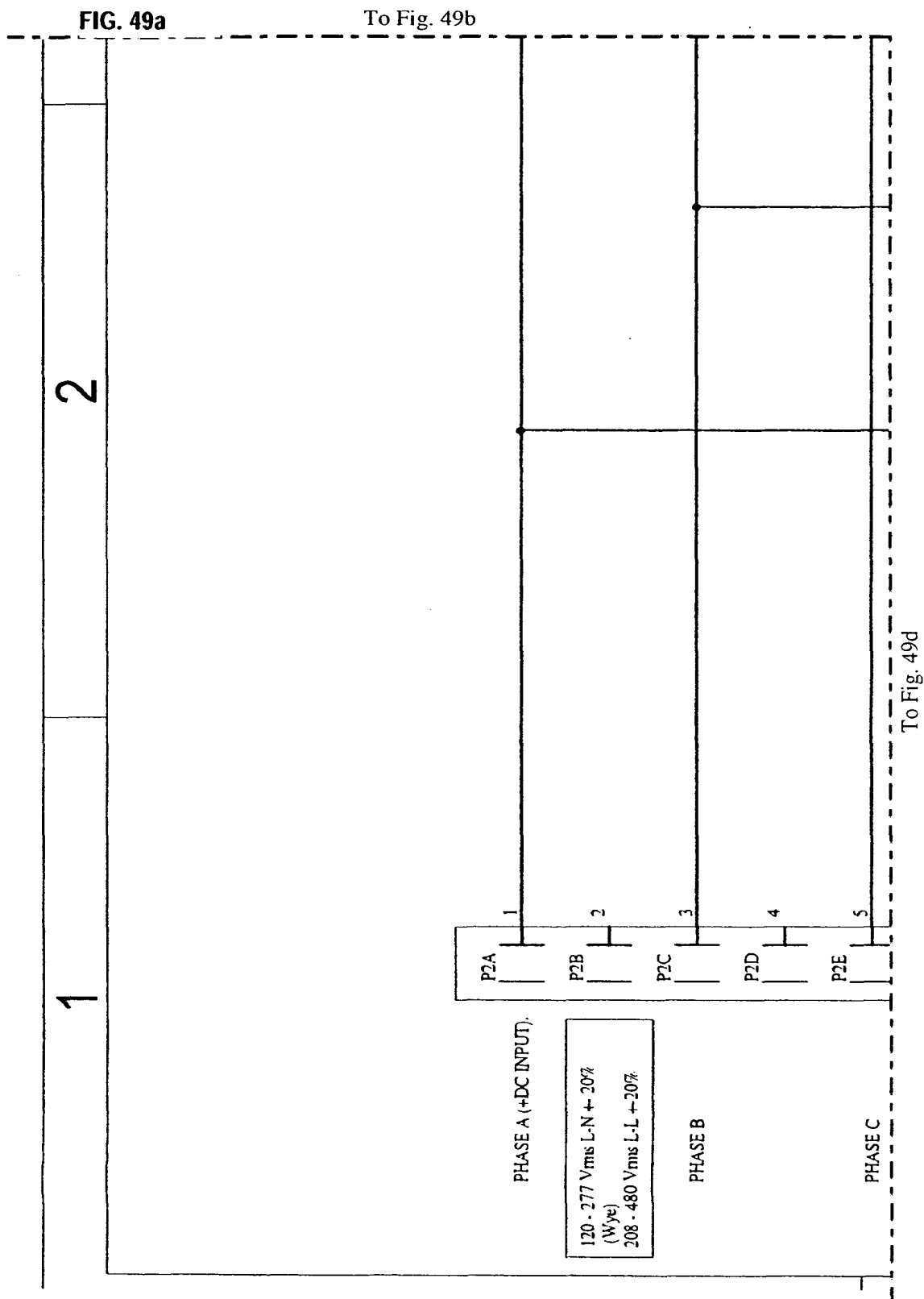


FIG. 48i





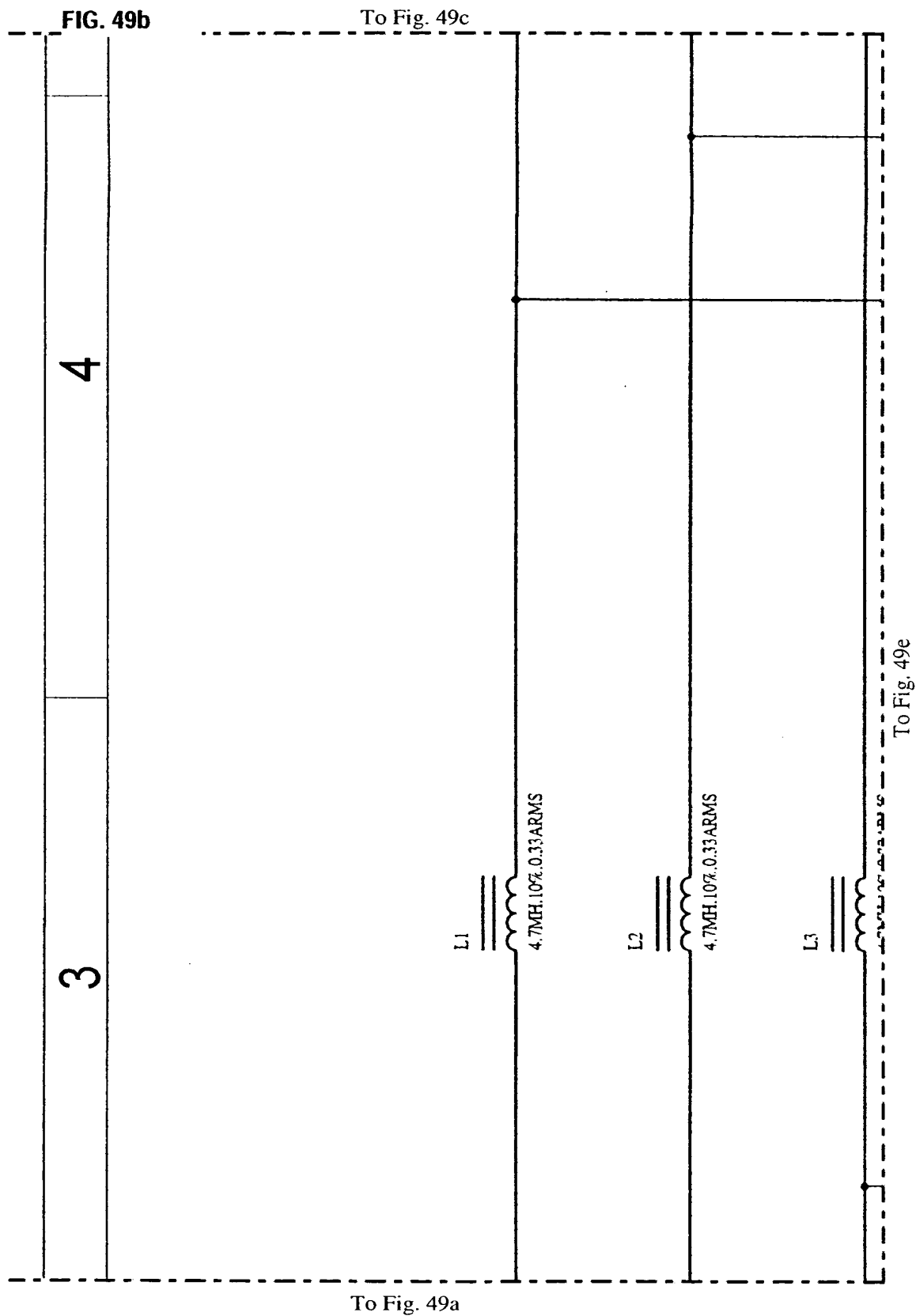
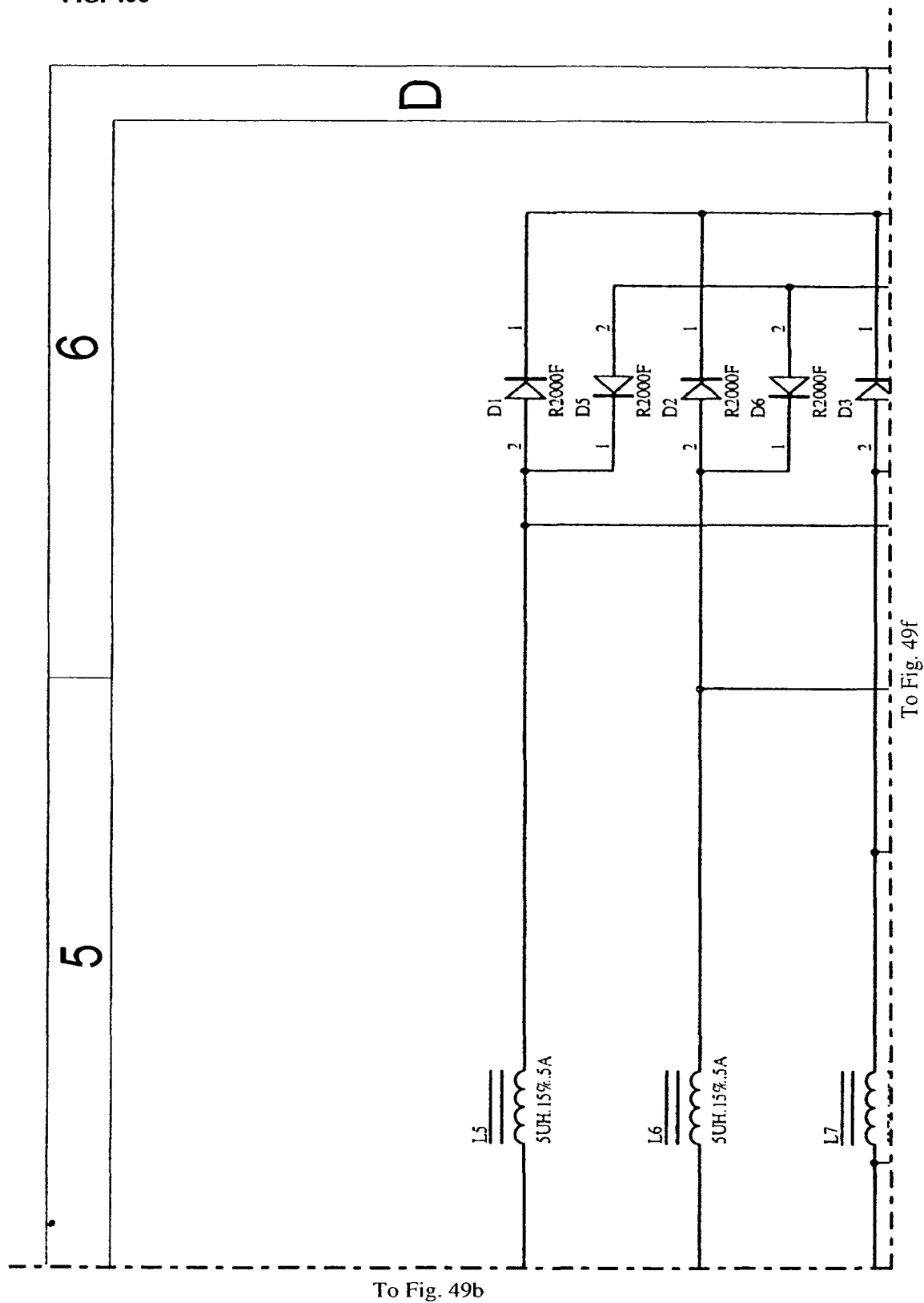
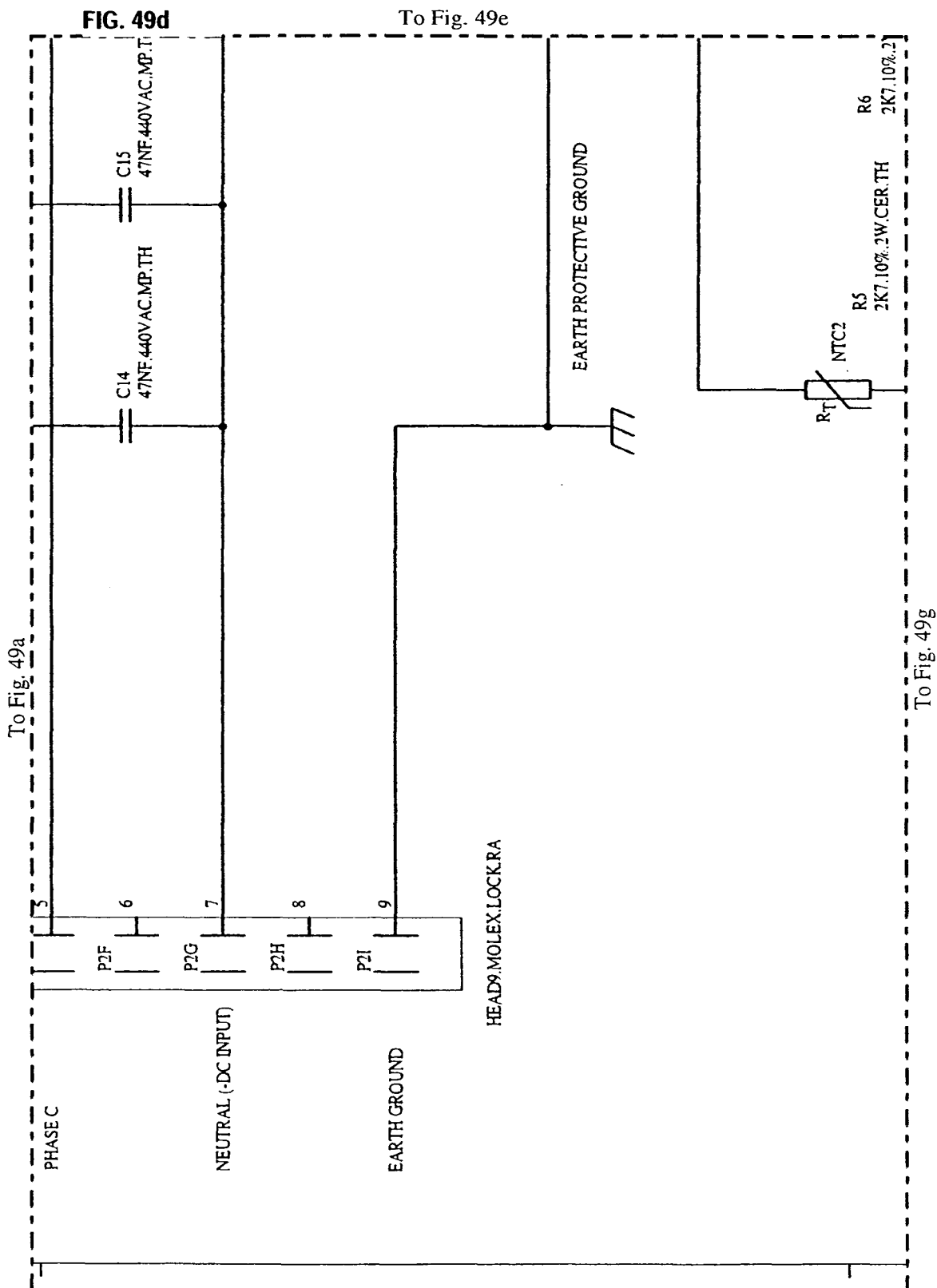


FIG. 49c





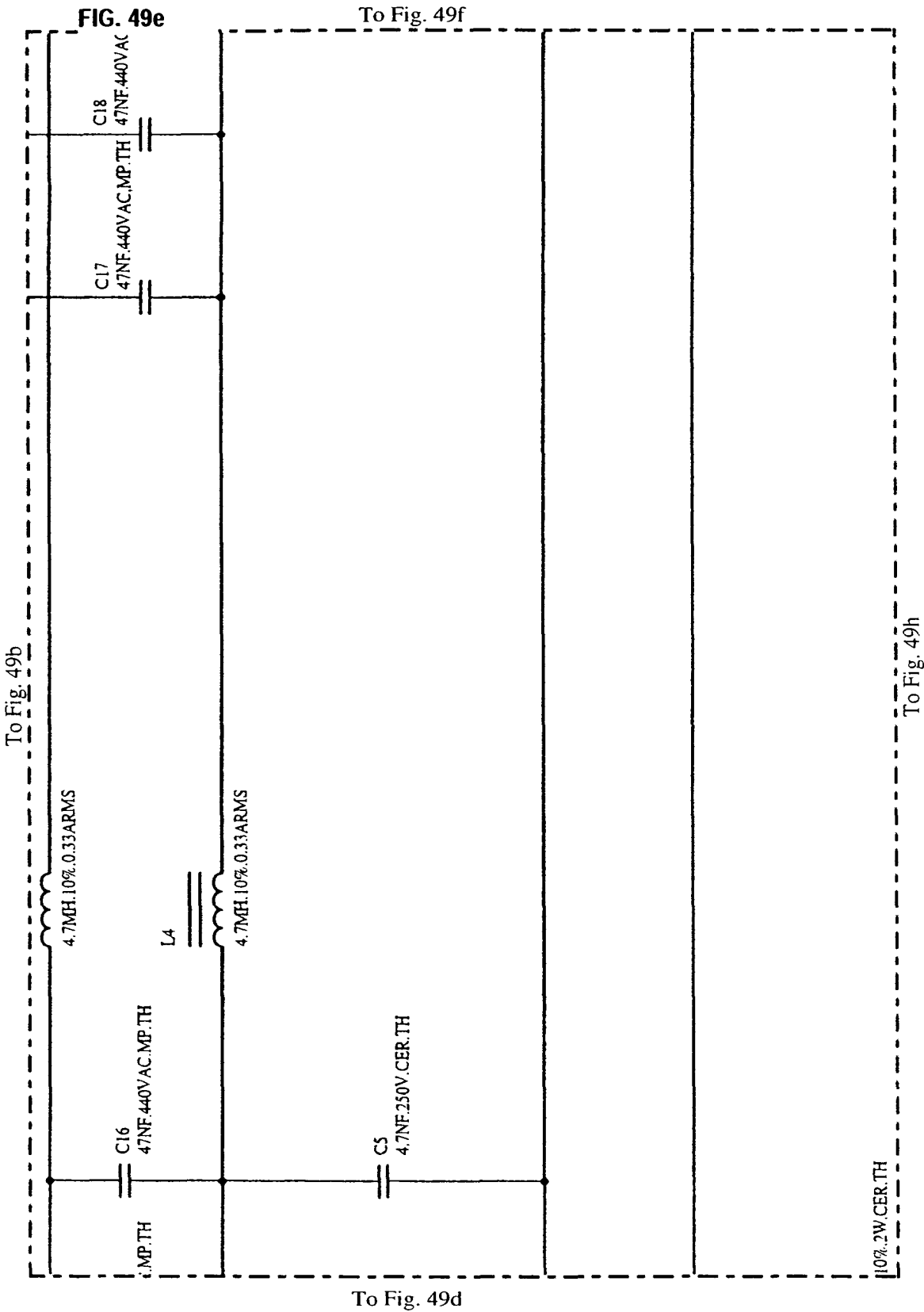
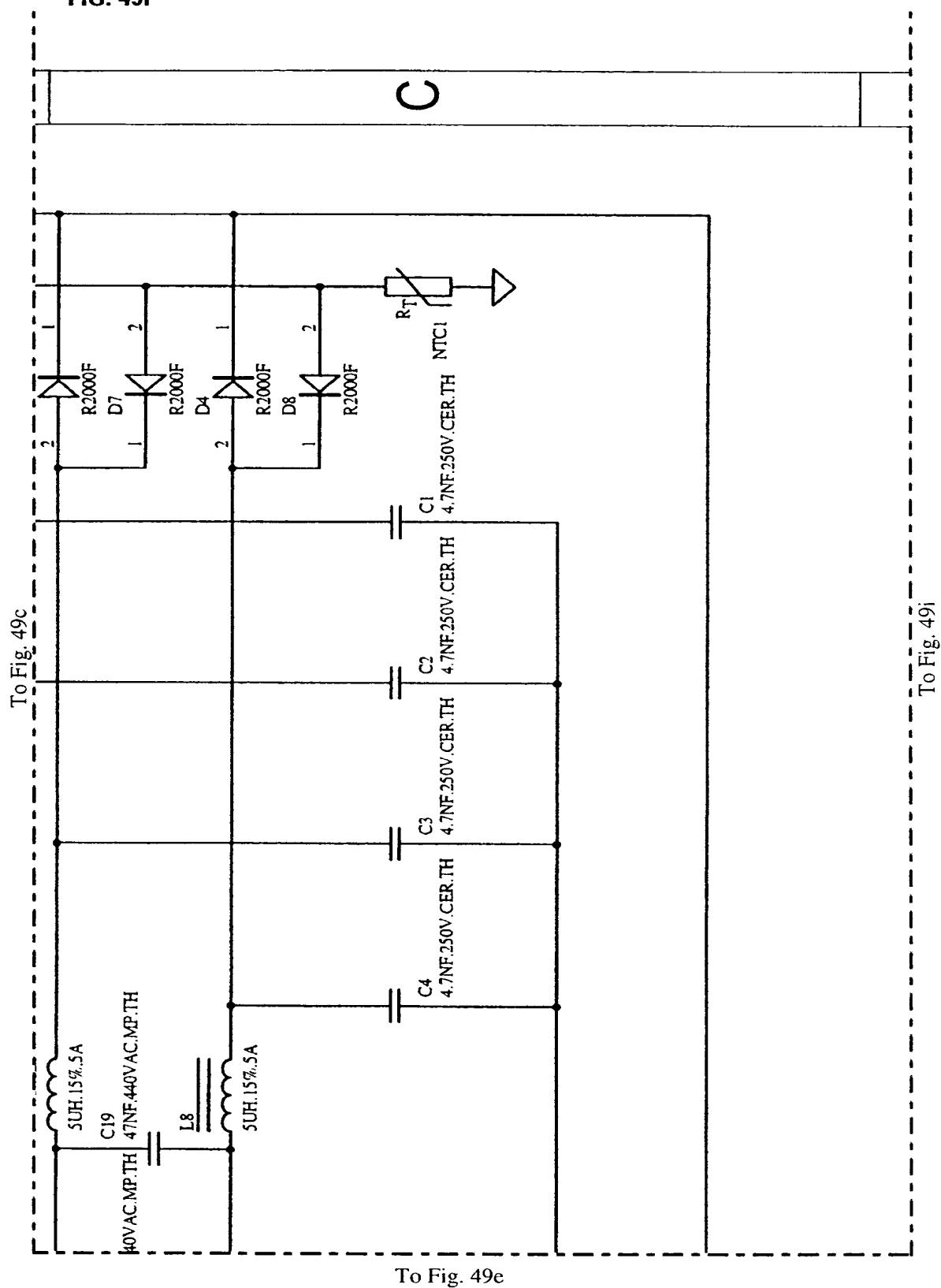


FIG. 49f





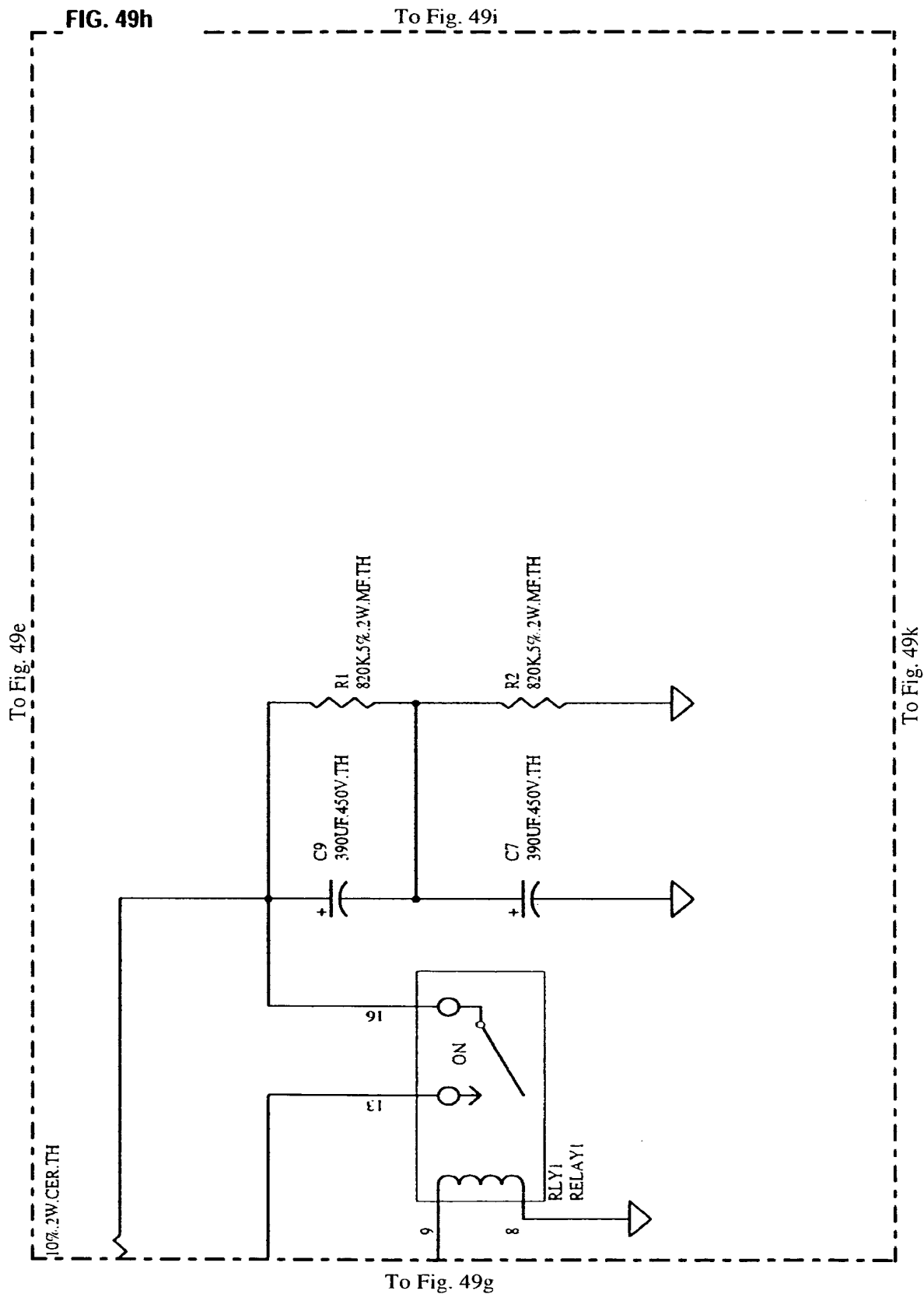
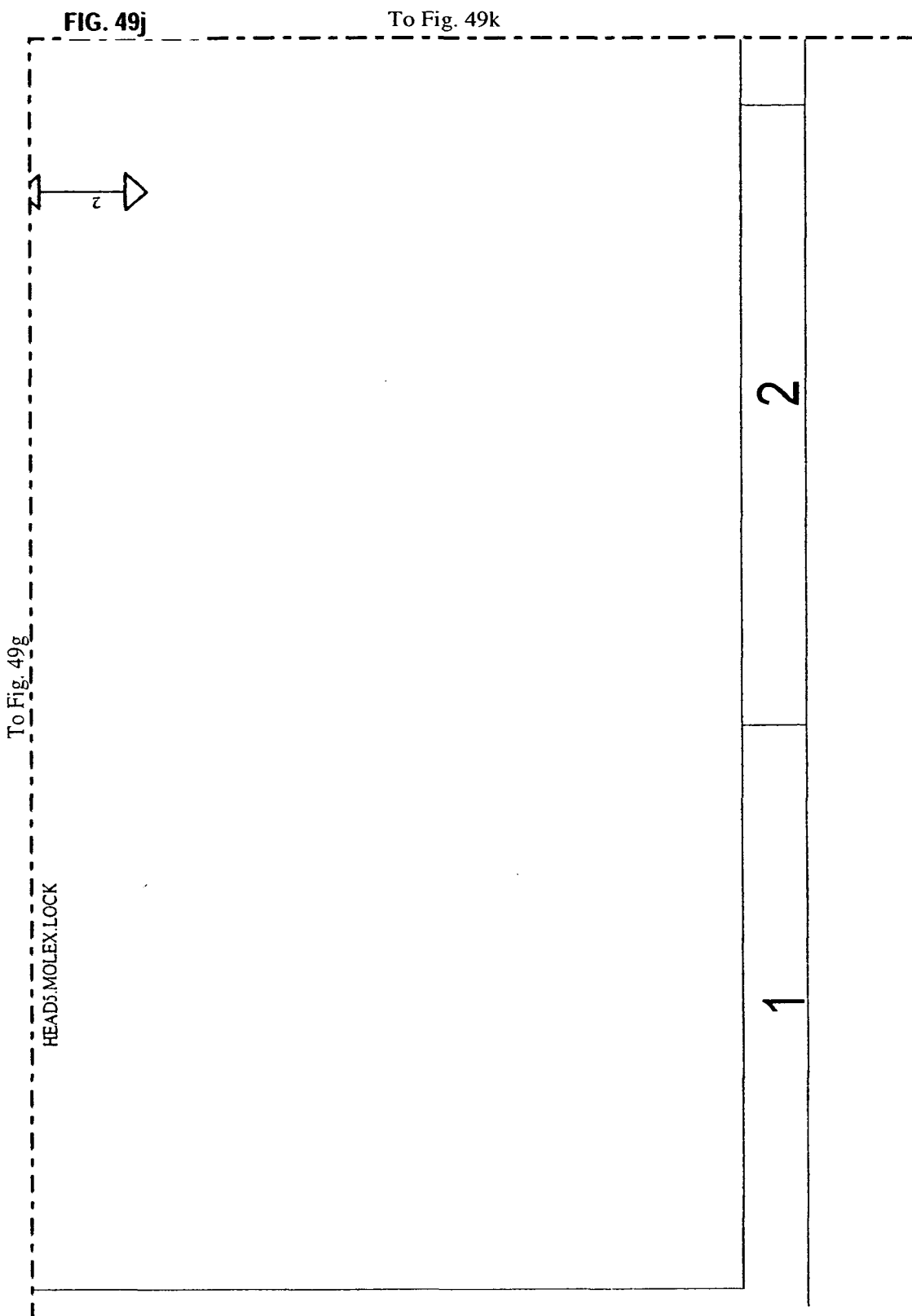


FIG. 49i





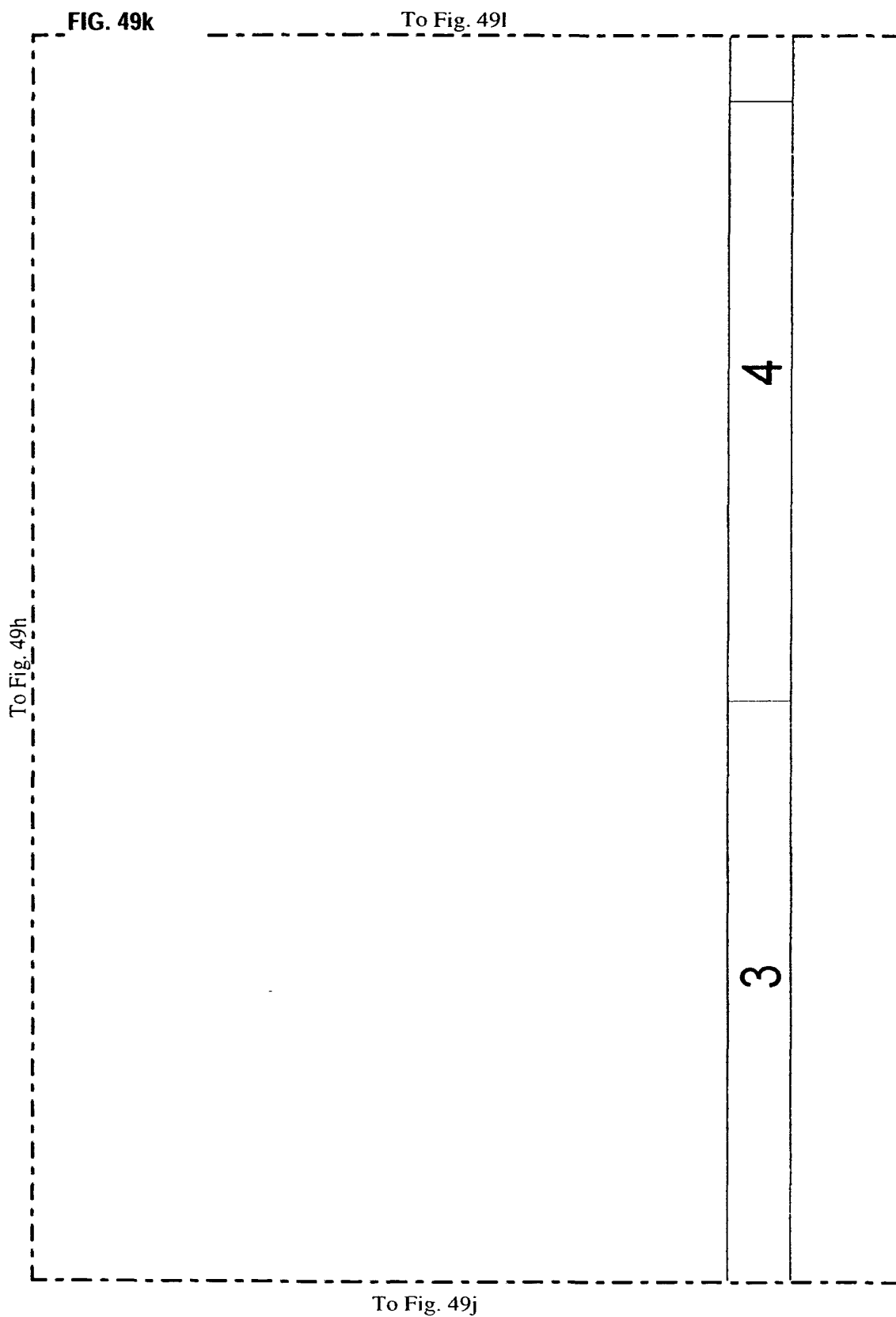
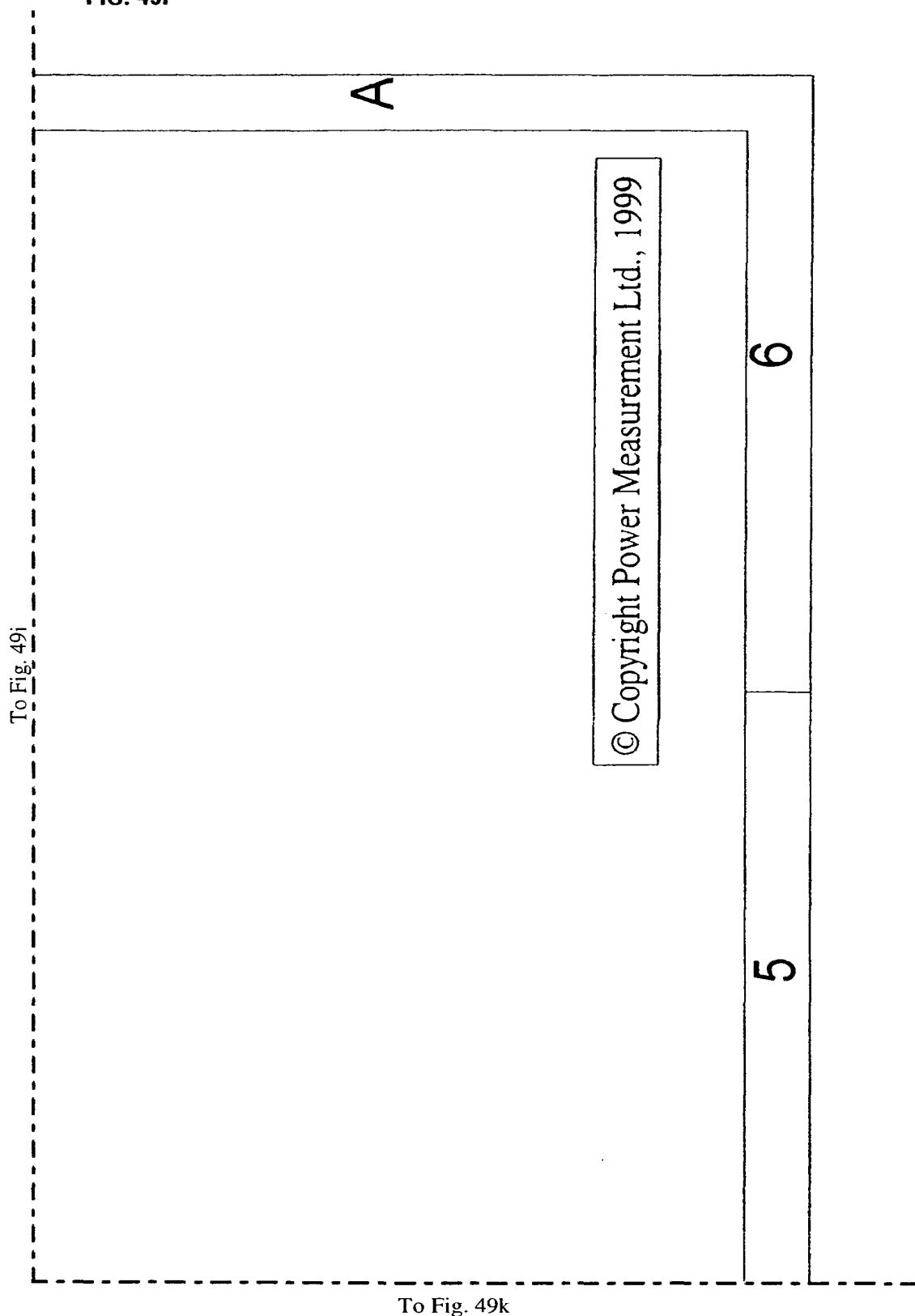
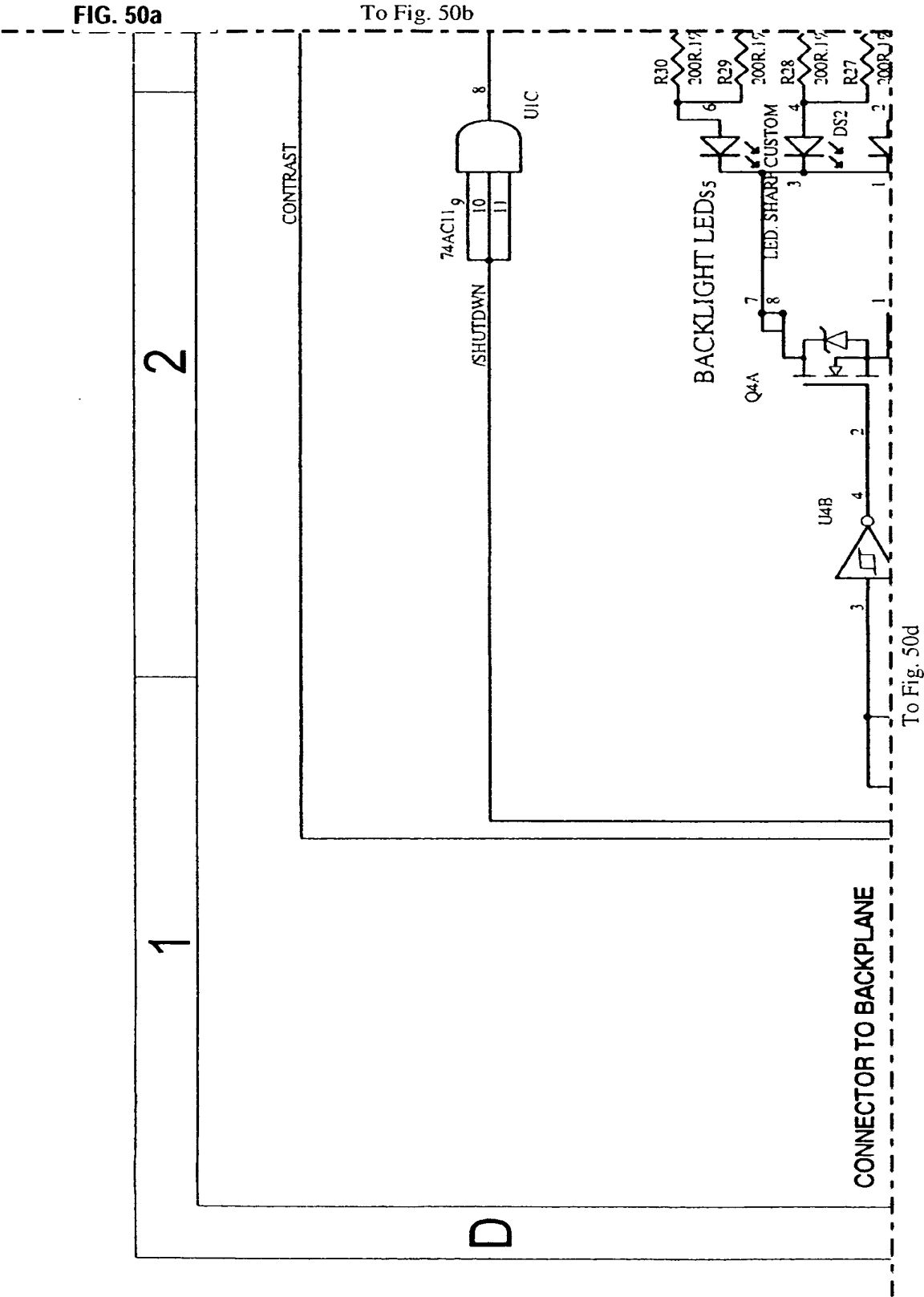


FIG. 49i





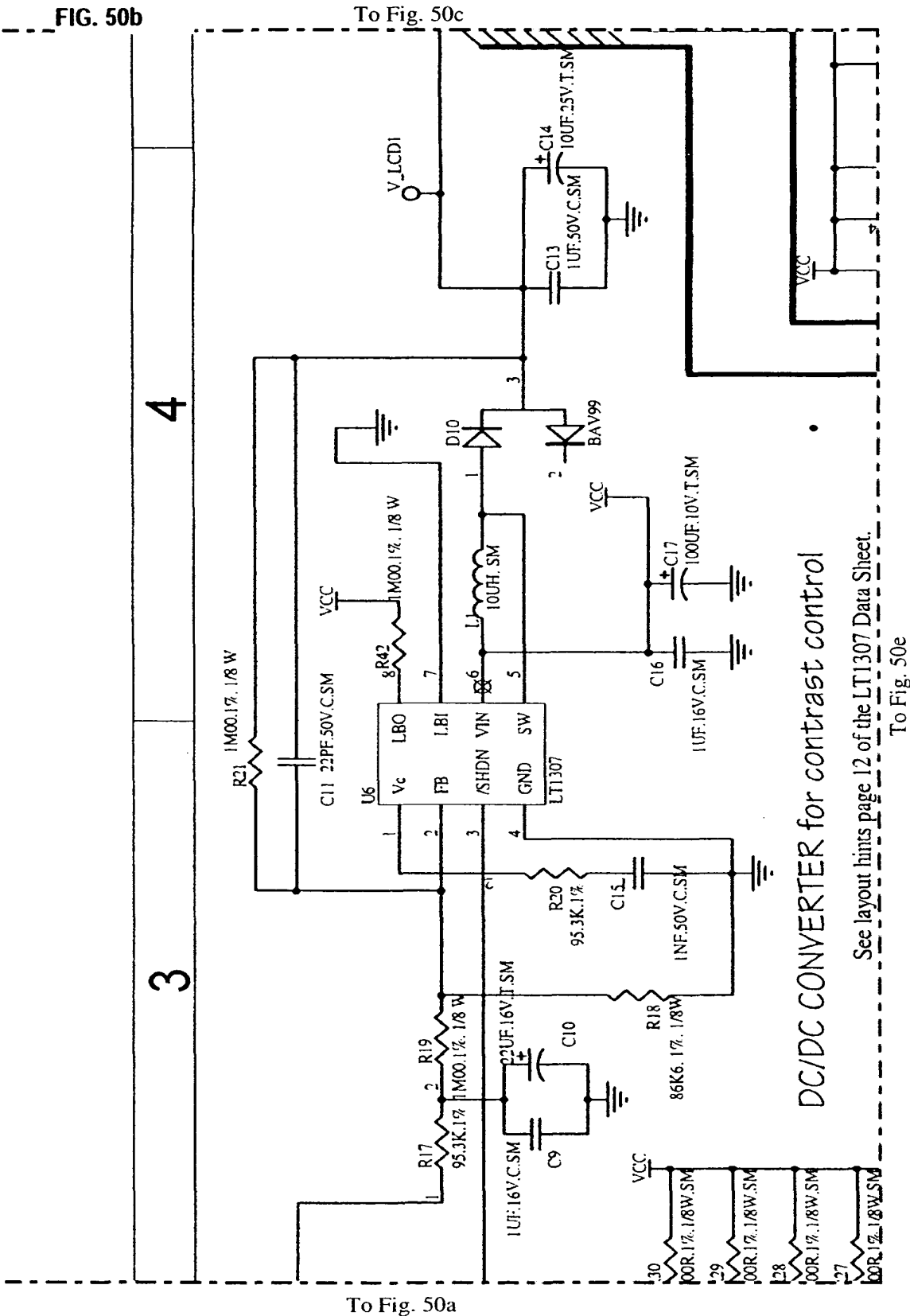
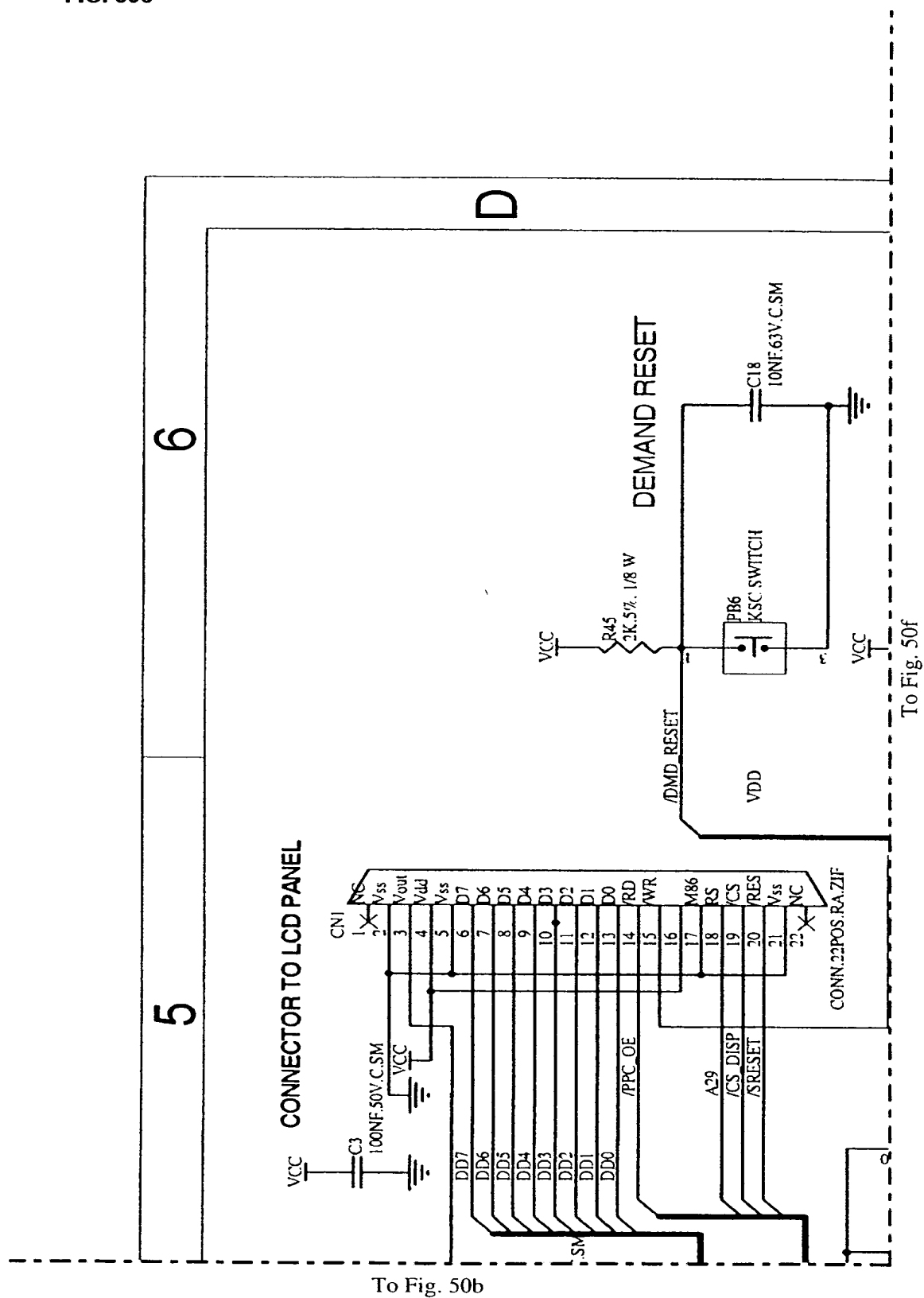
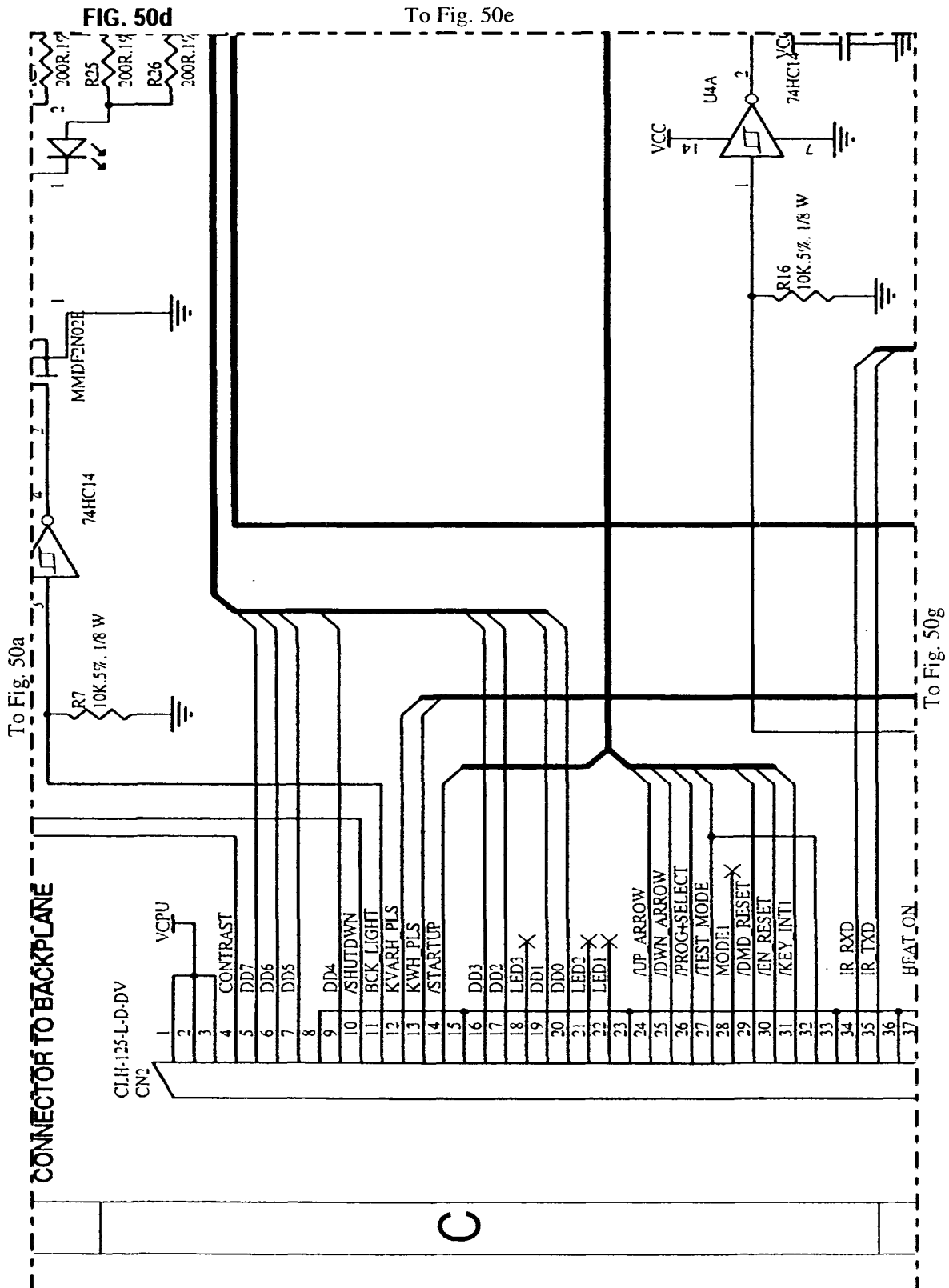
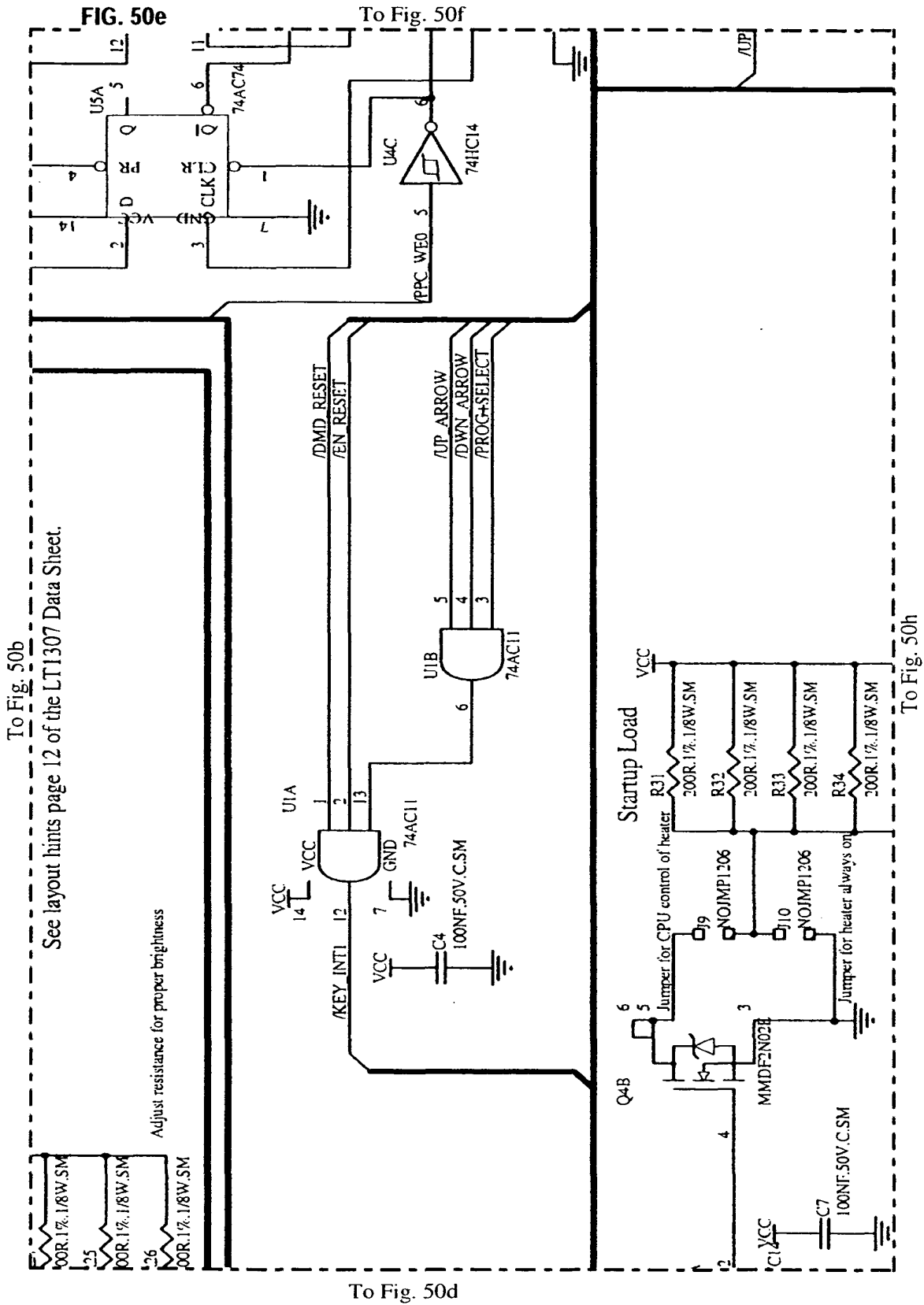
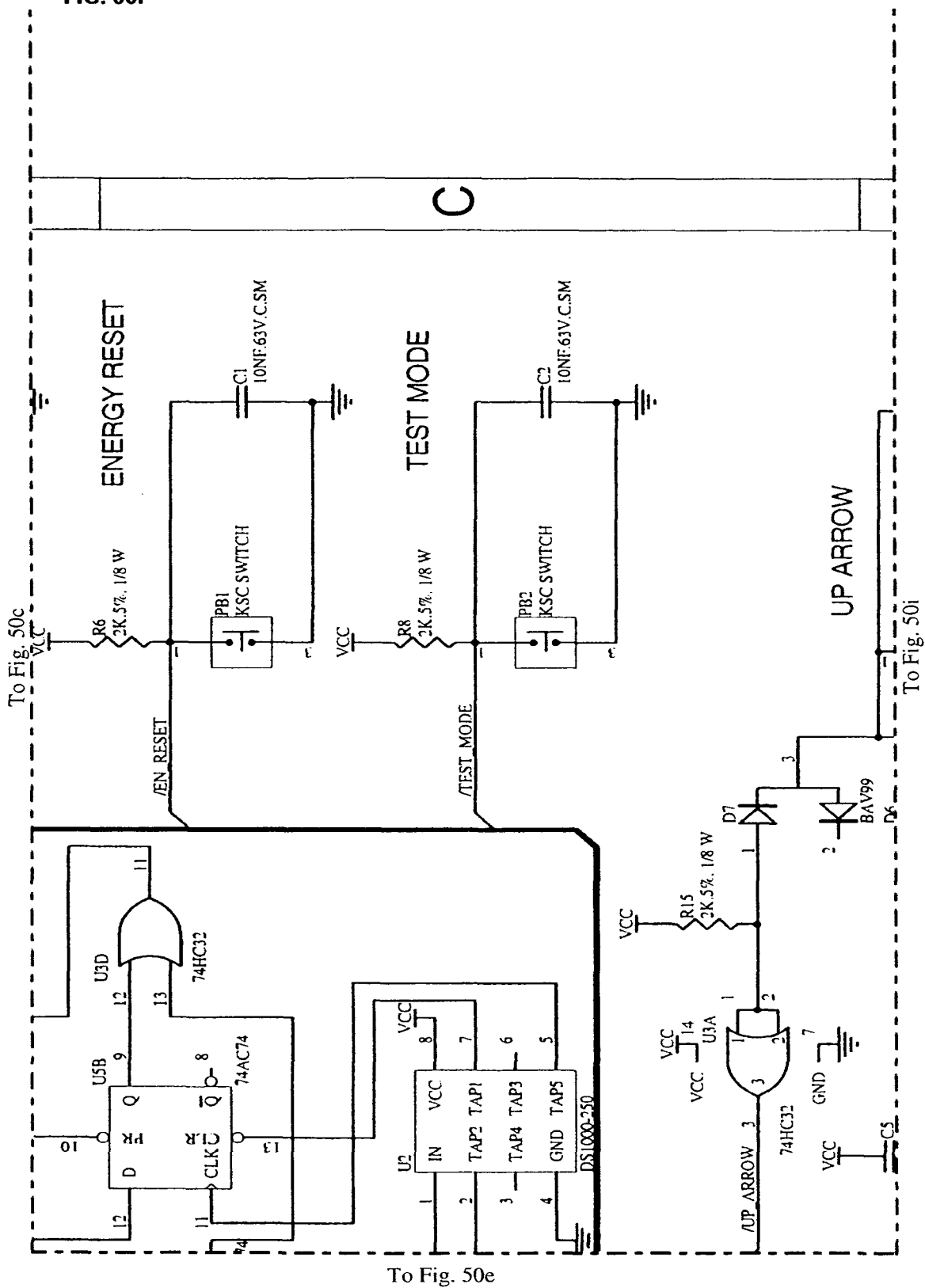


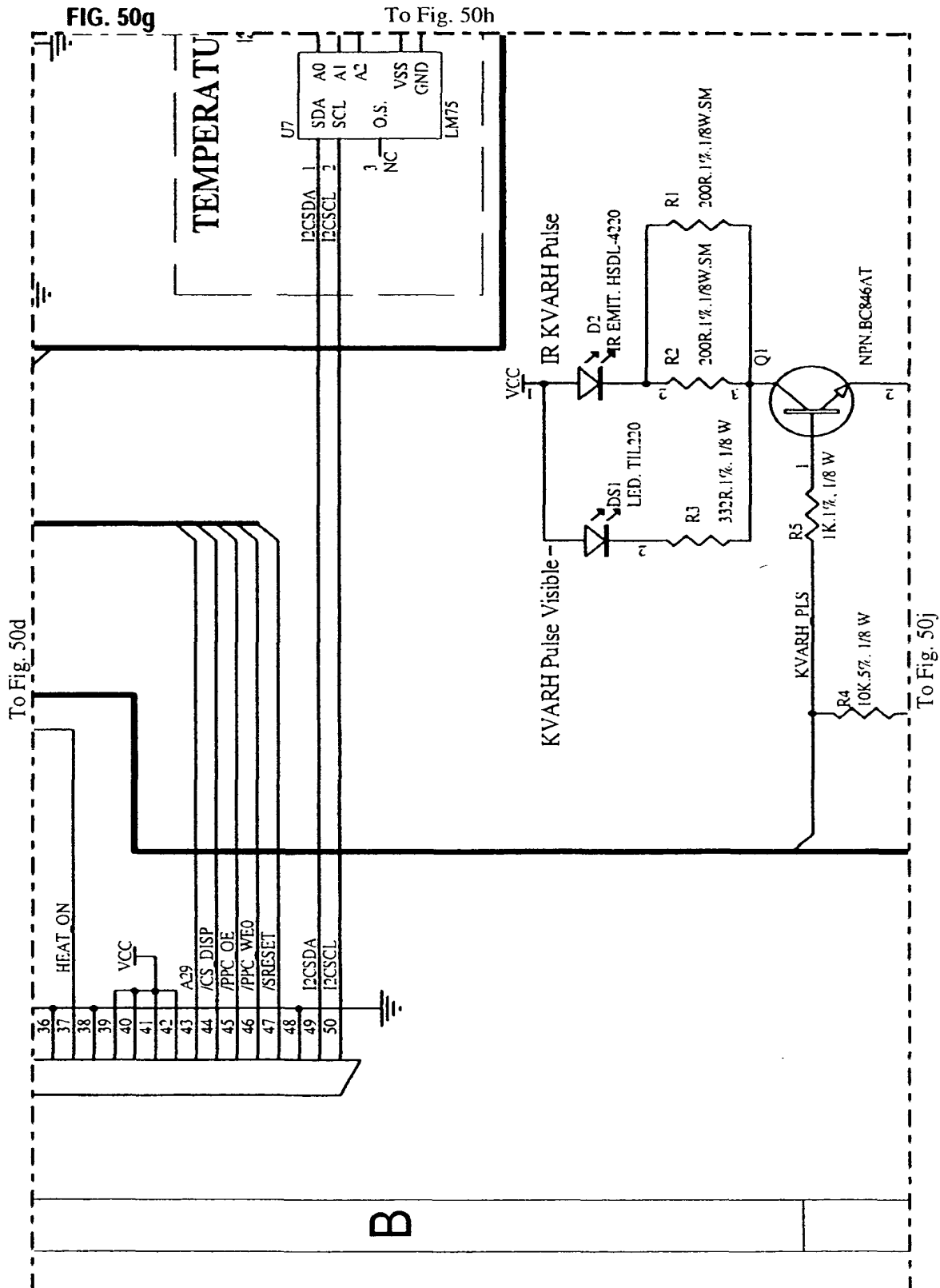
FIG. 50c











To Fig. 50i

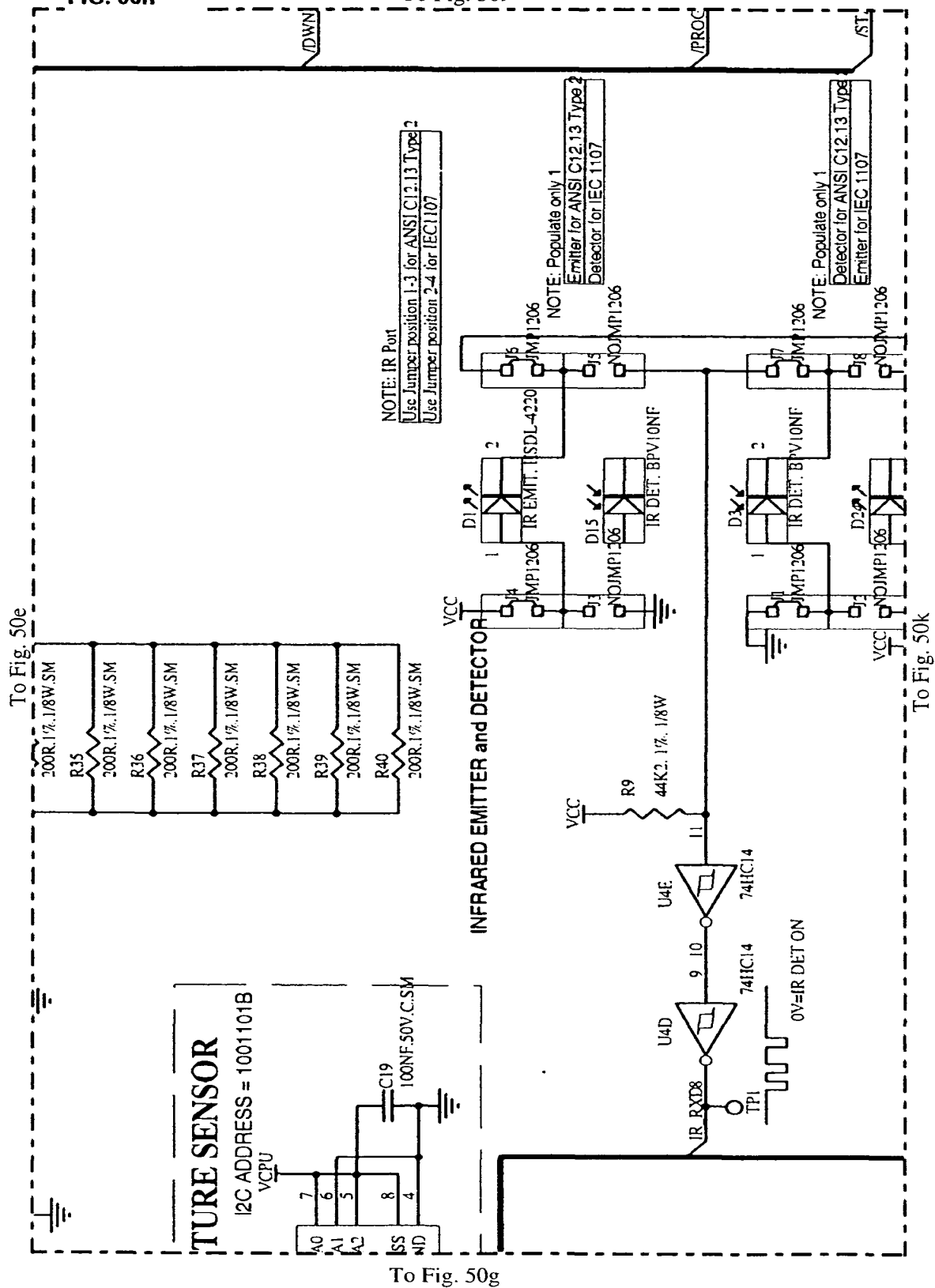


FIG. 50i

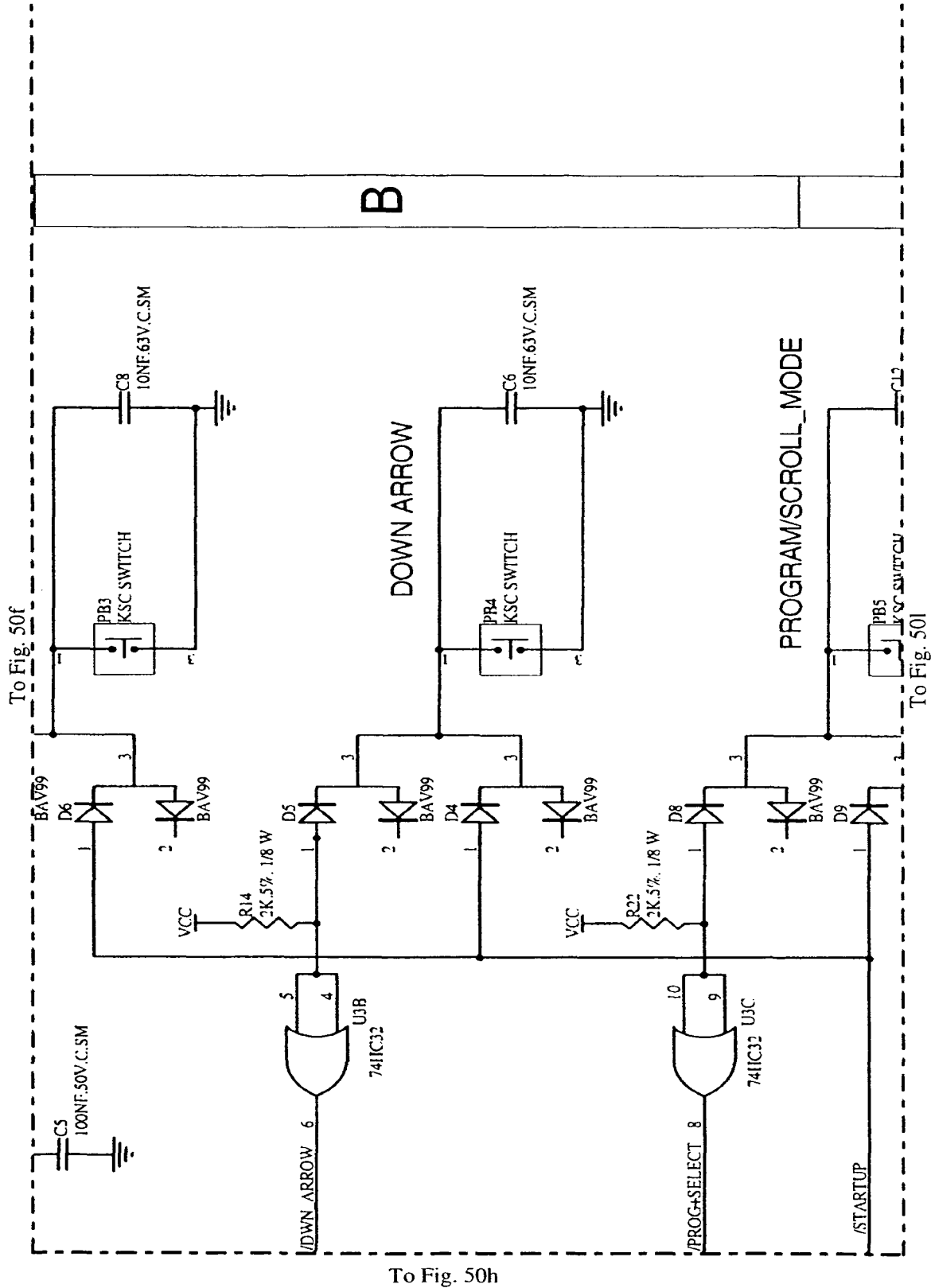
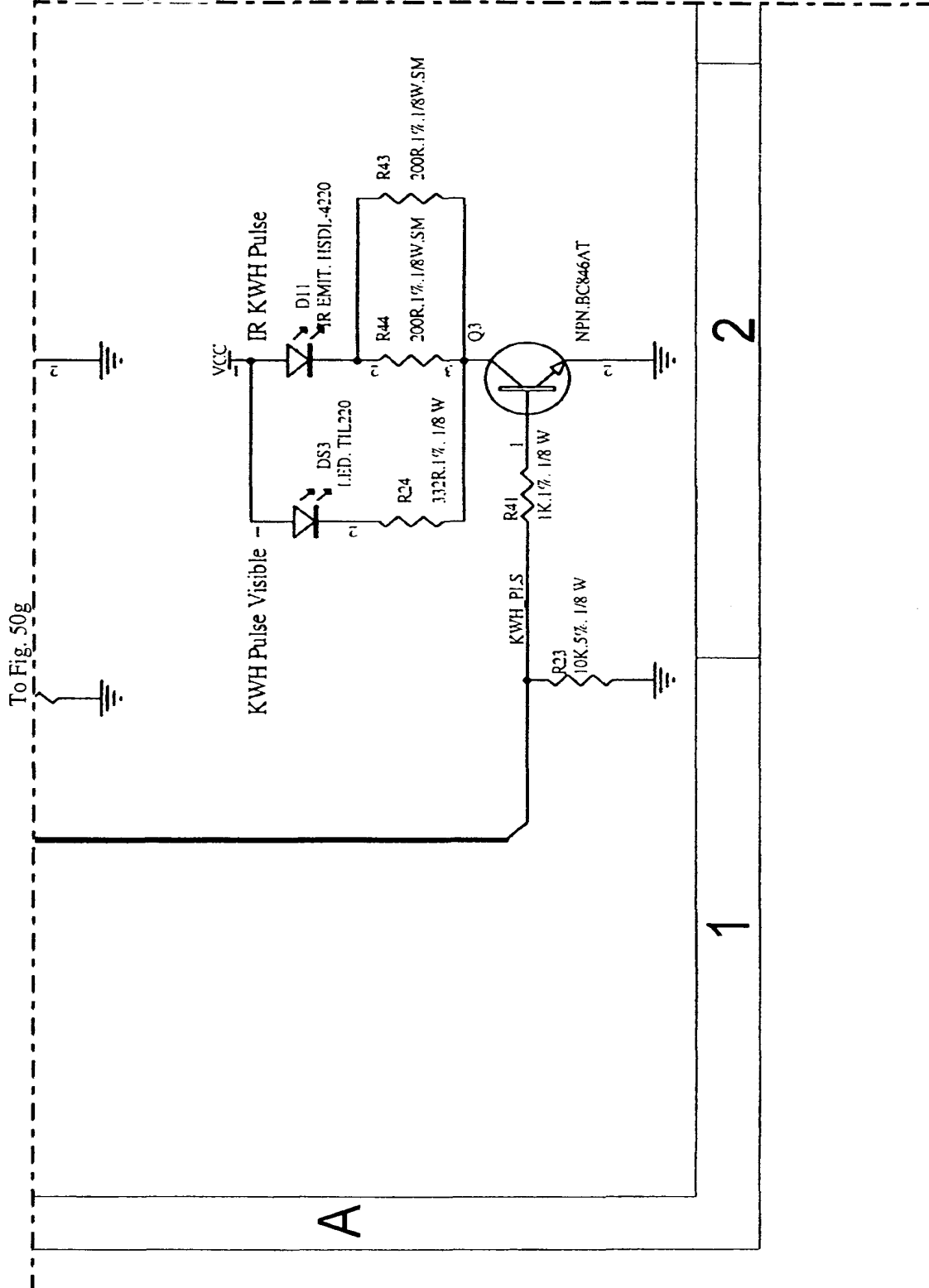


FIG. 50j

To Fig. 50k



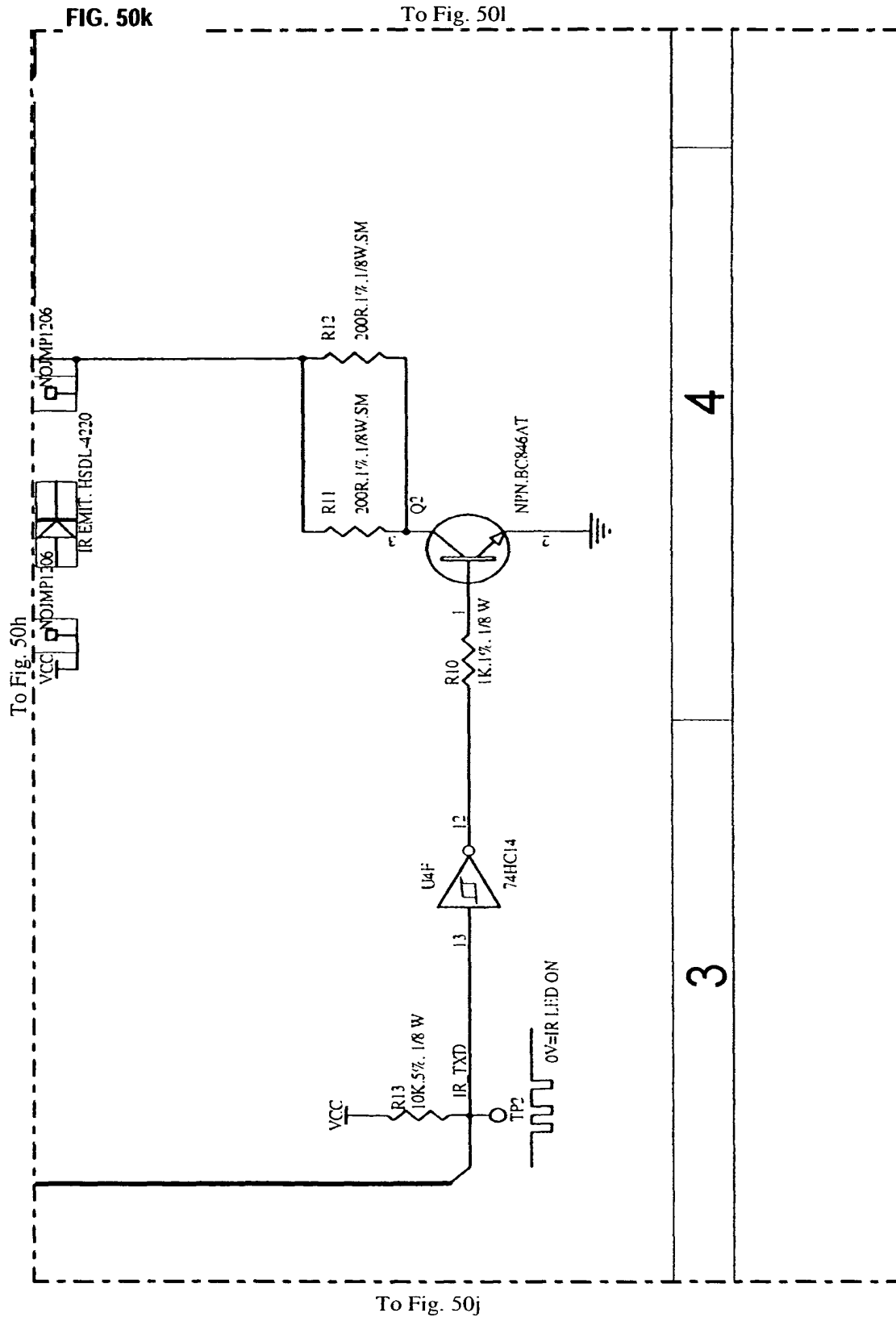
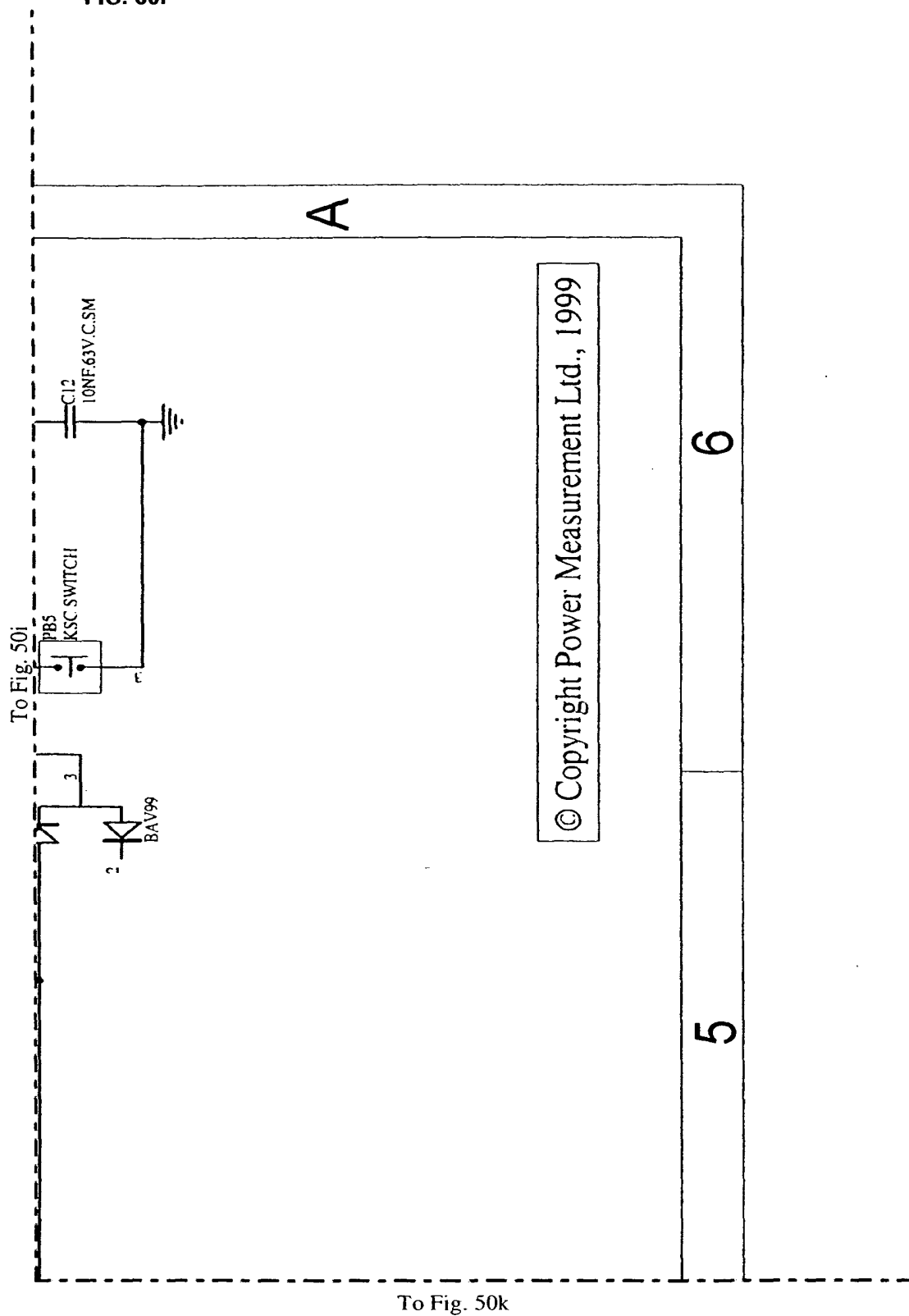
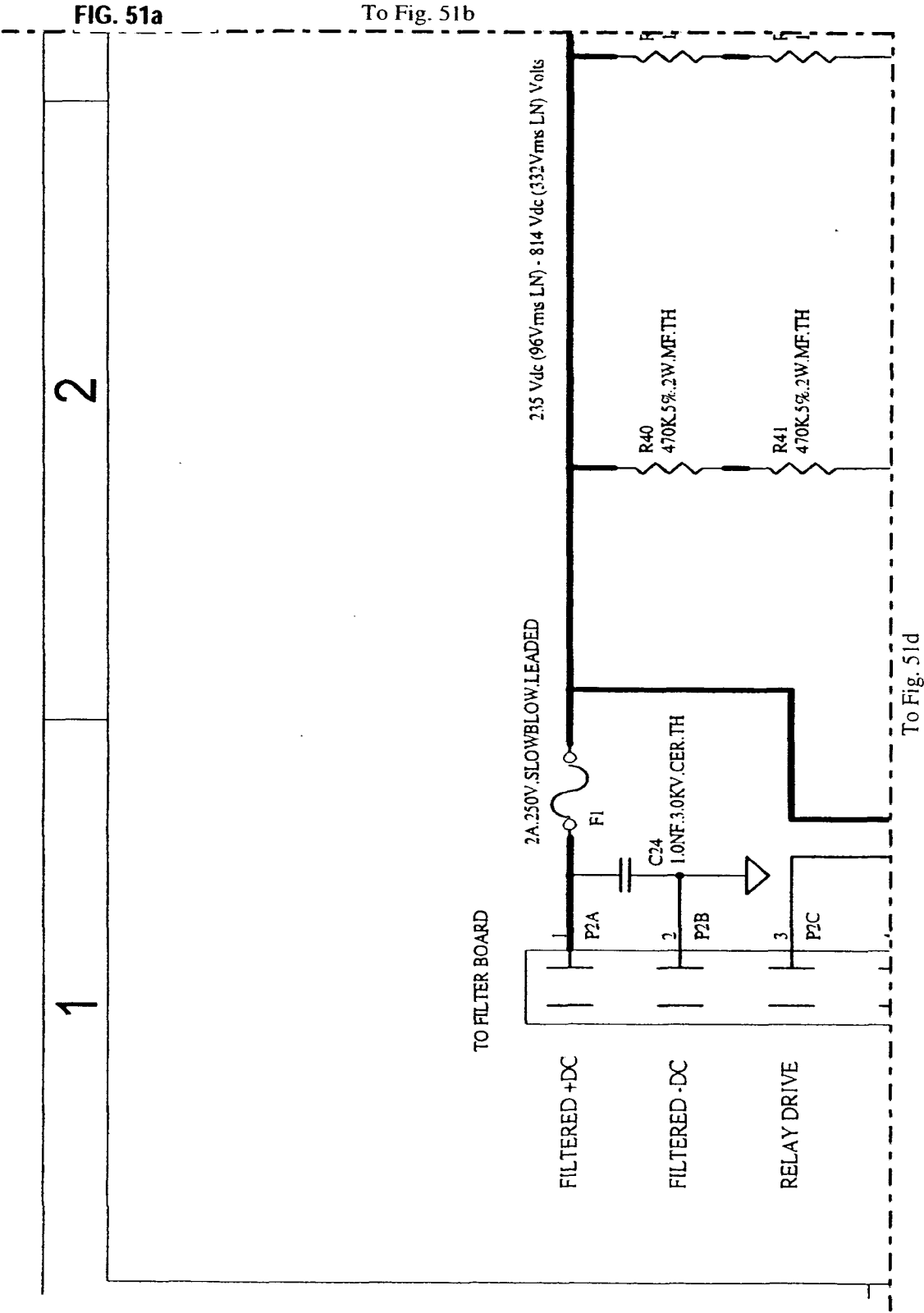


FIG. 50l





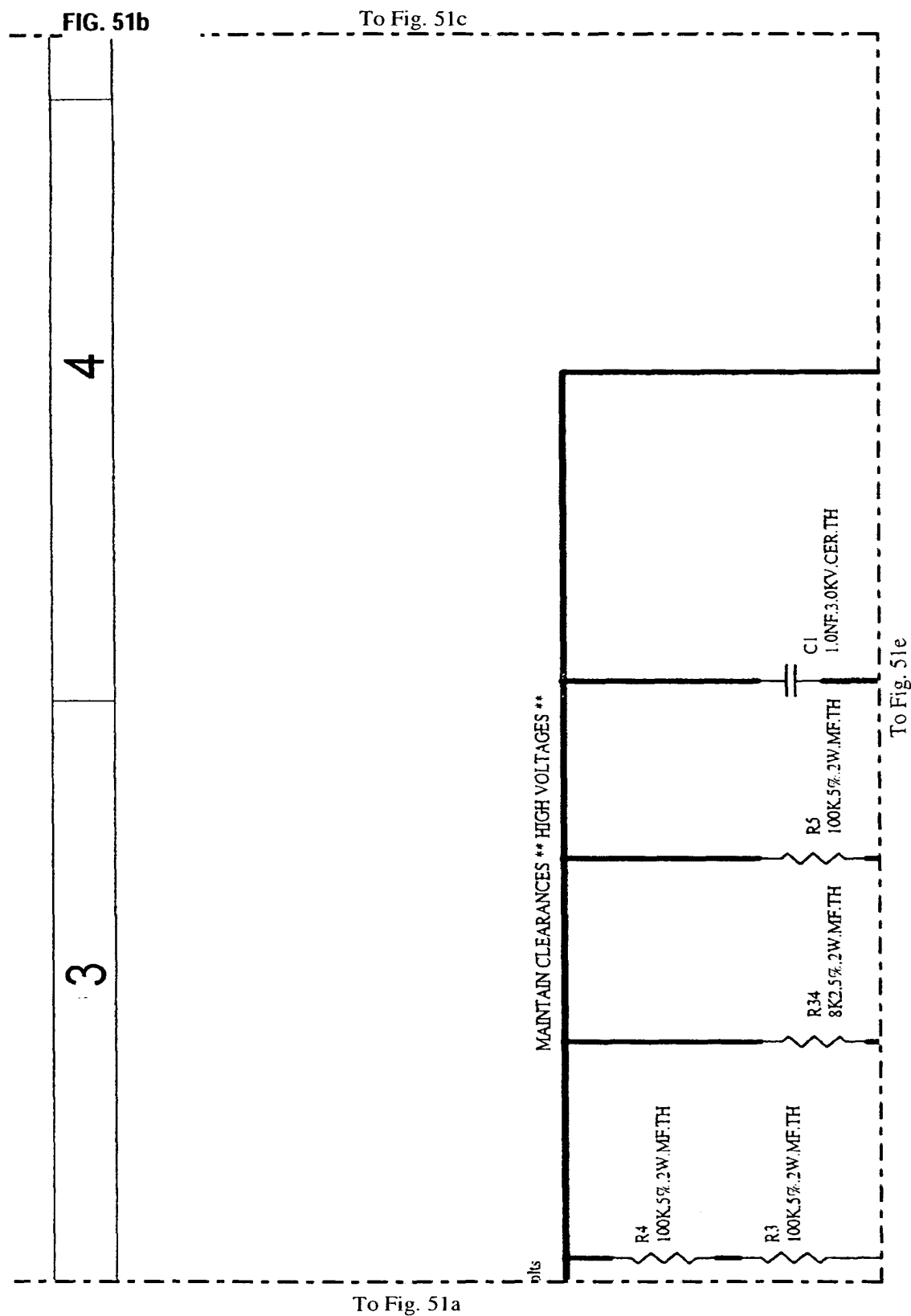
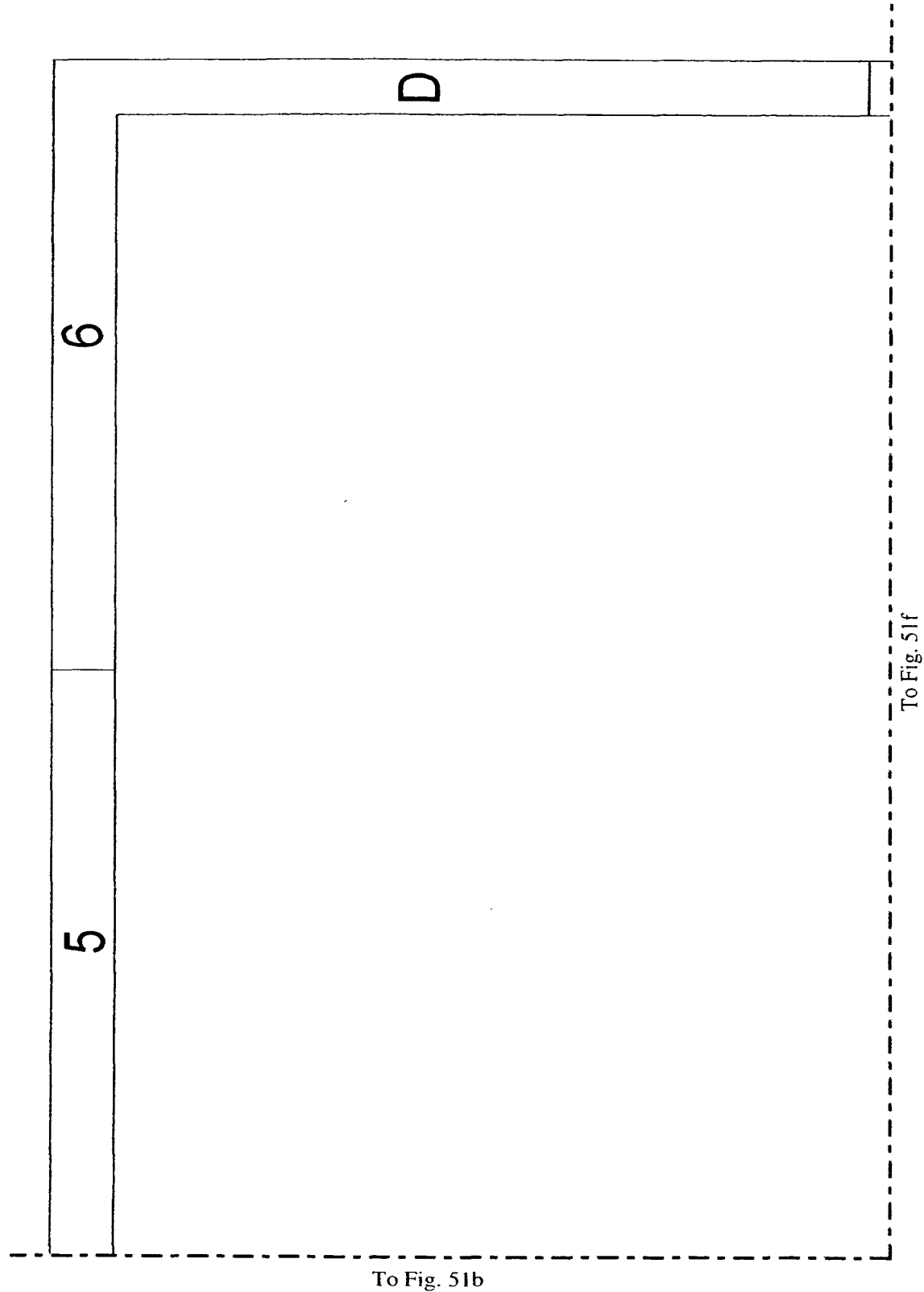
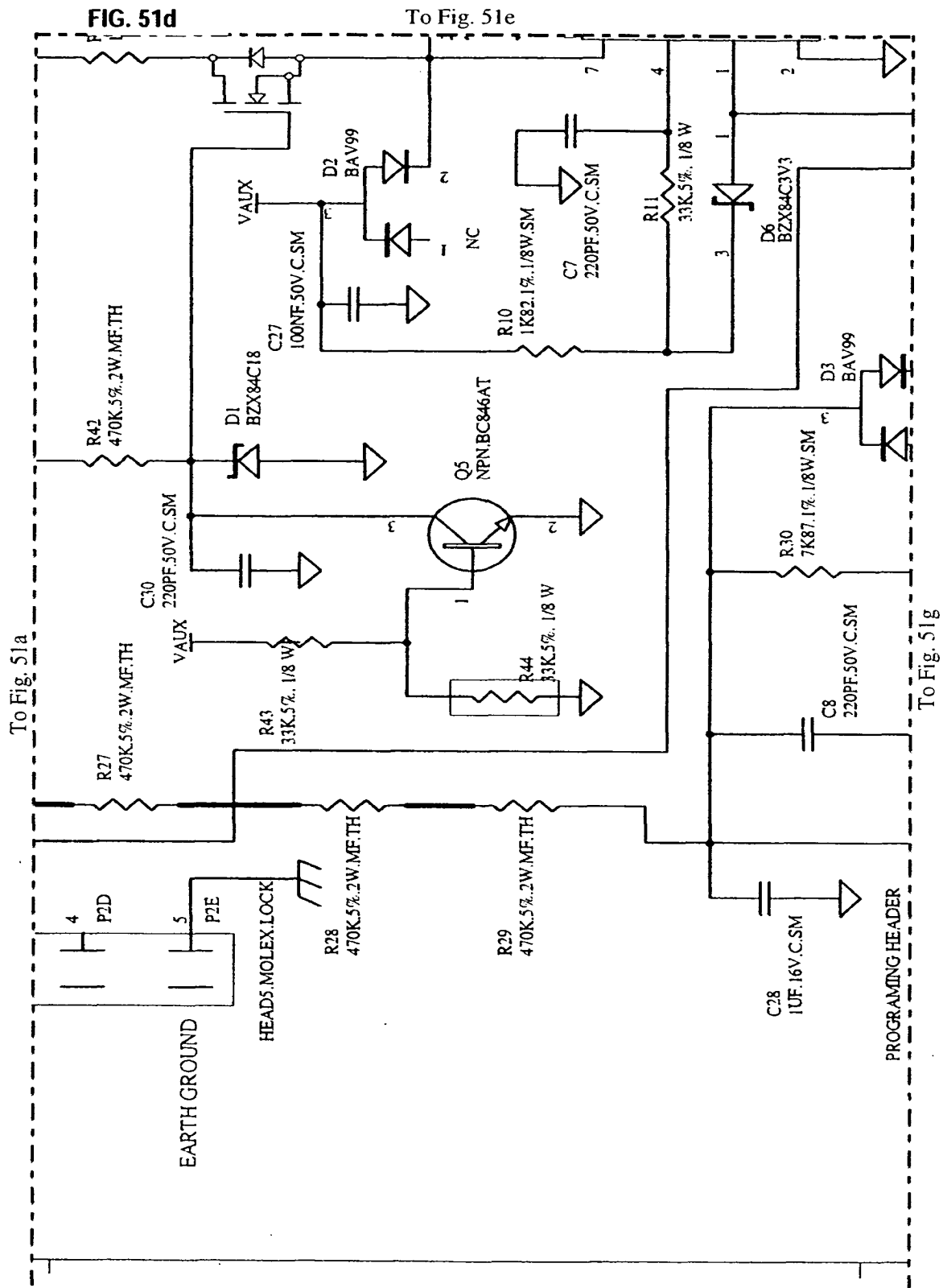


FIG. 51c





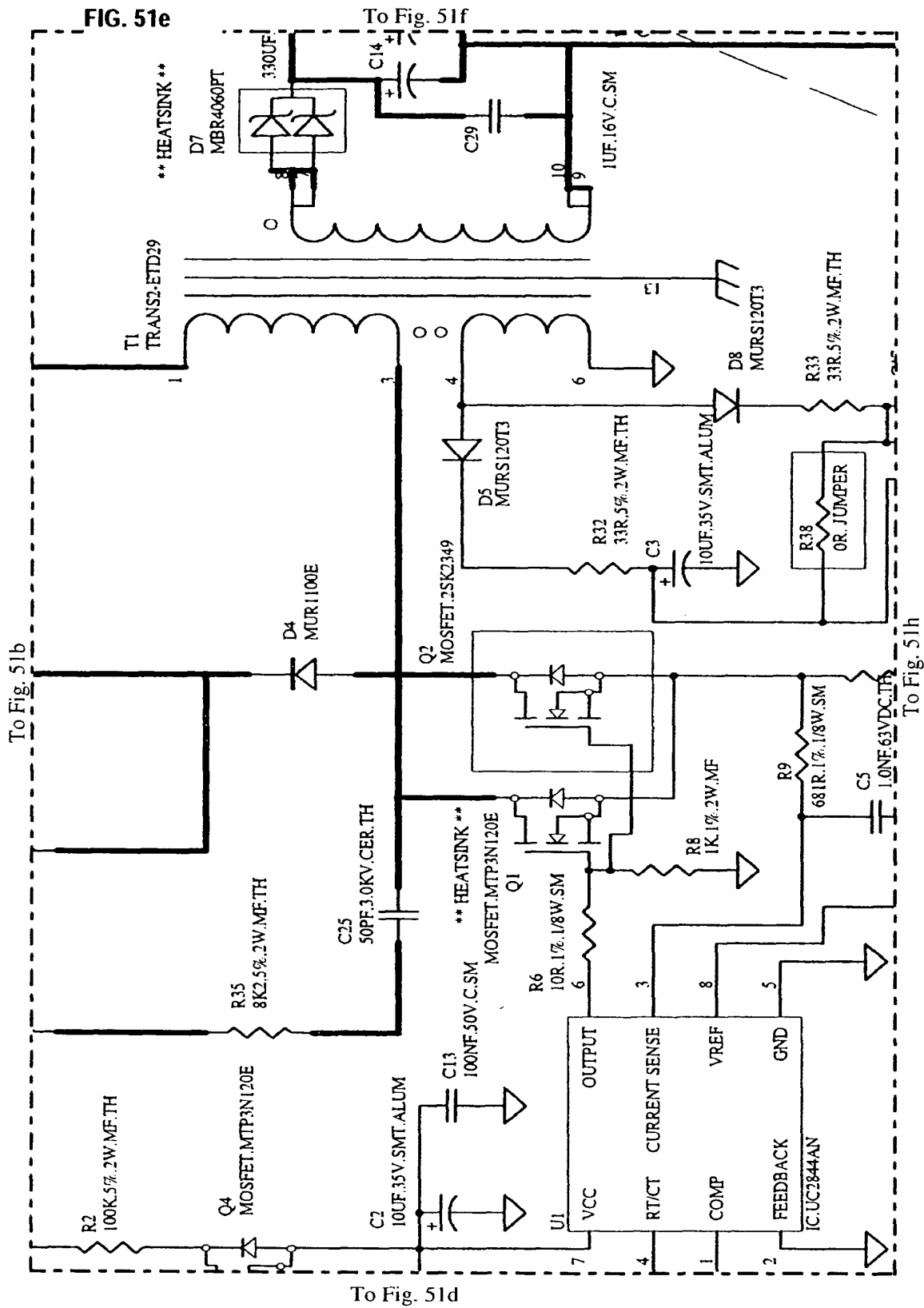
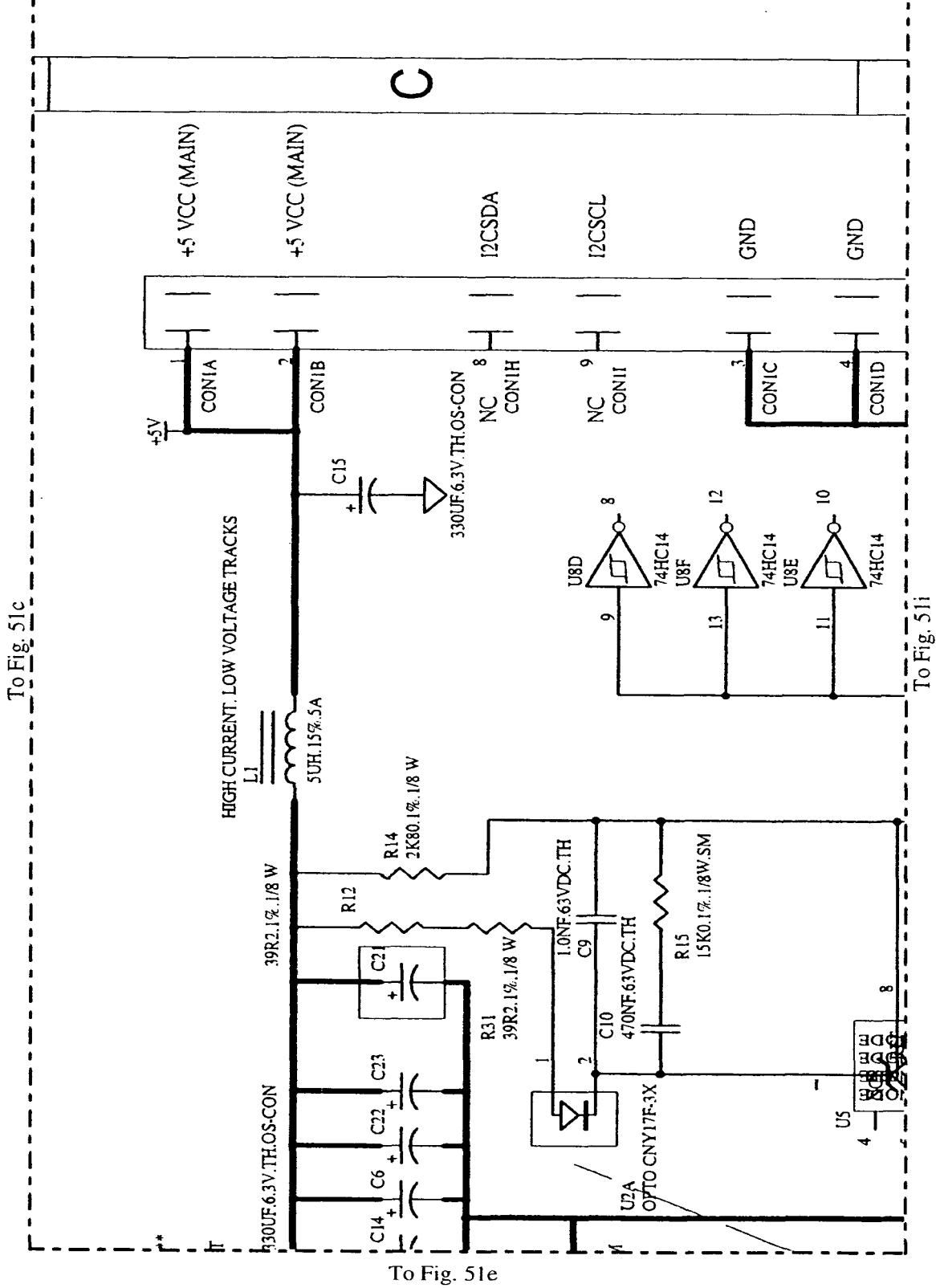
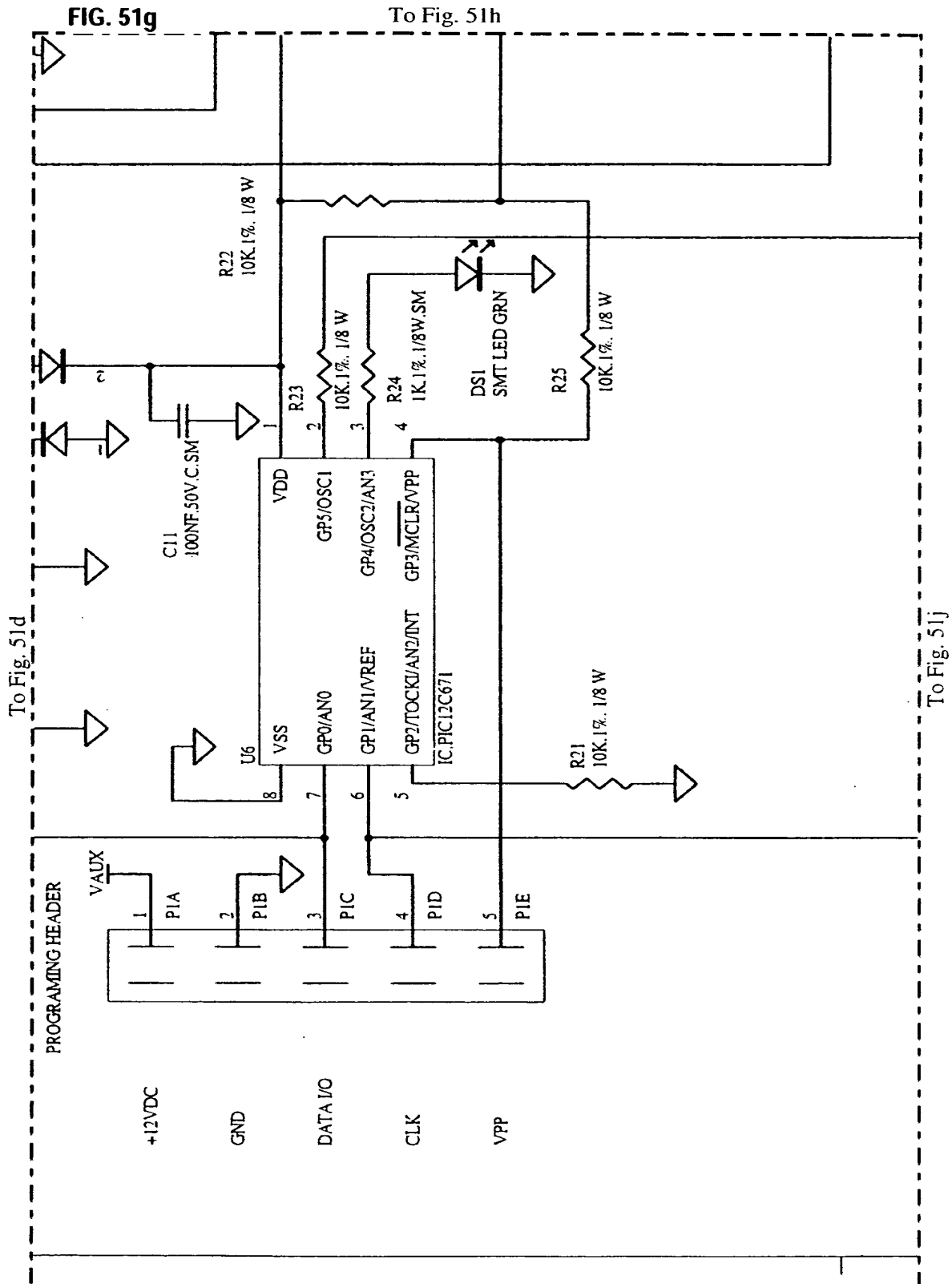


FIG. 51f





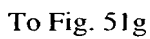
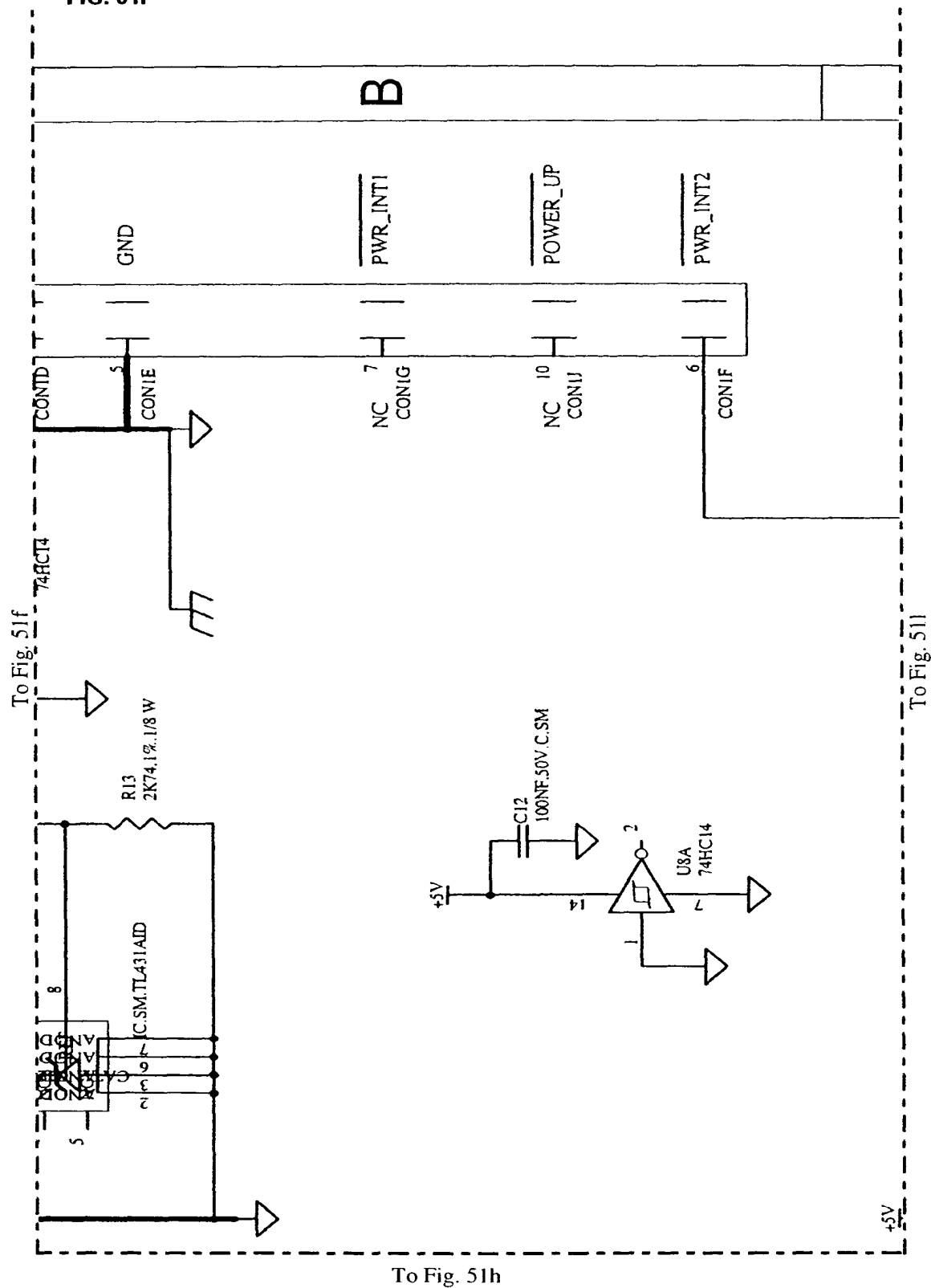
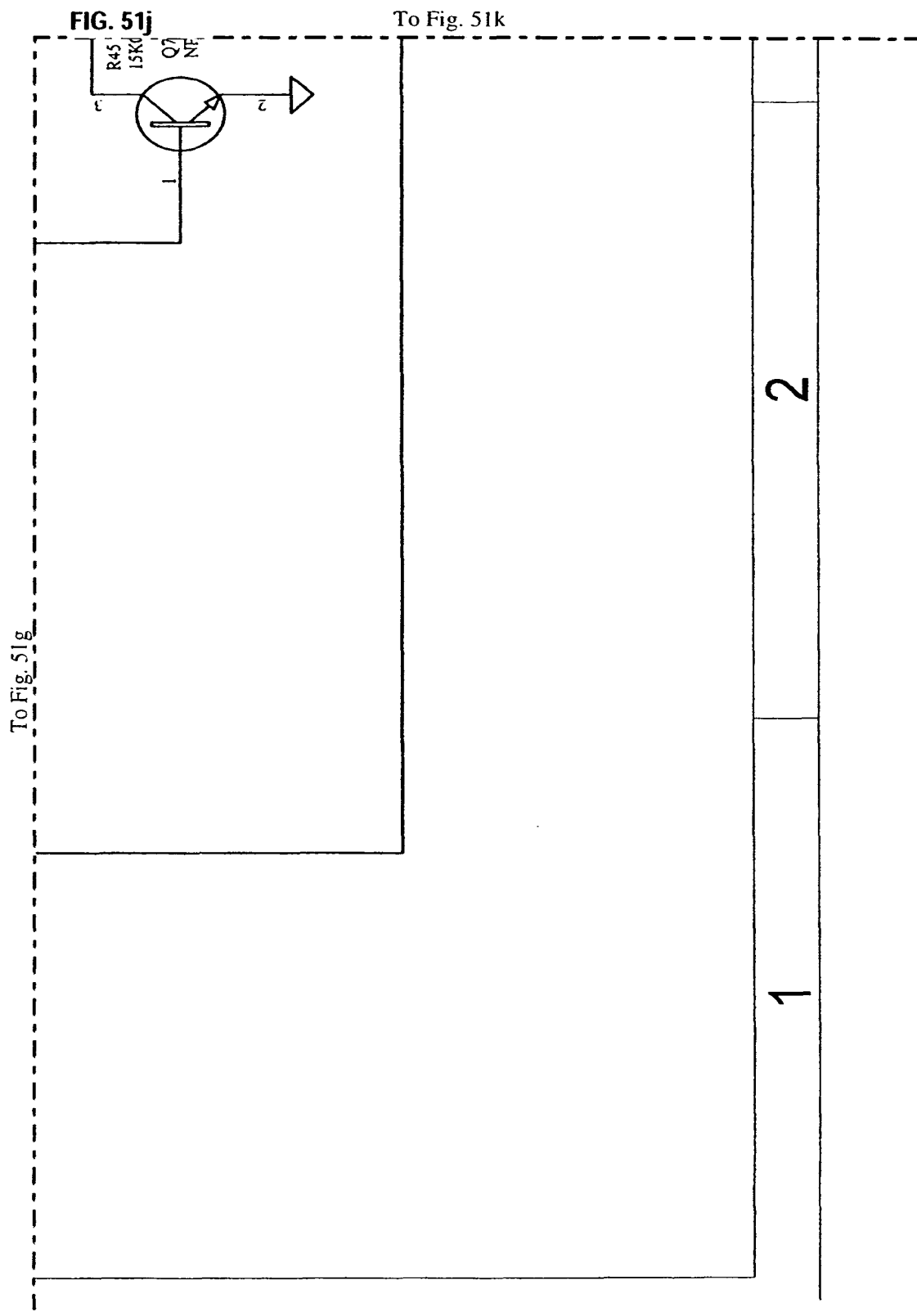


FIG. 51i





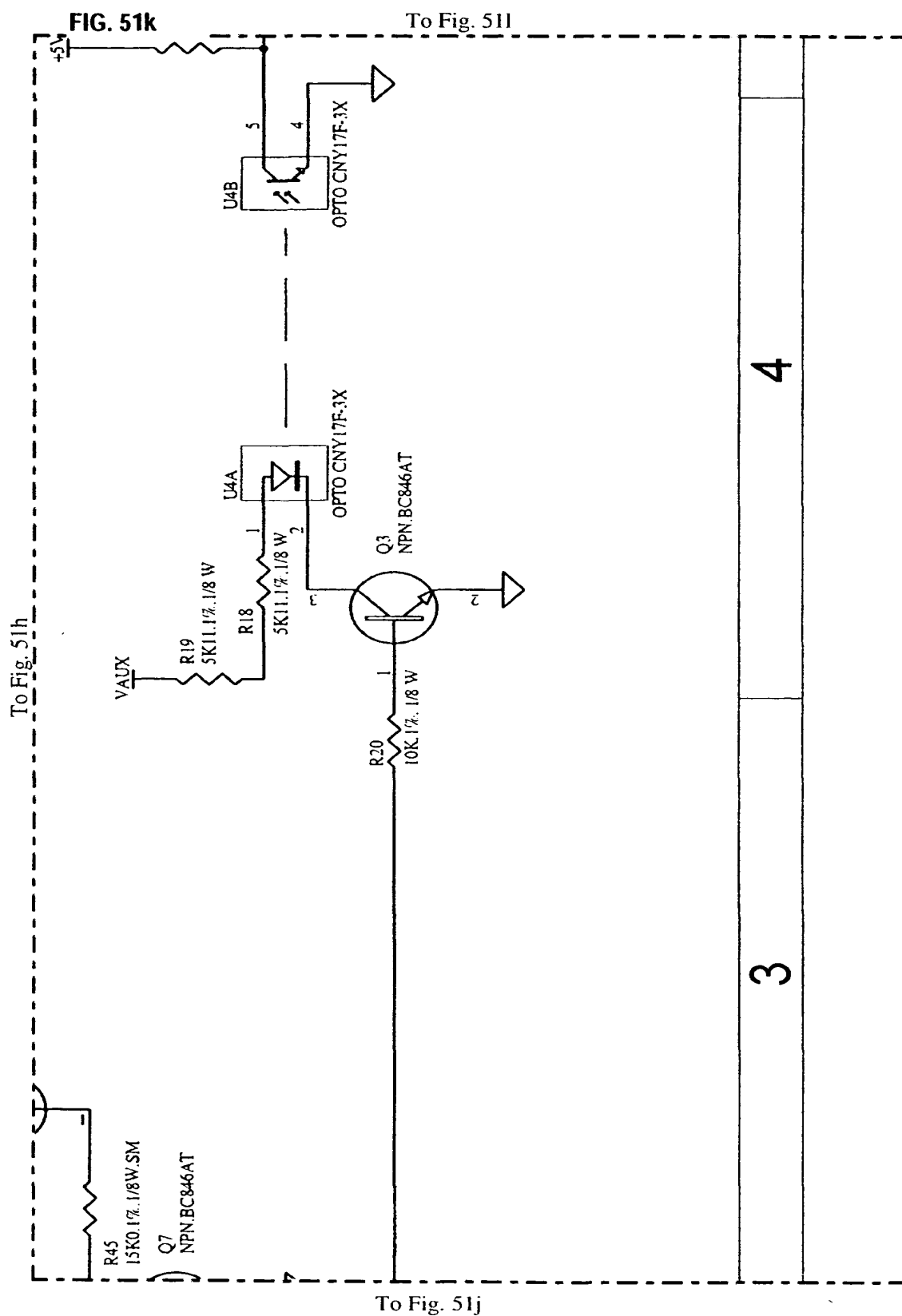
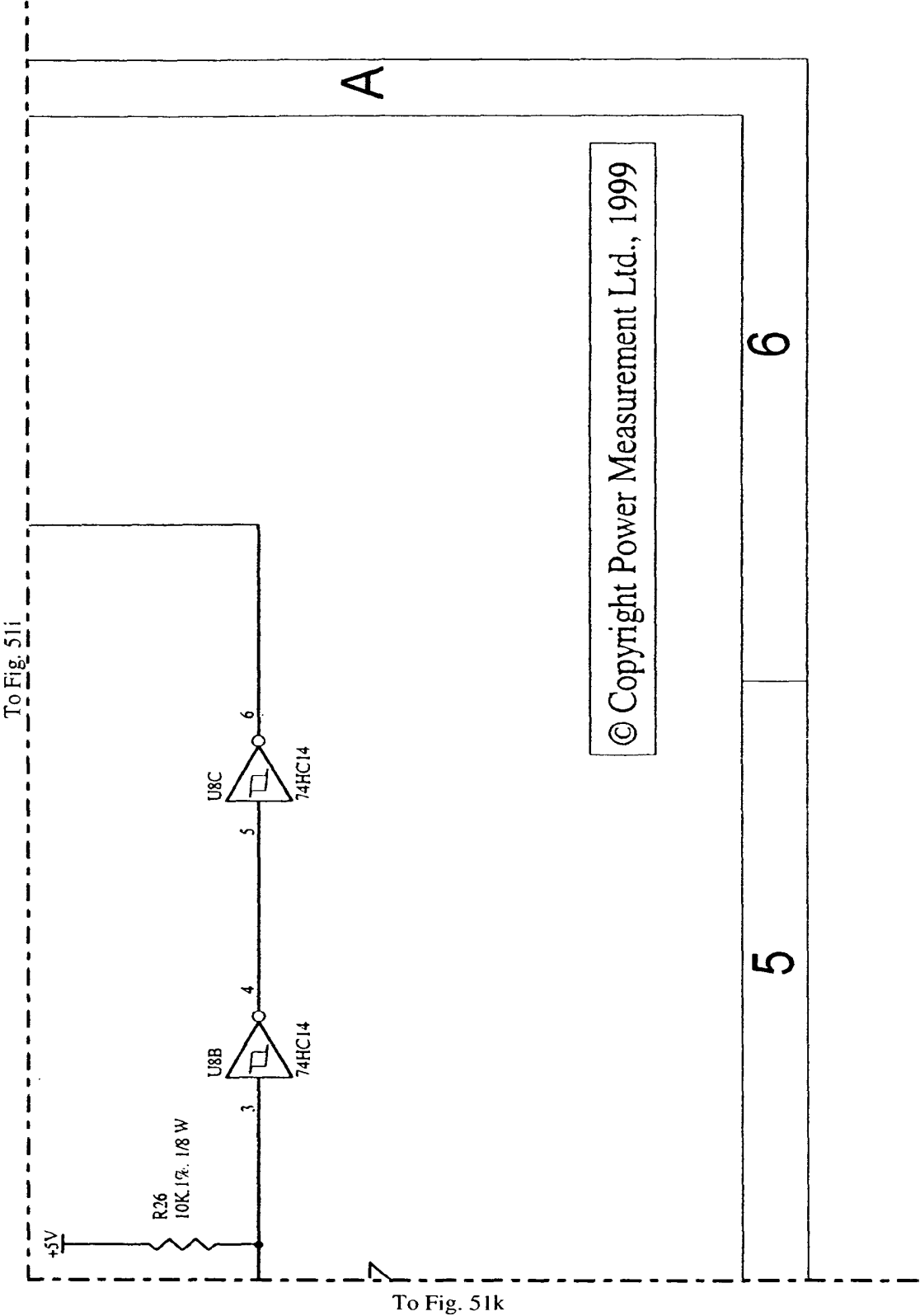
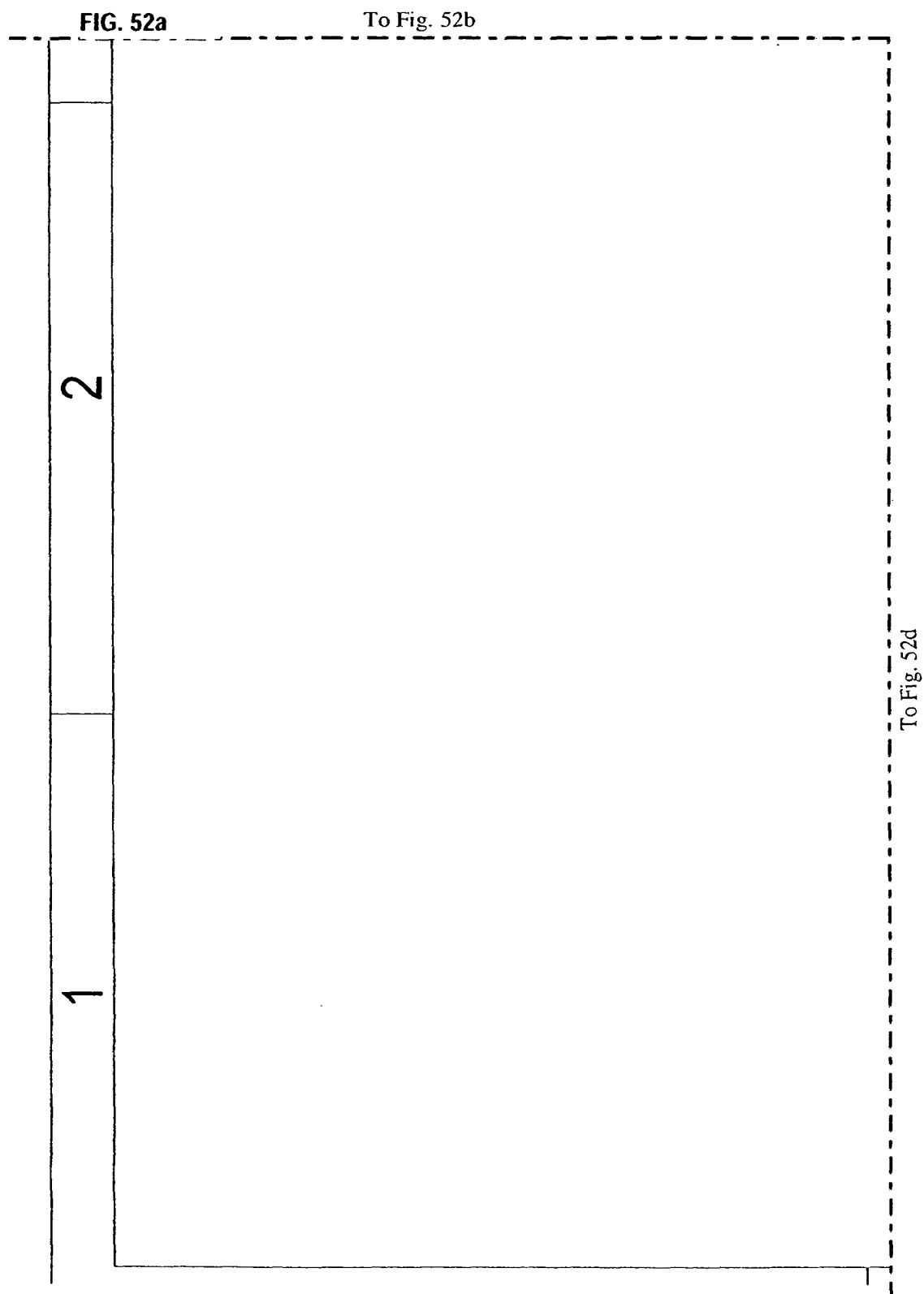


FIG. 51l





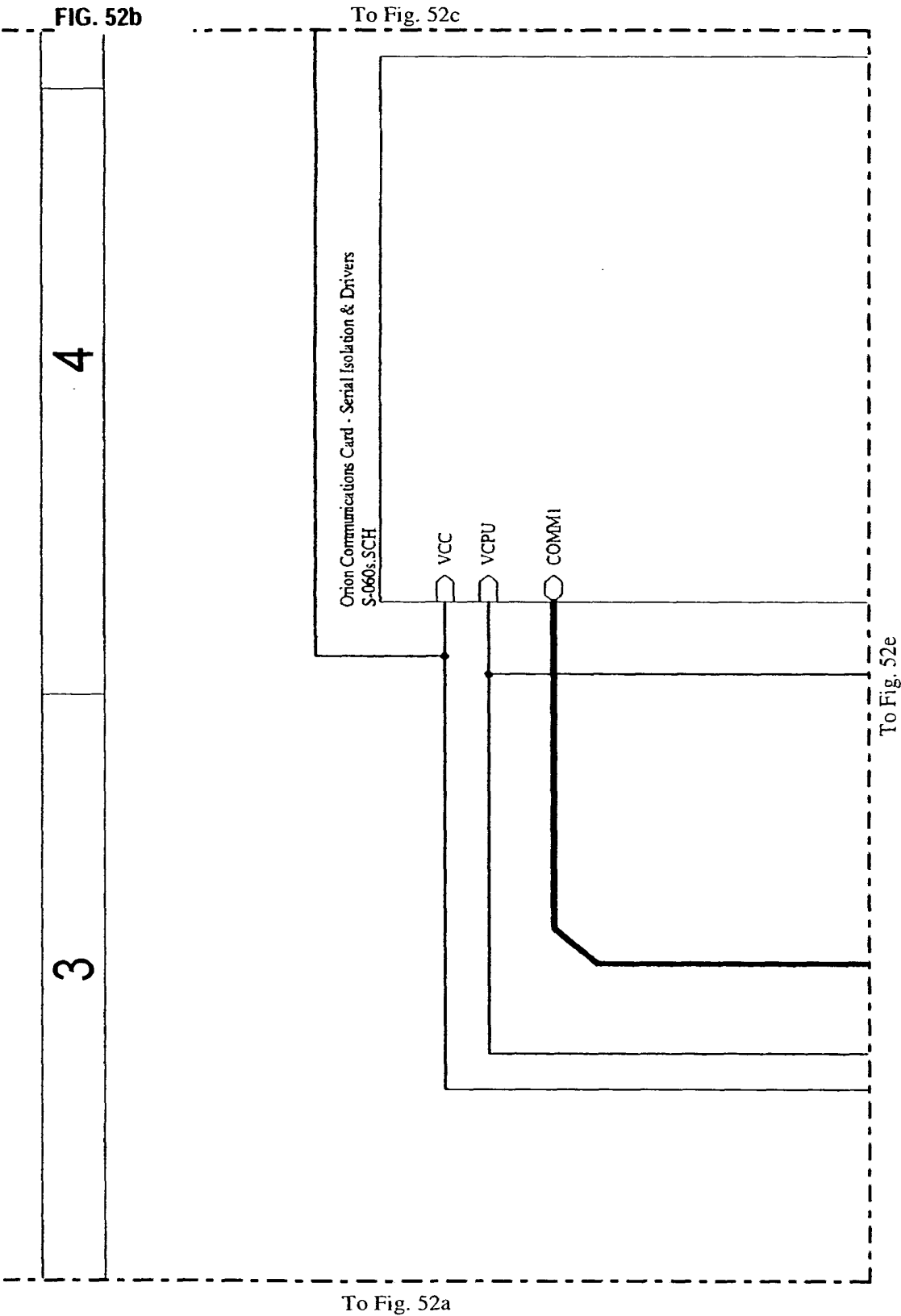
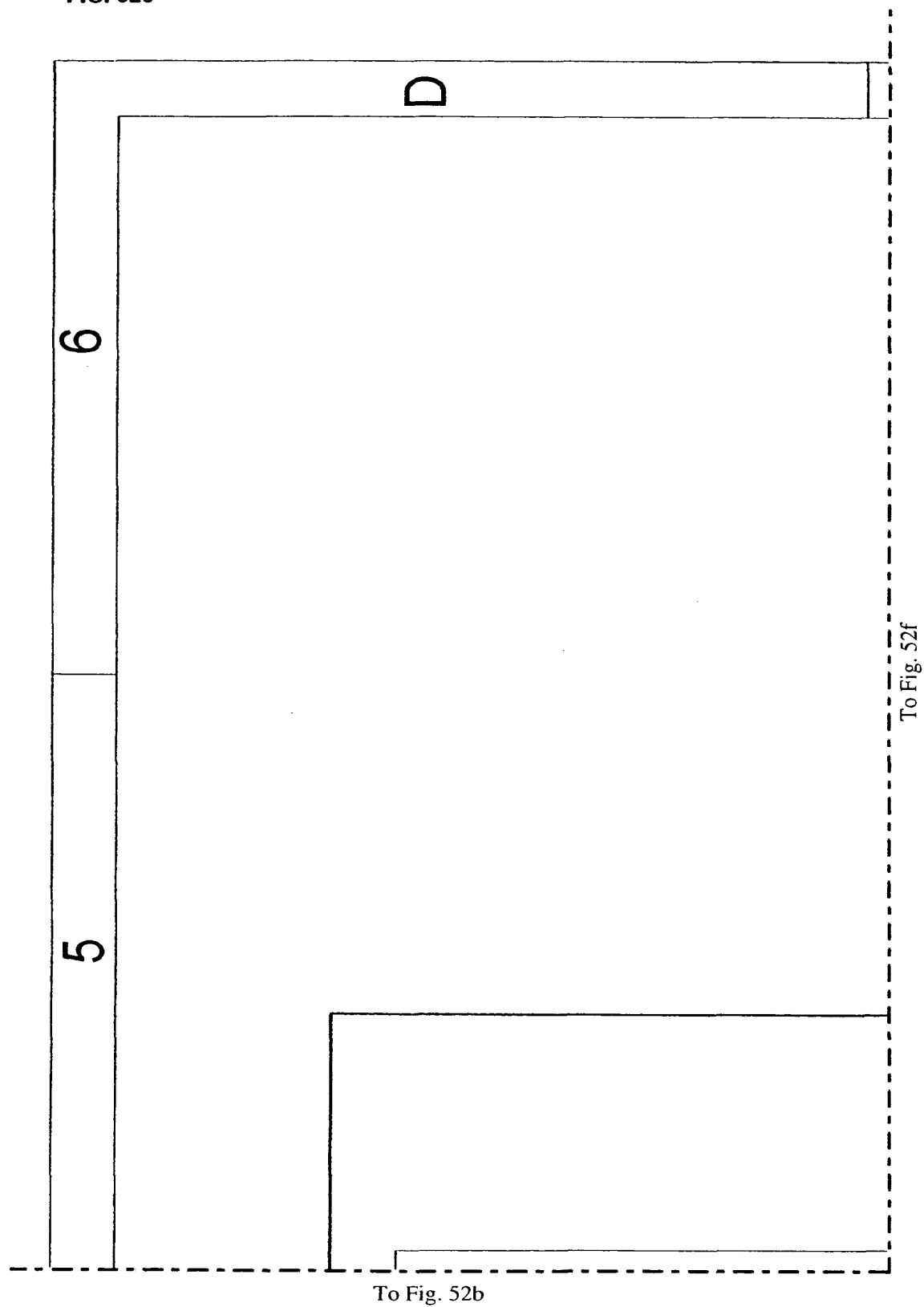
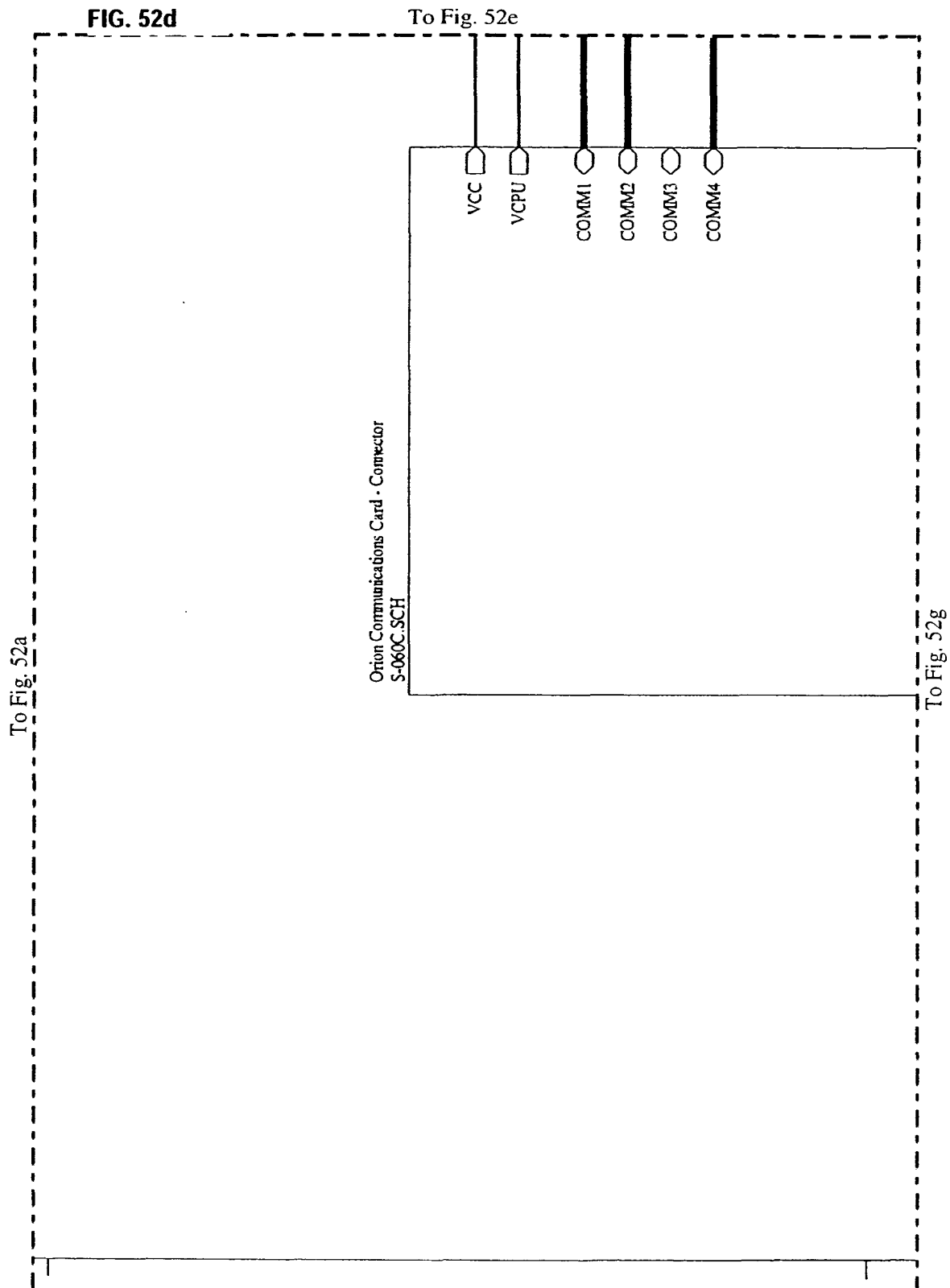


FIG. 52c





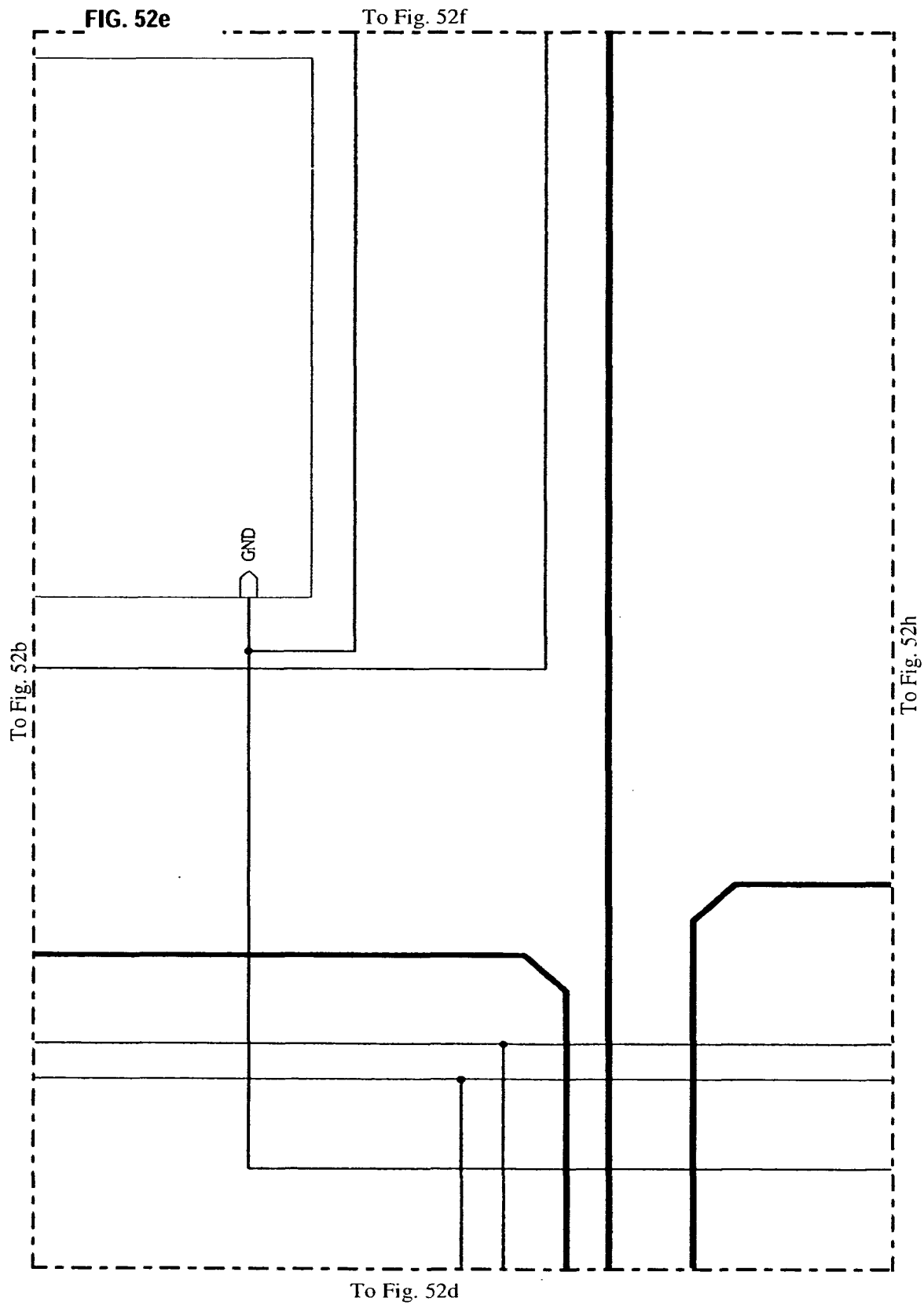
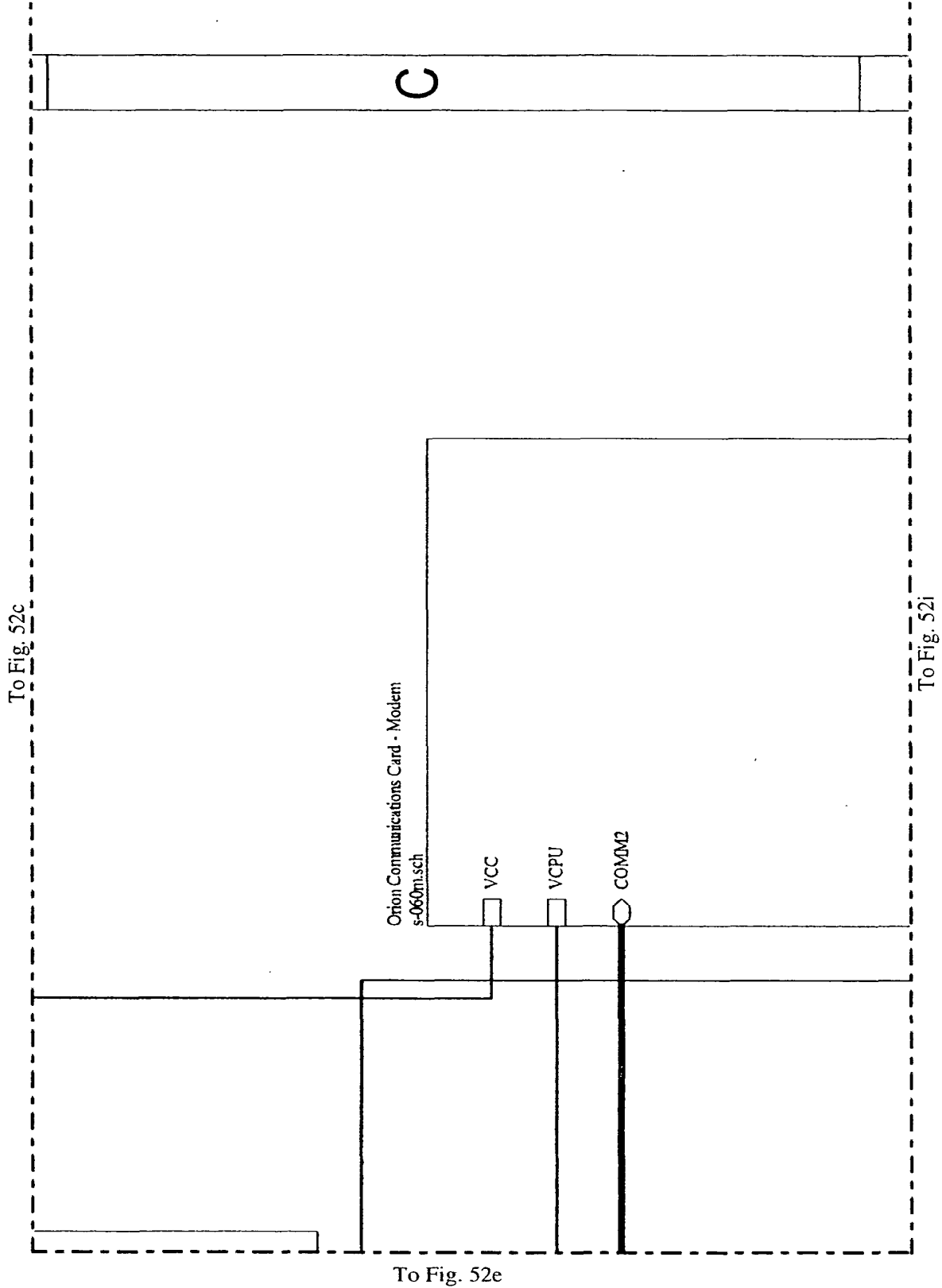
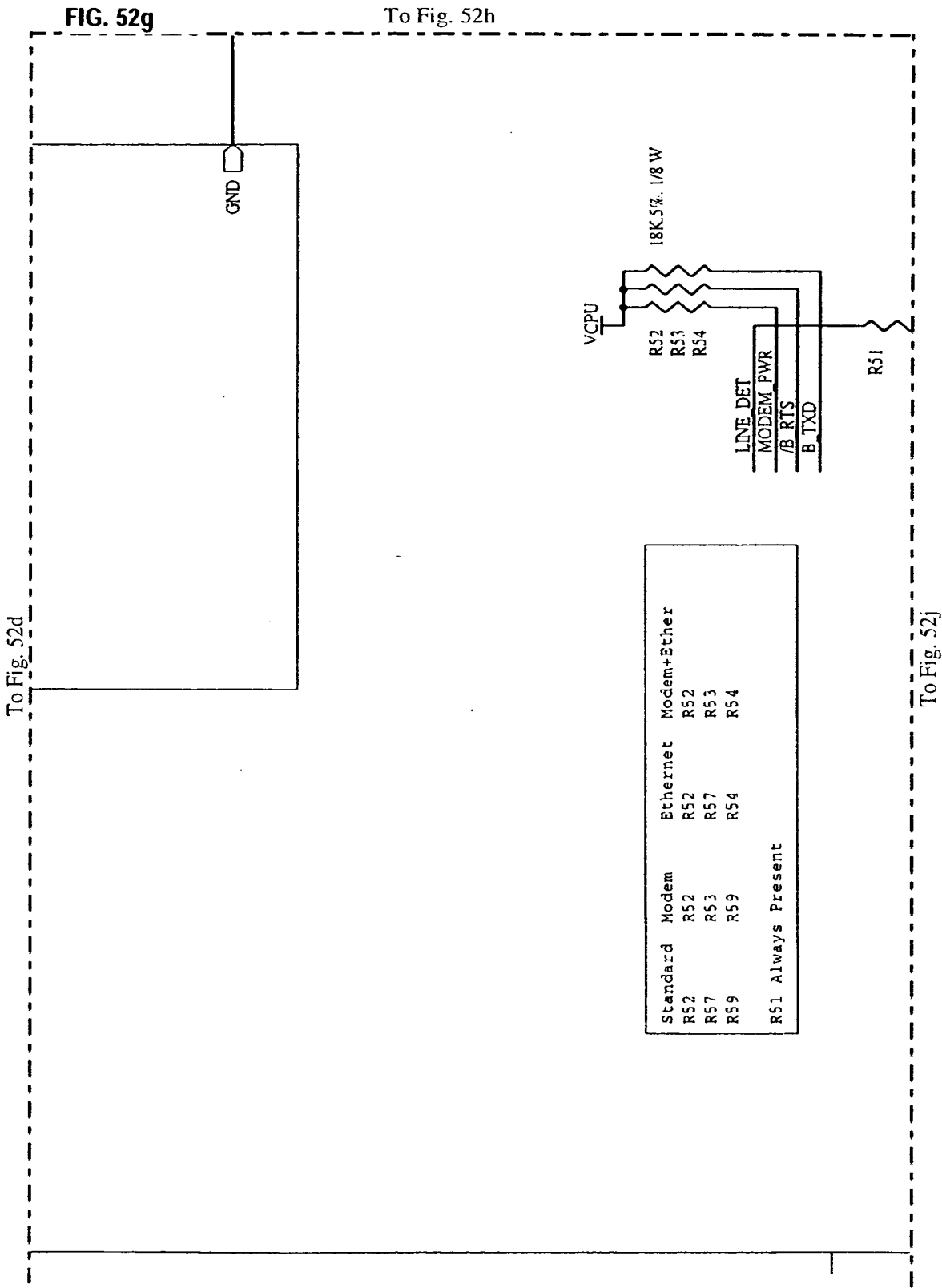


FIG. 52f





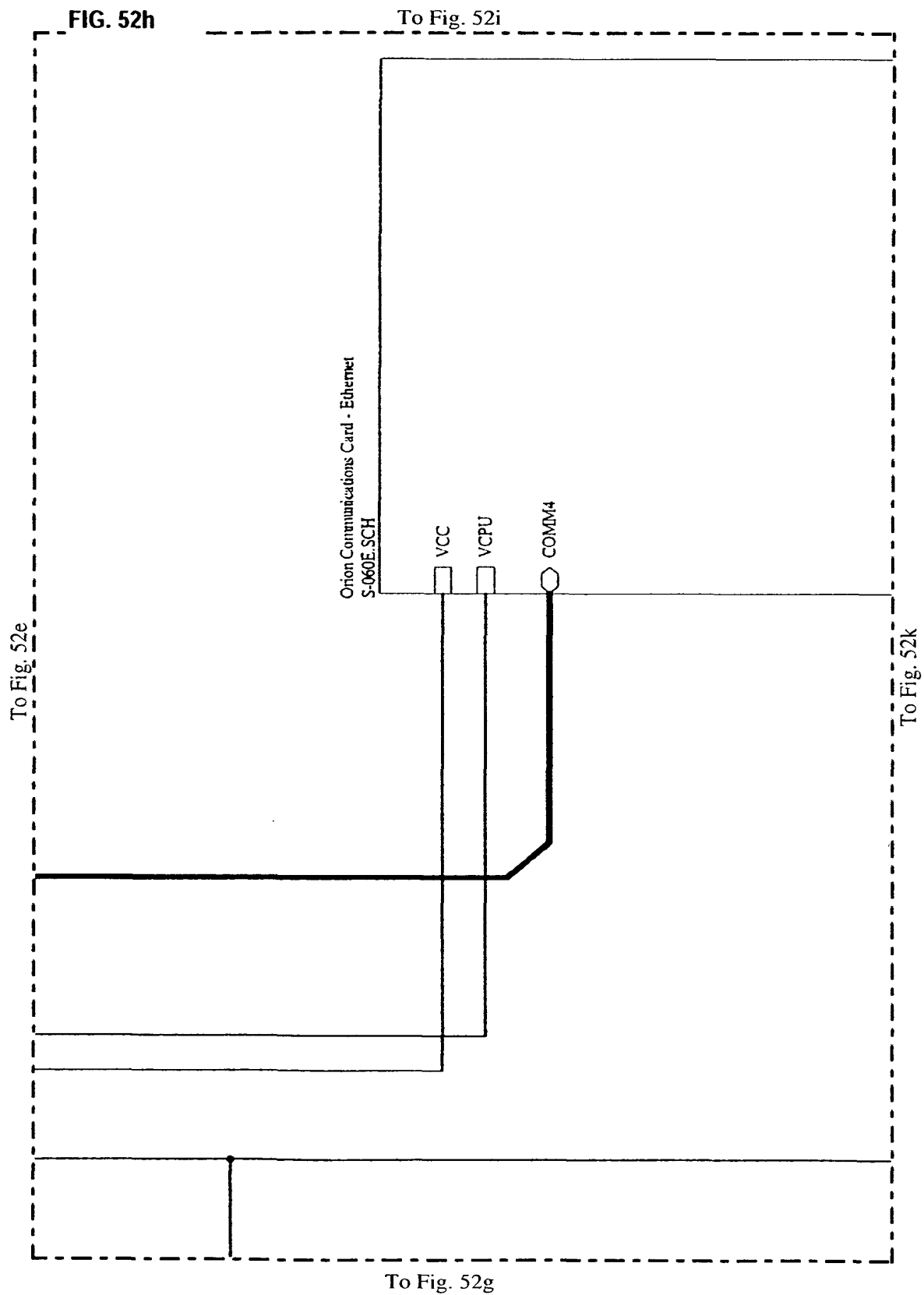
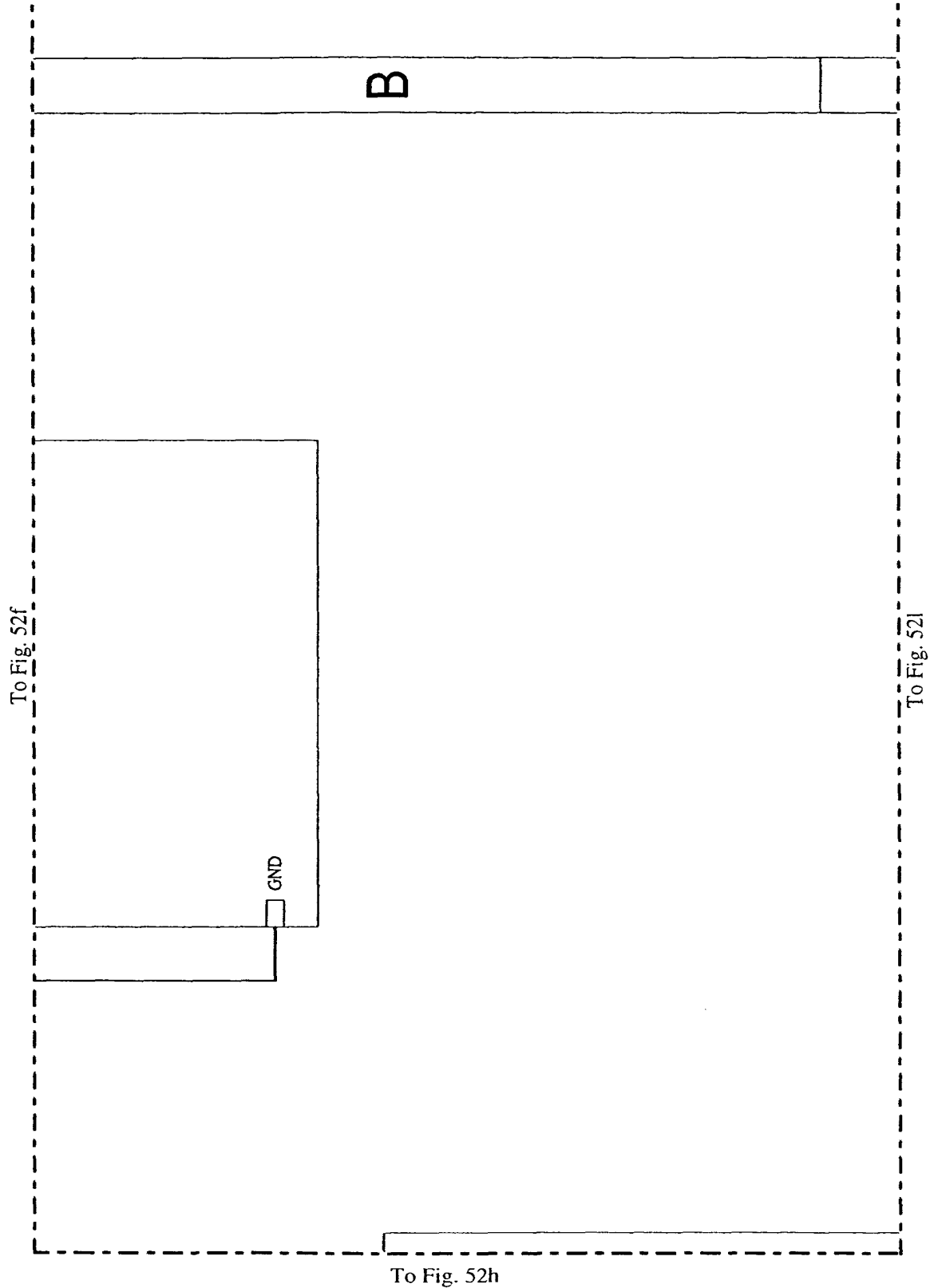
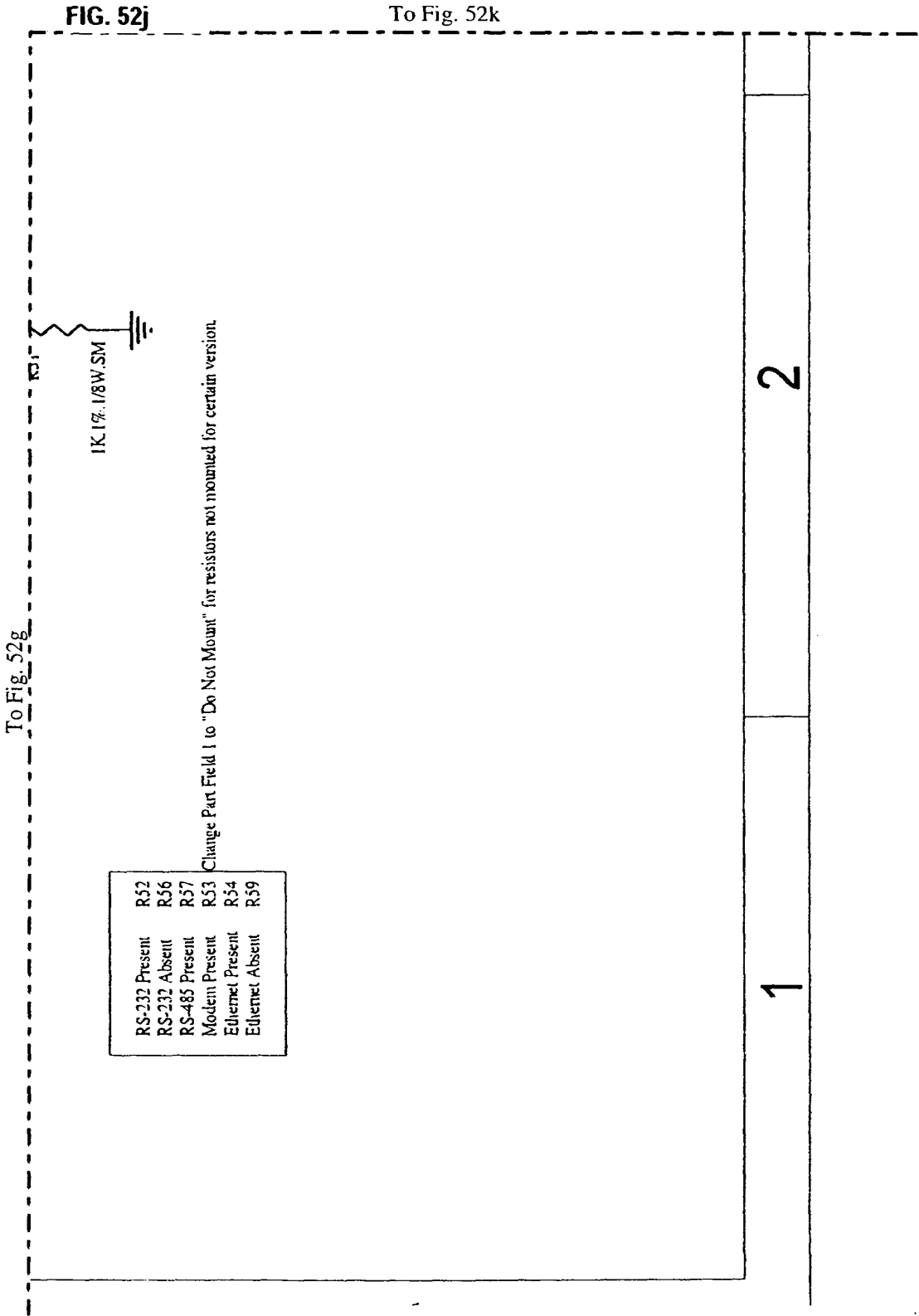


FIG. 52i





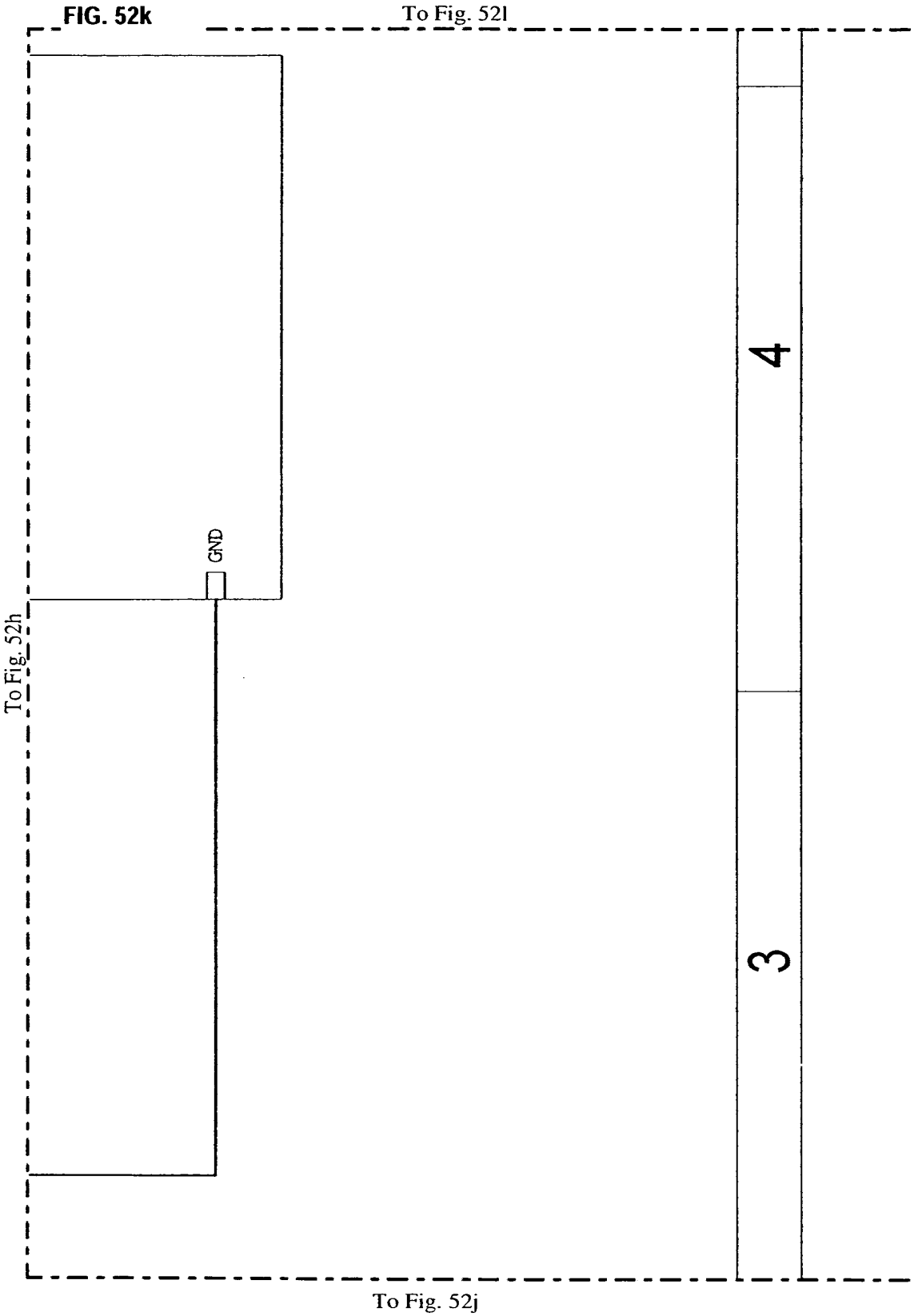
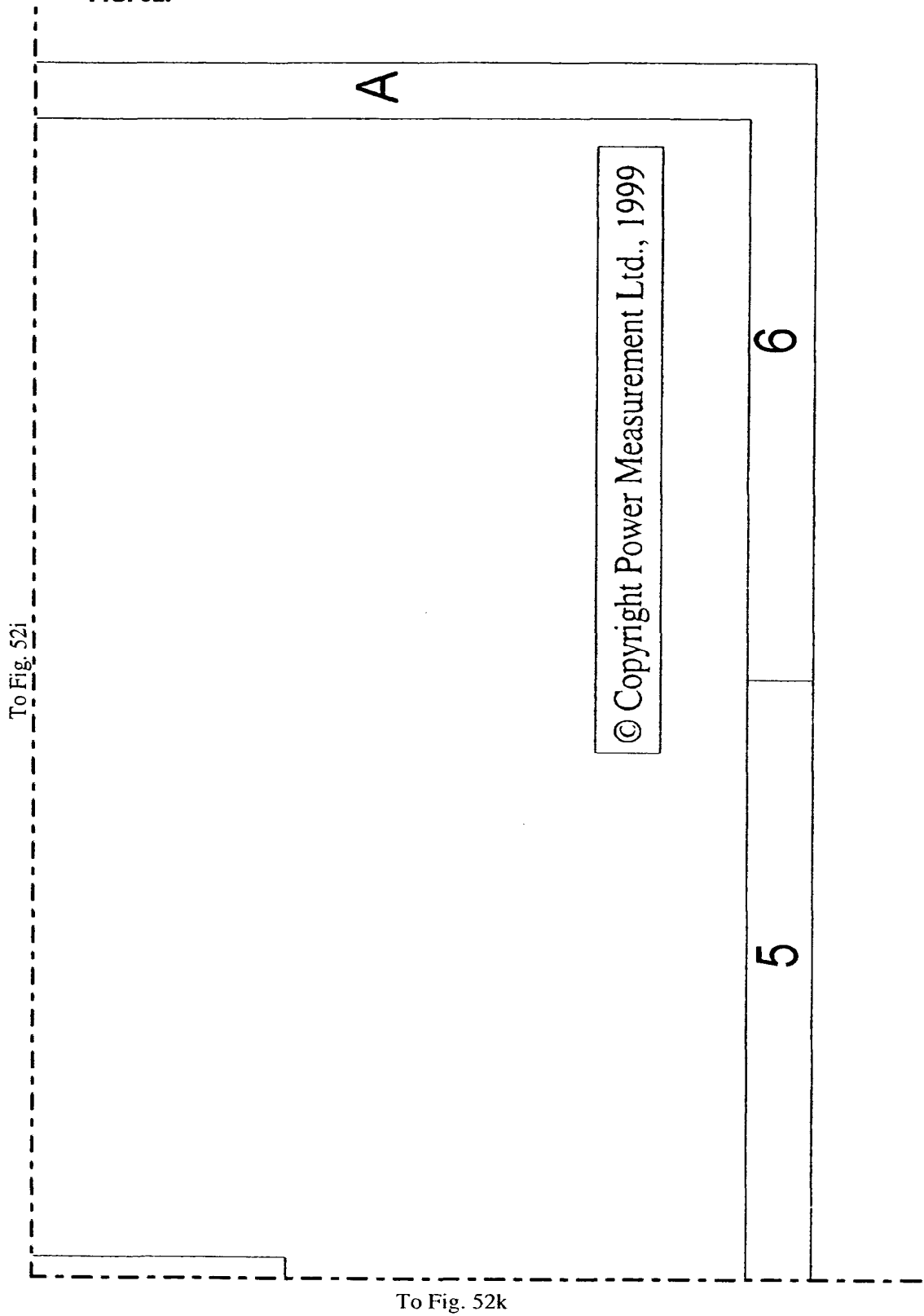
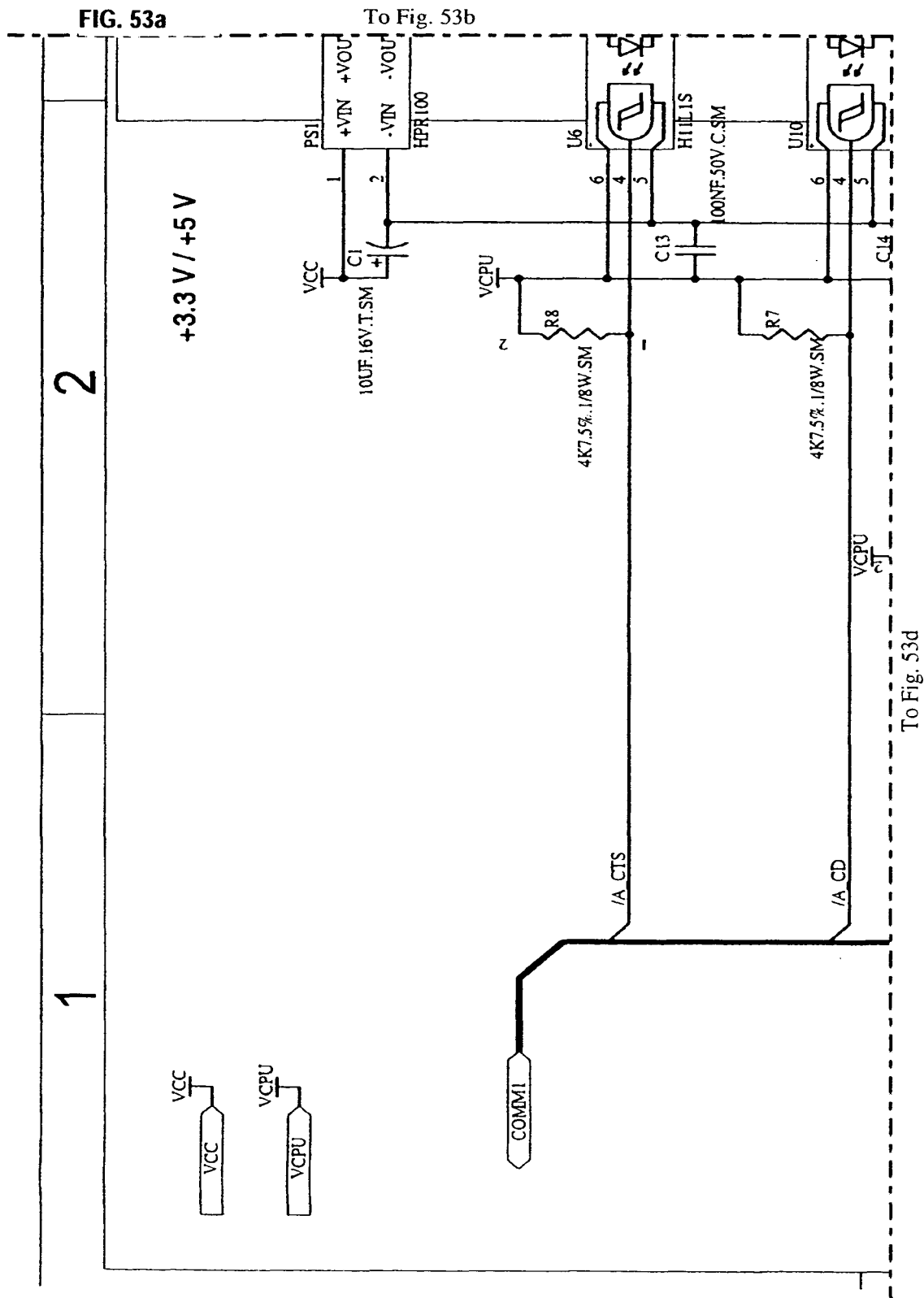


FIG. 52l





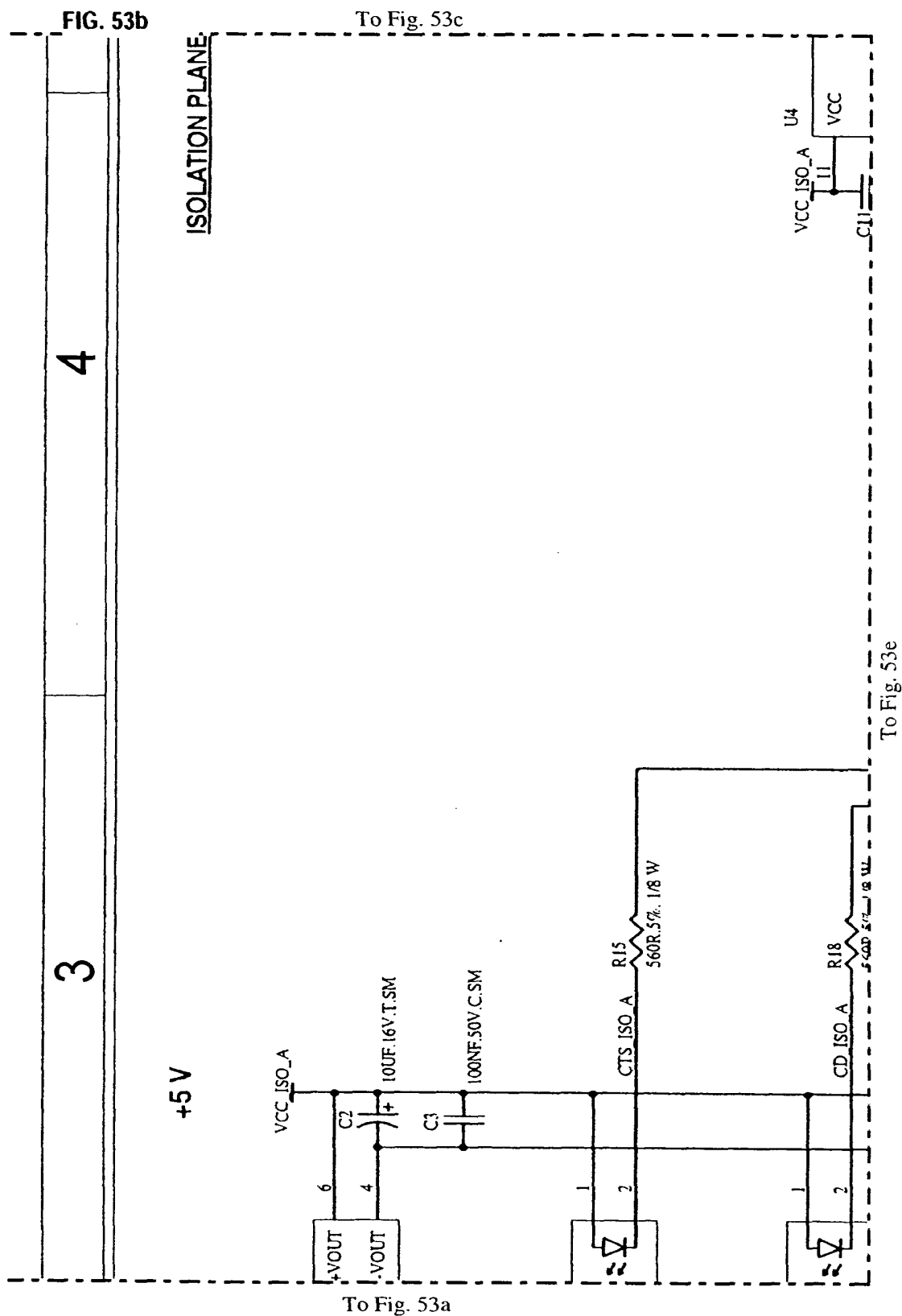
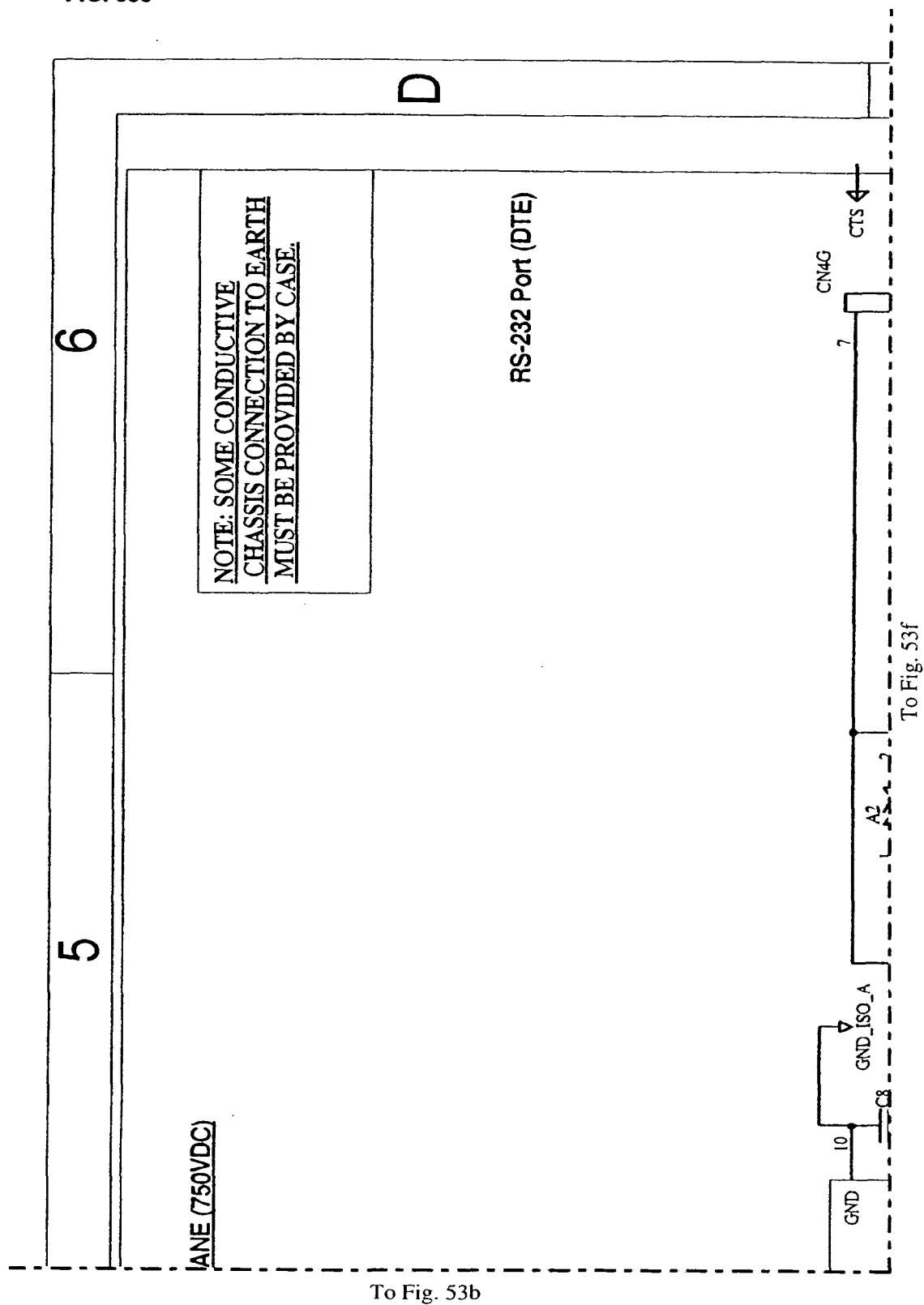


FIG. 53c



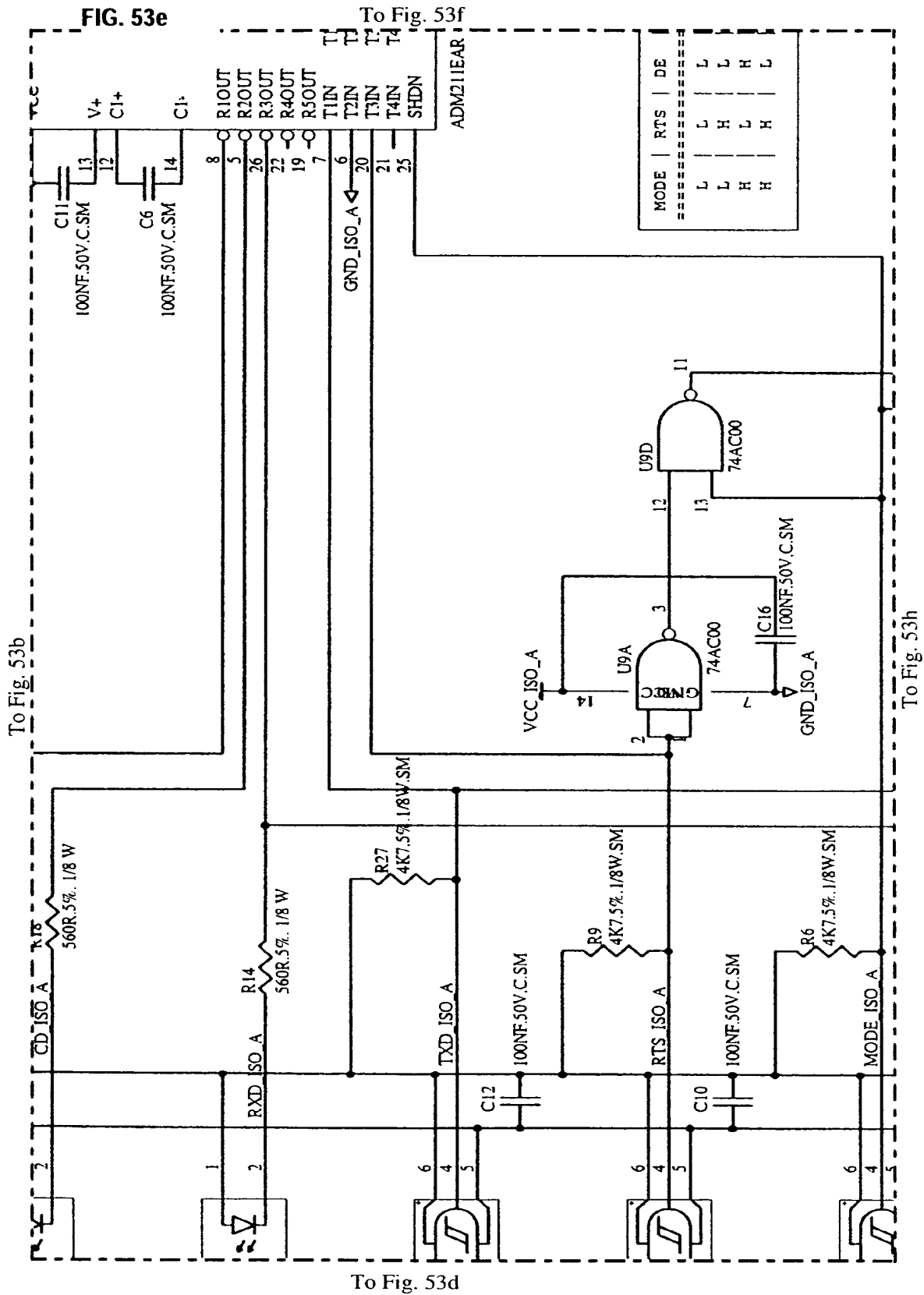
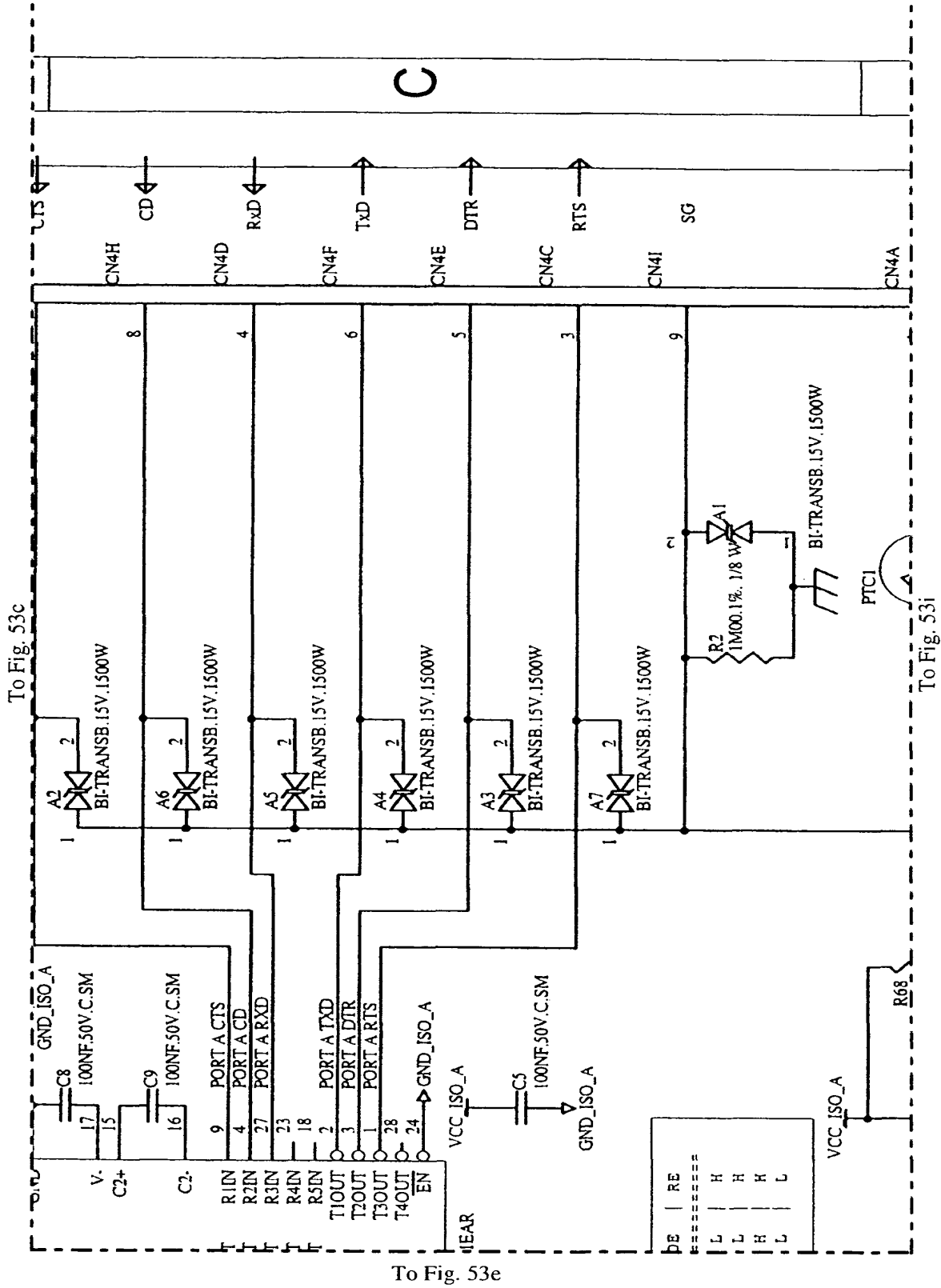
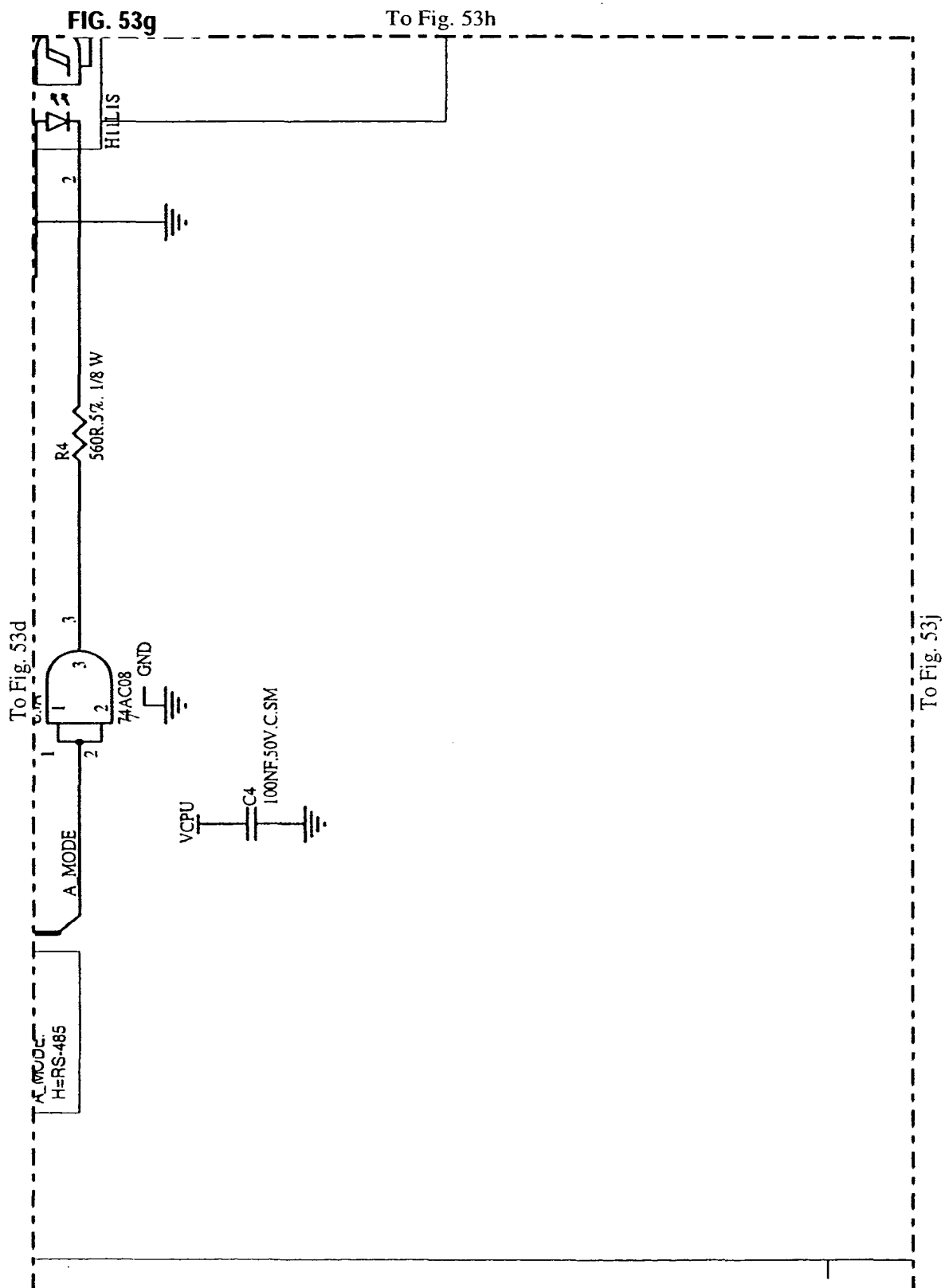
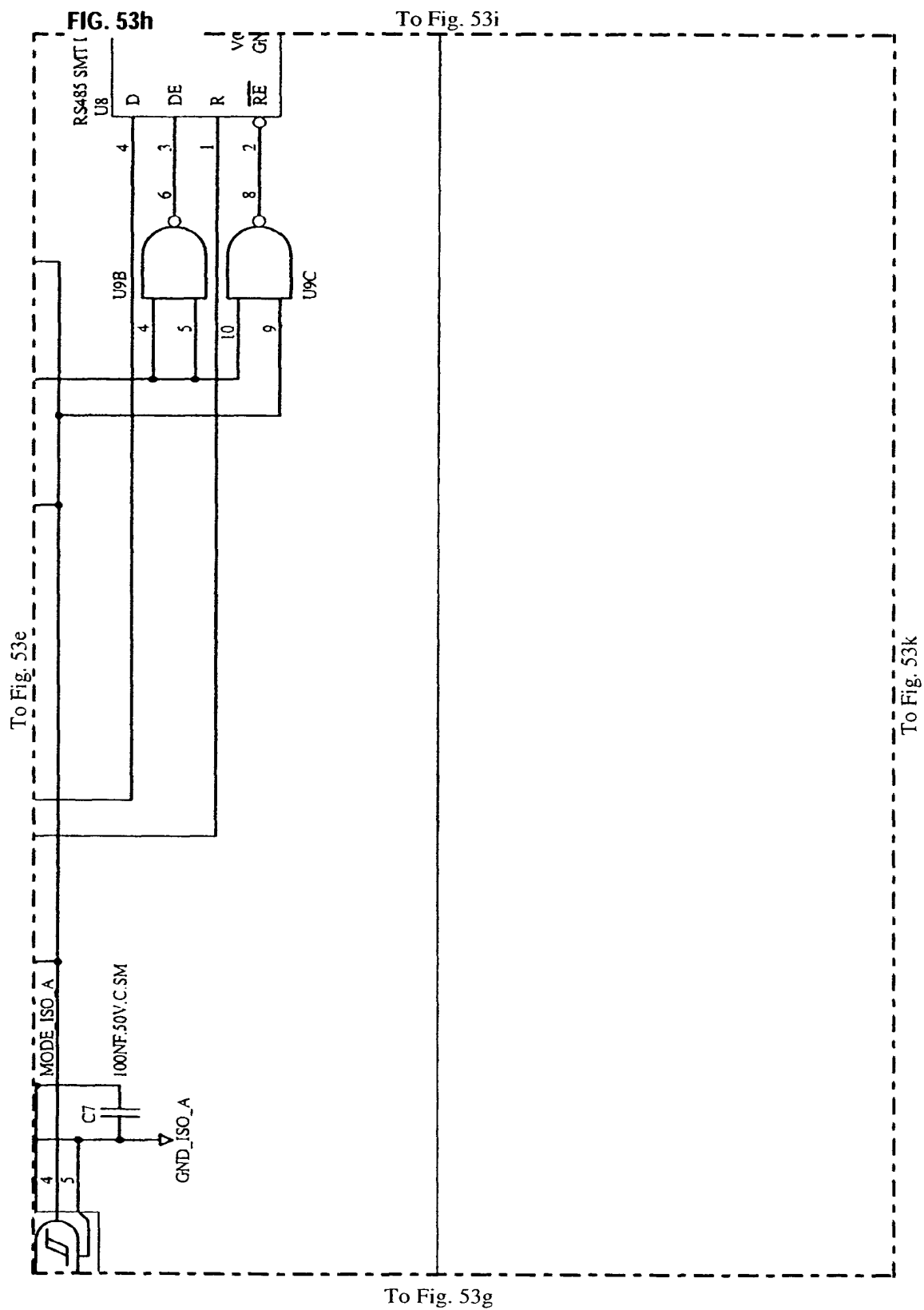
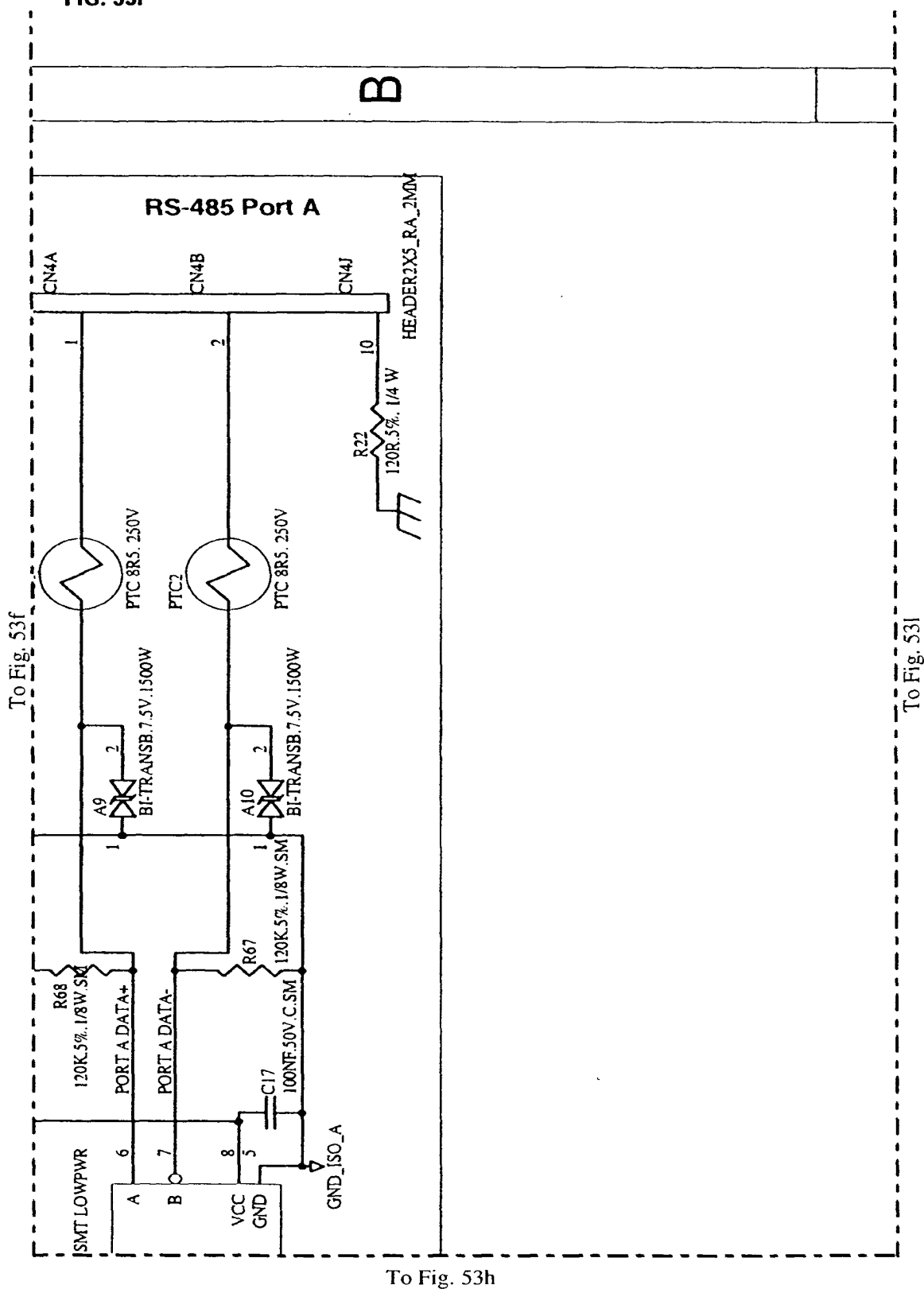


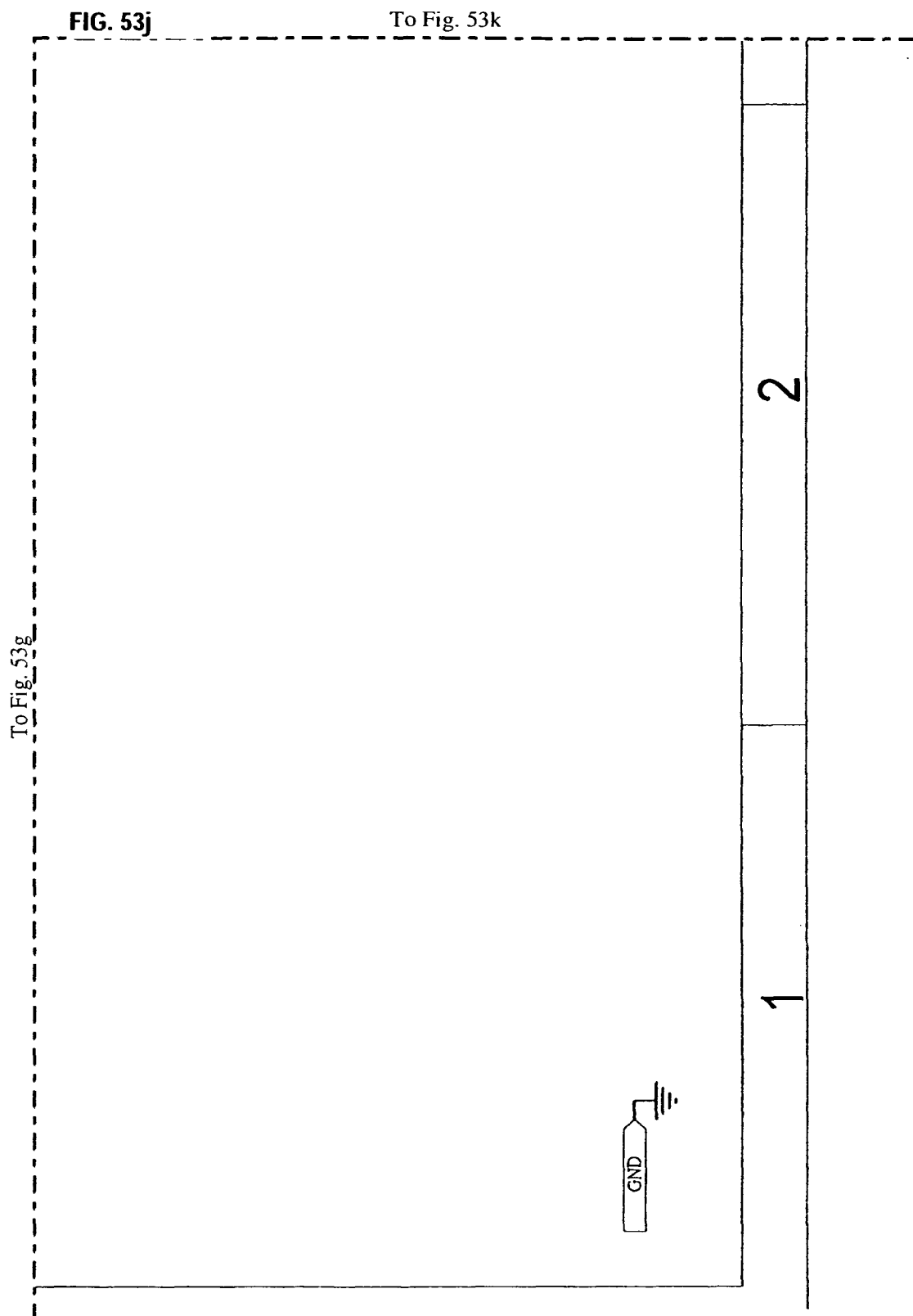
FIG. 53f











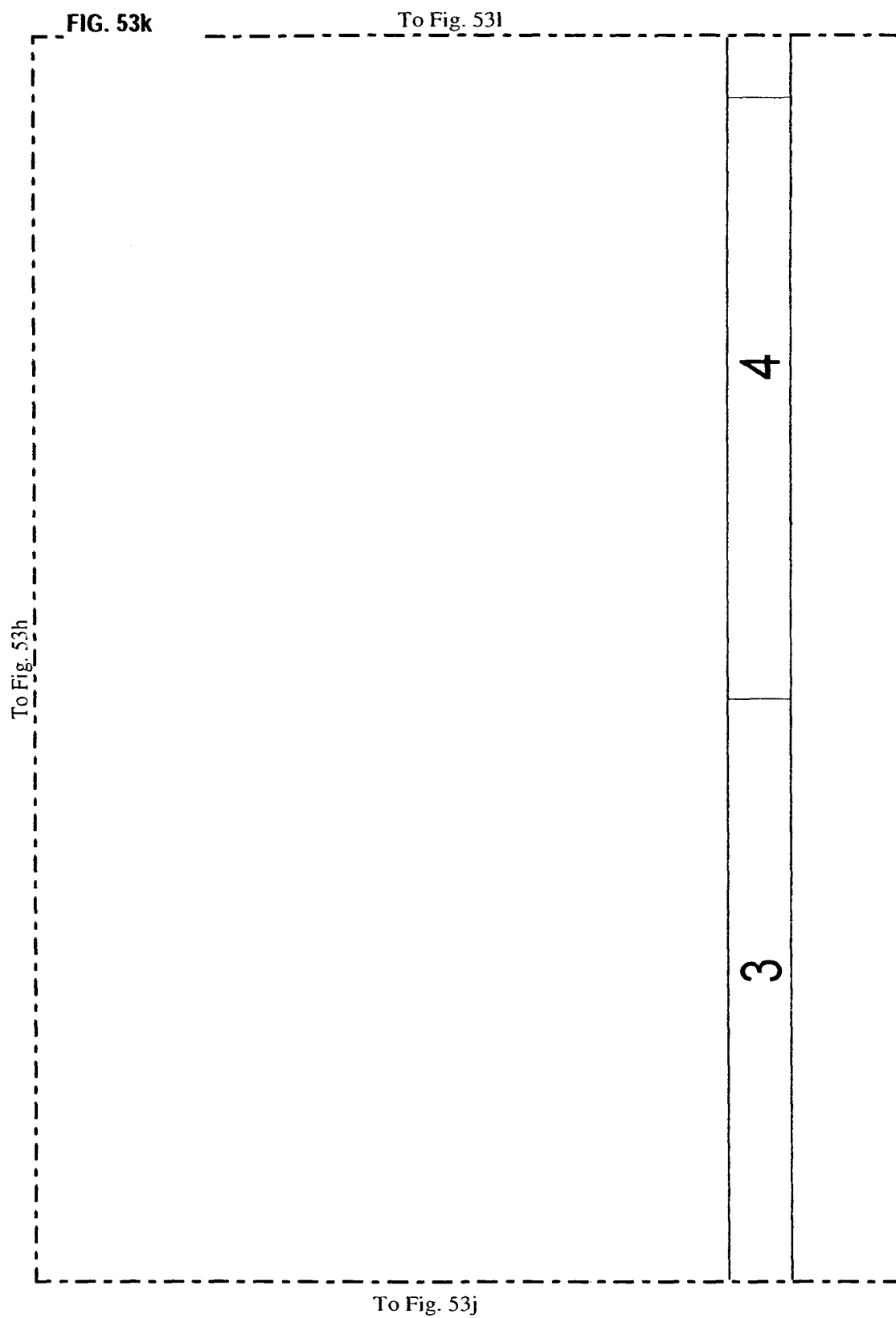


FIG. 53l

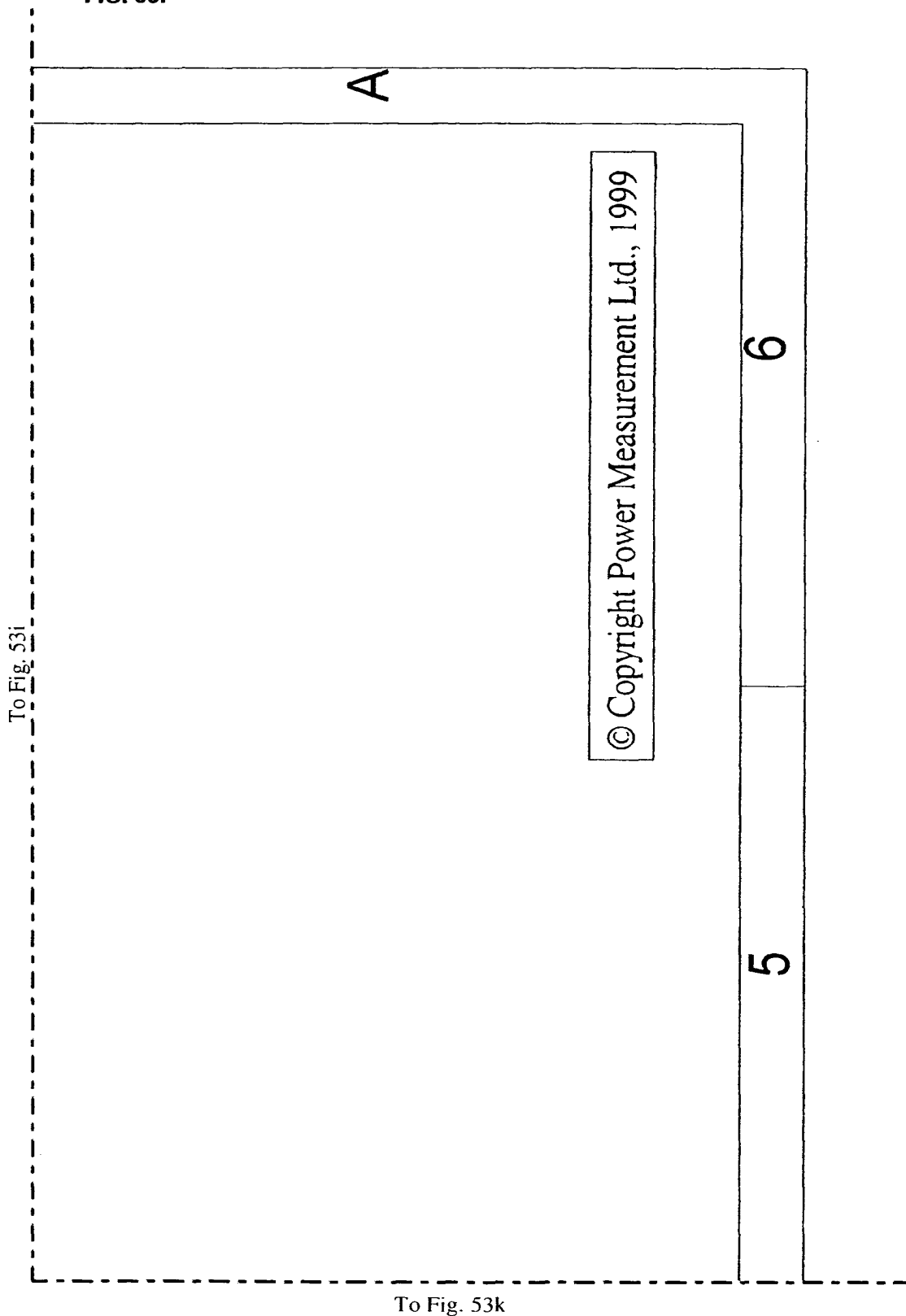


FIG. 54a

To Fig. 54b

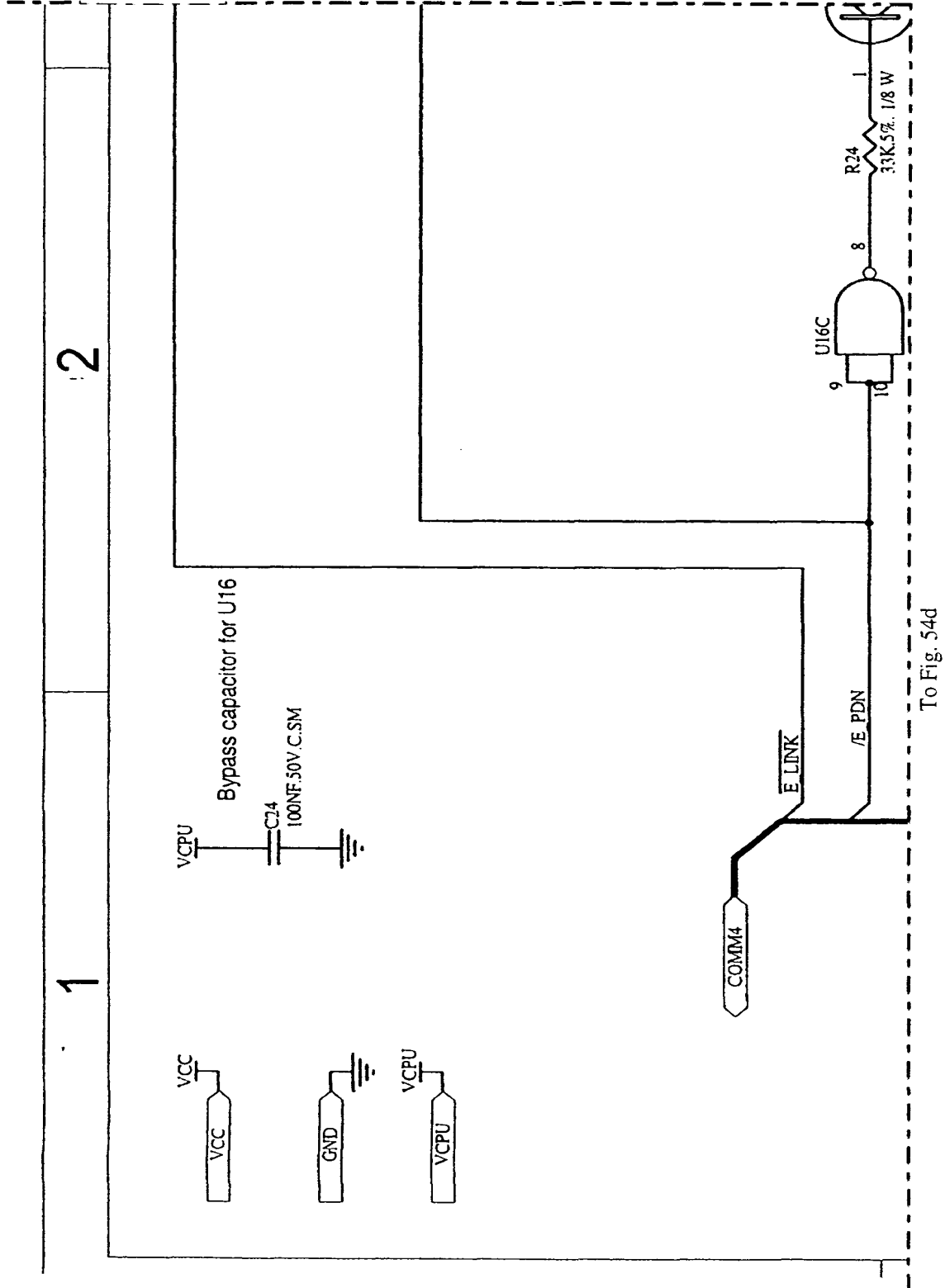


FIG. 54b

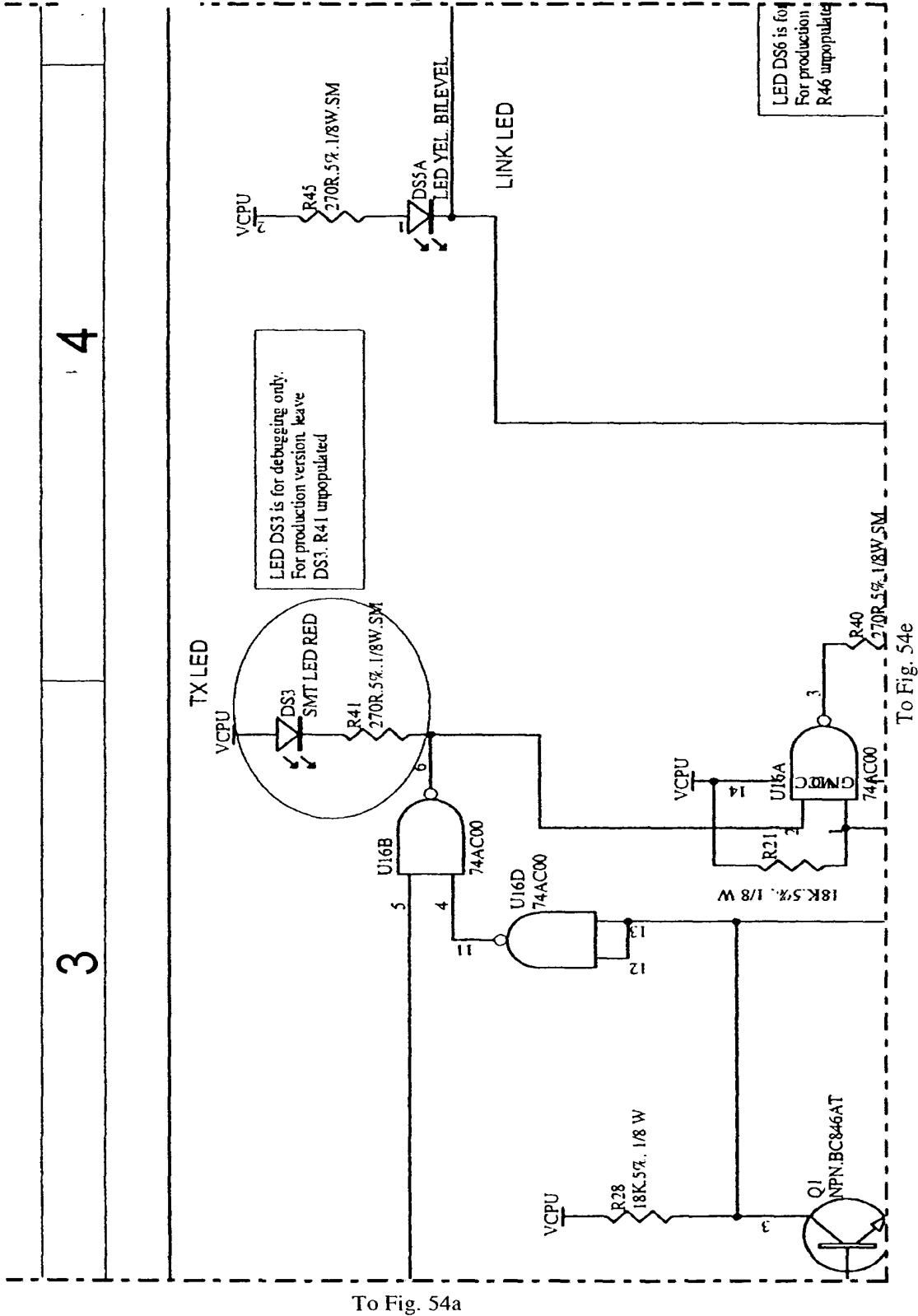
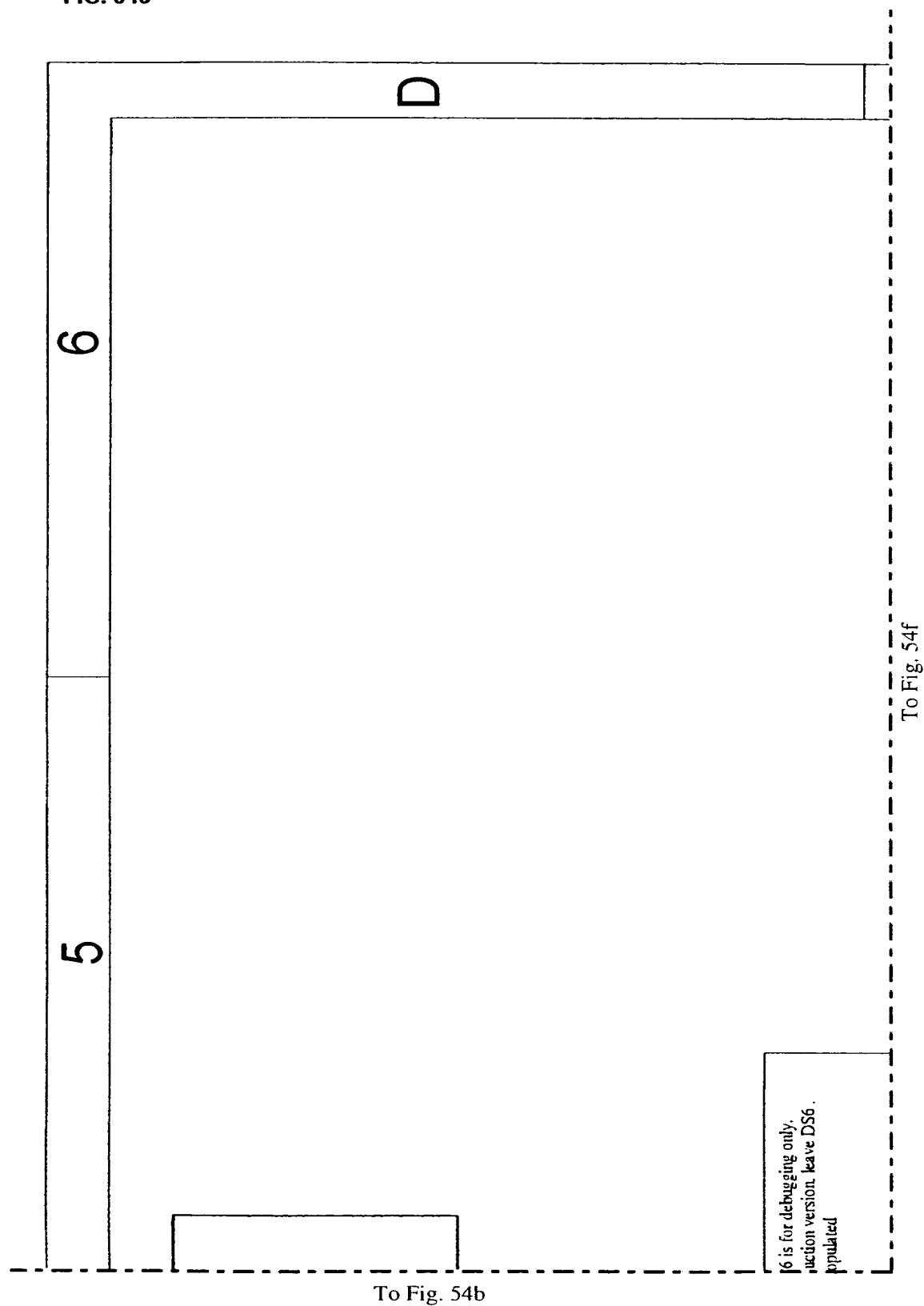
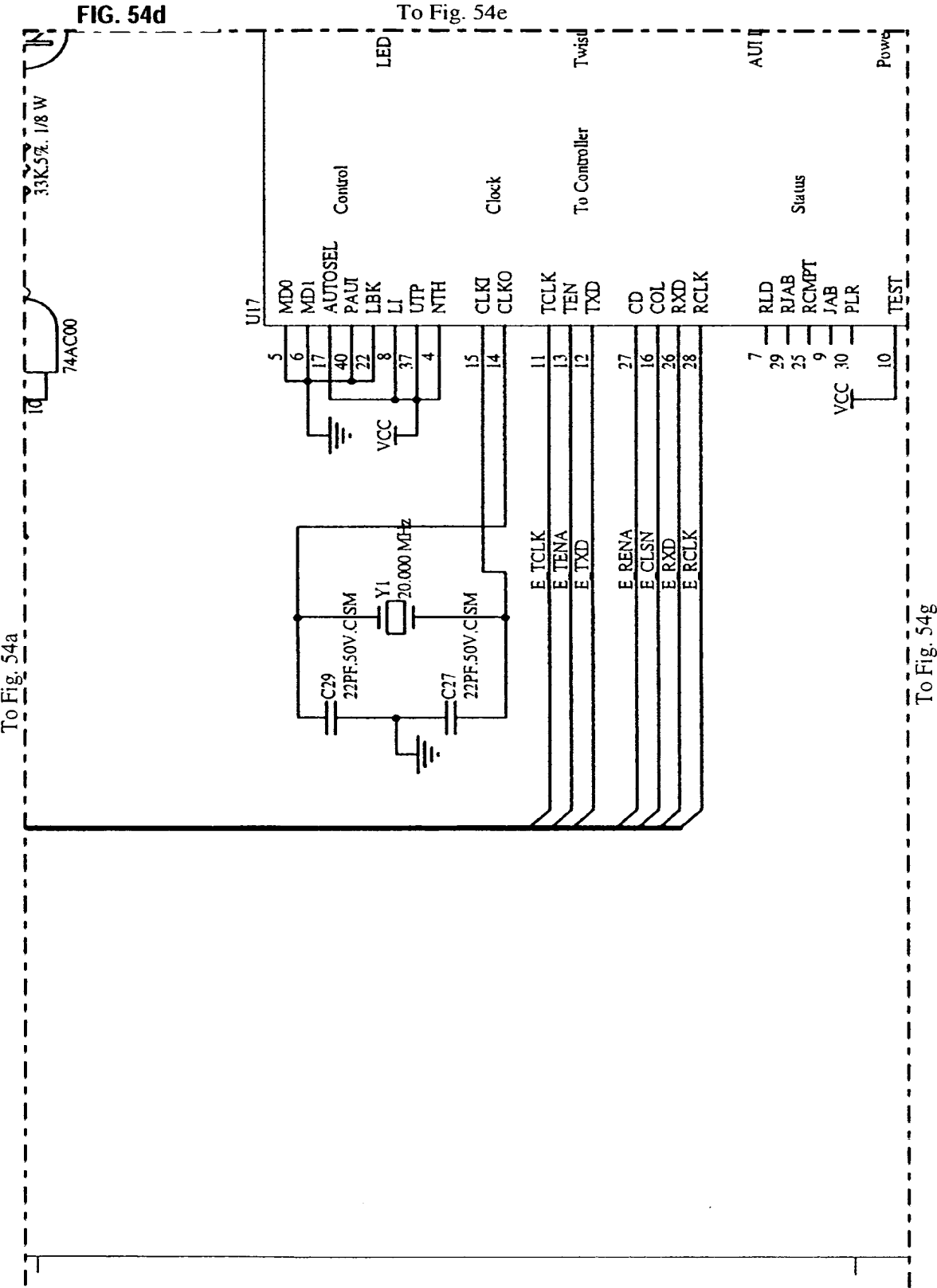


FIG. 54c





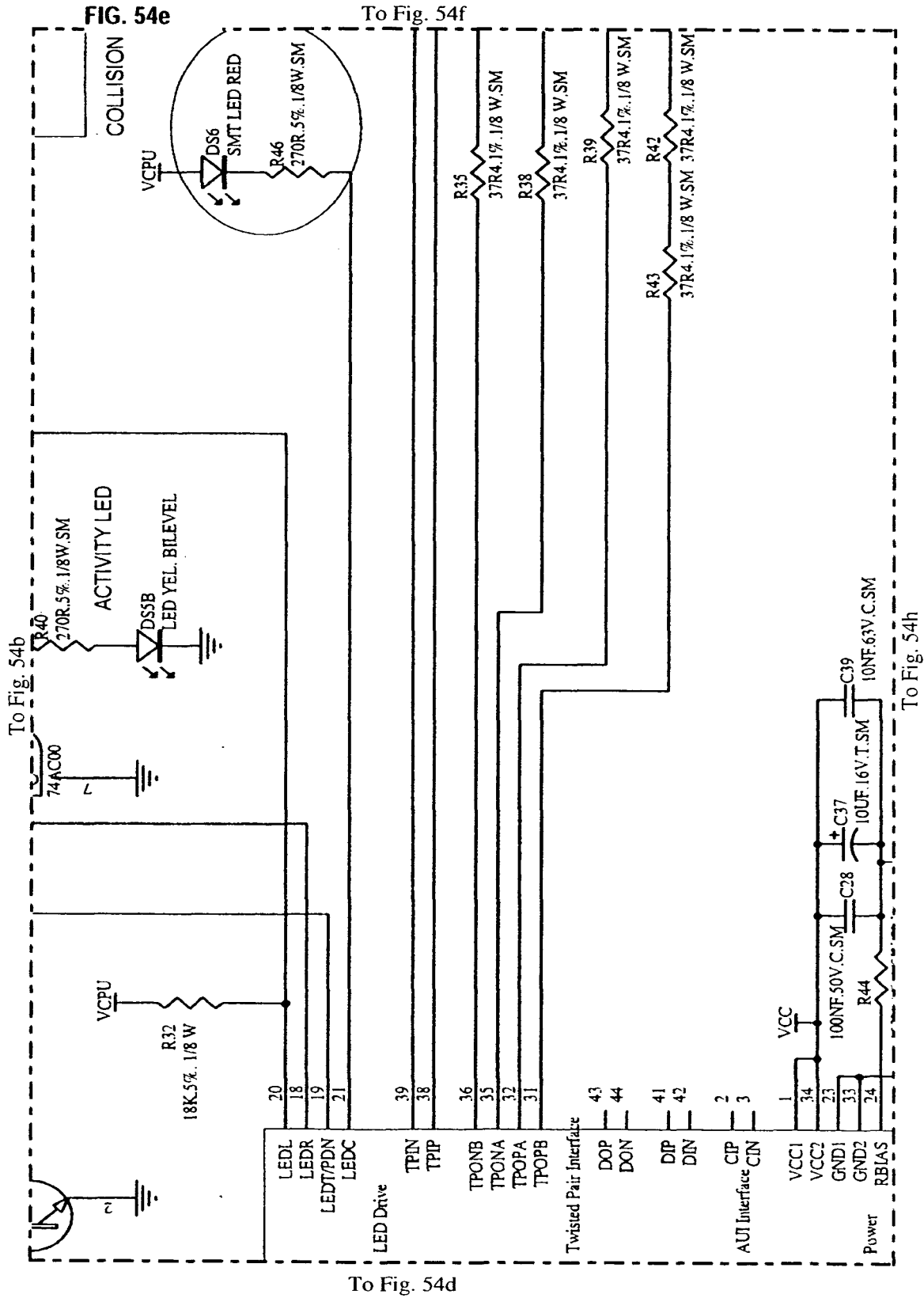
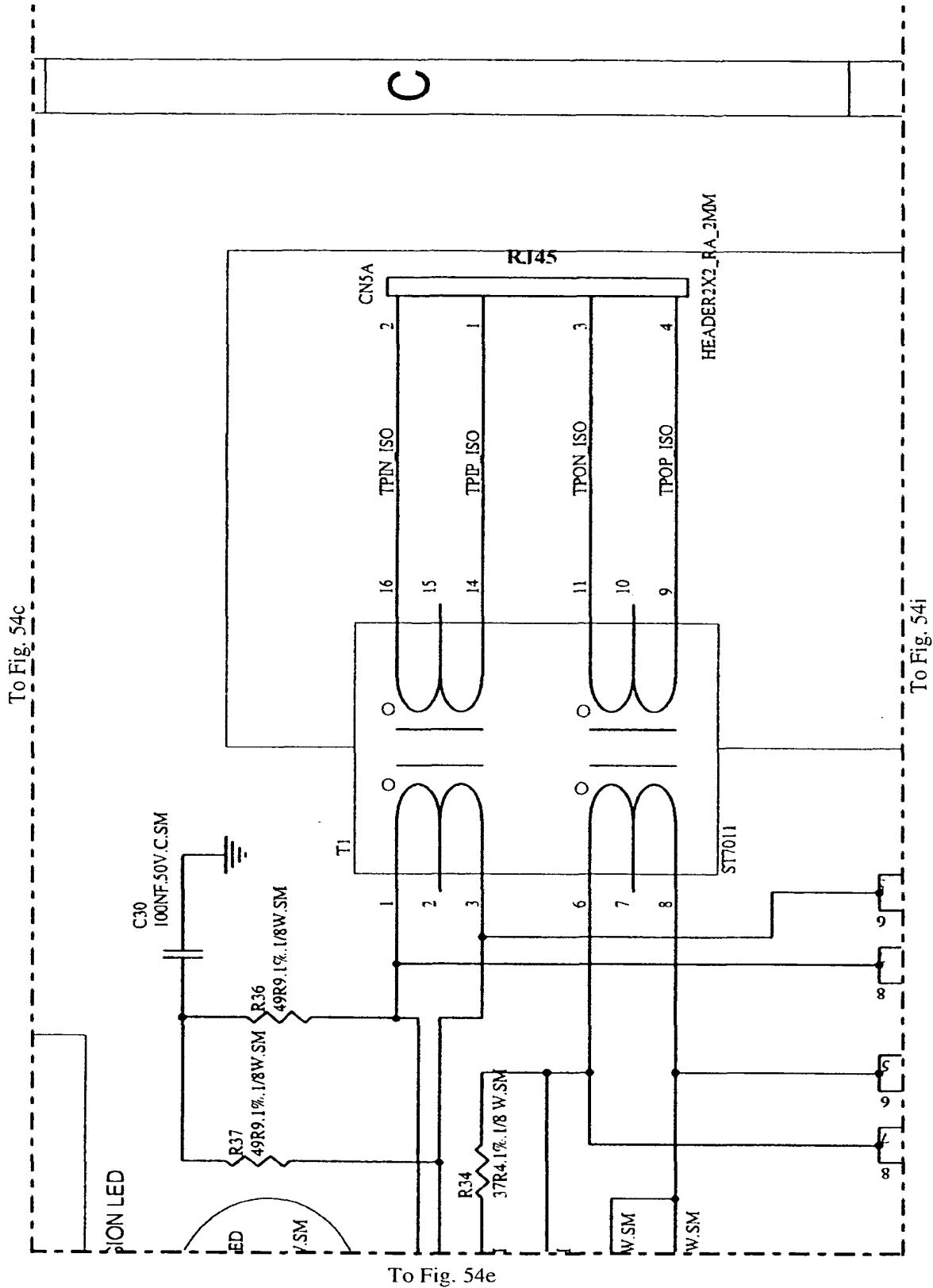
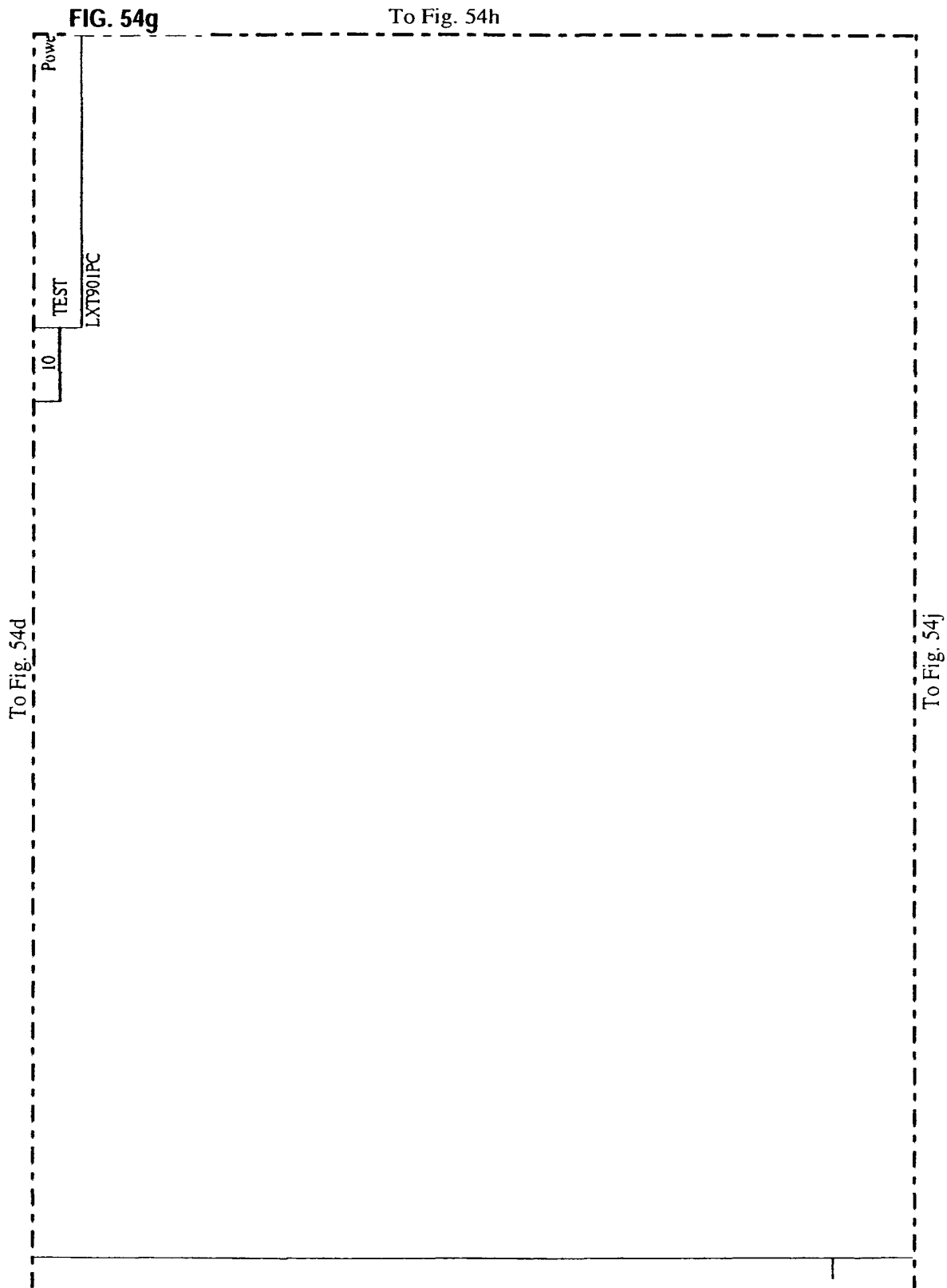


FIG. 54f



To Fig. 54e

To Fig. 54i



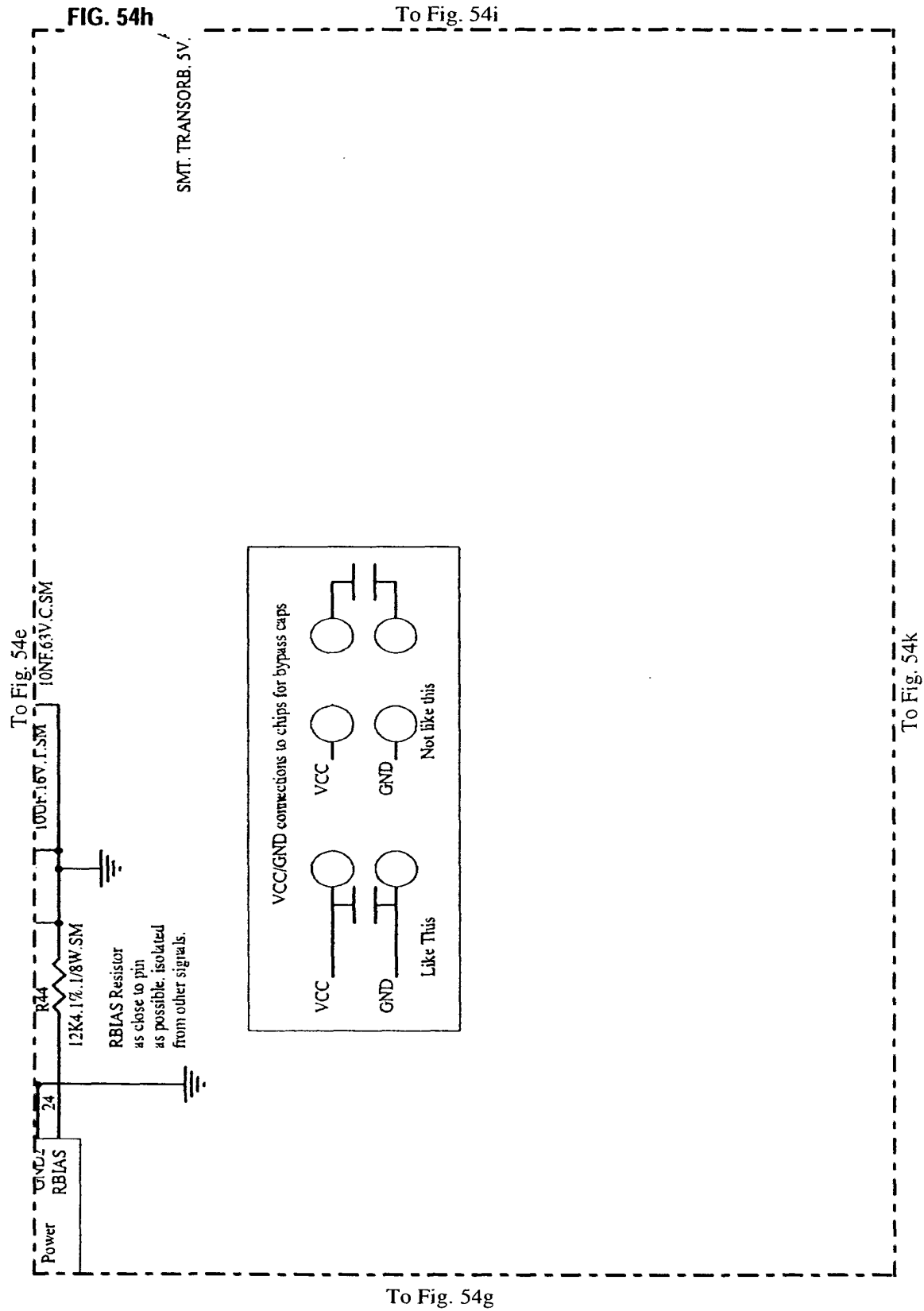


FIG. 54i

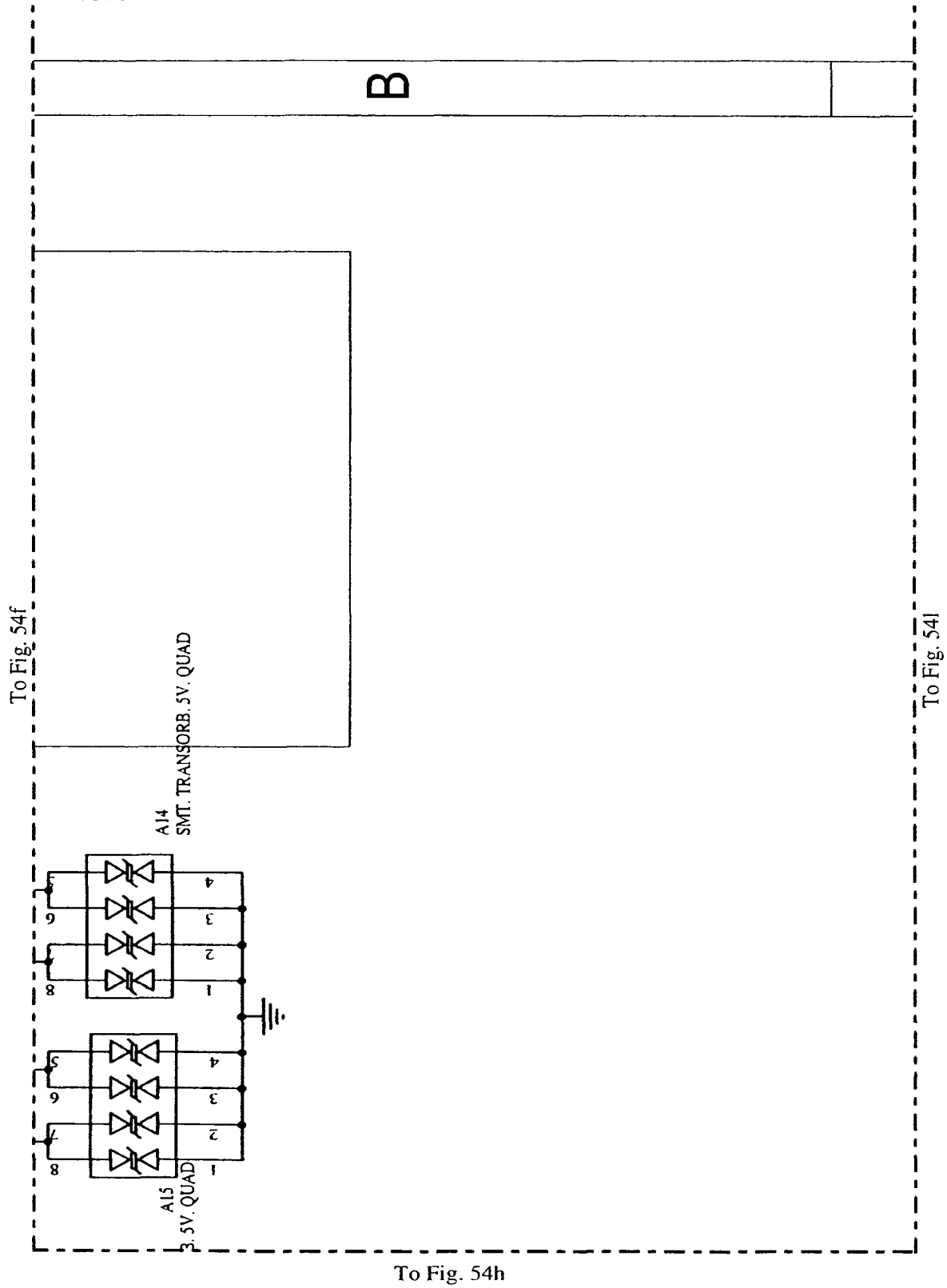
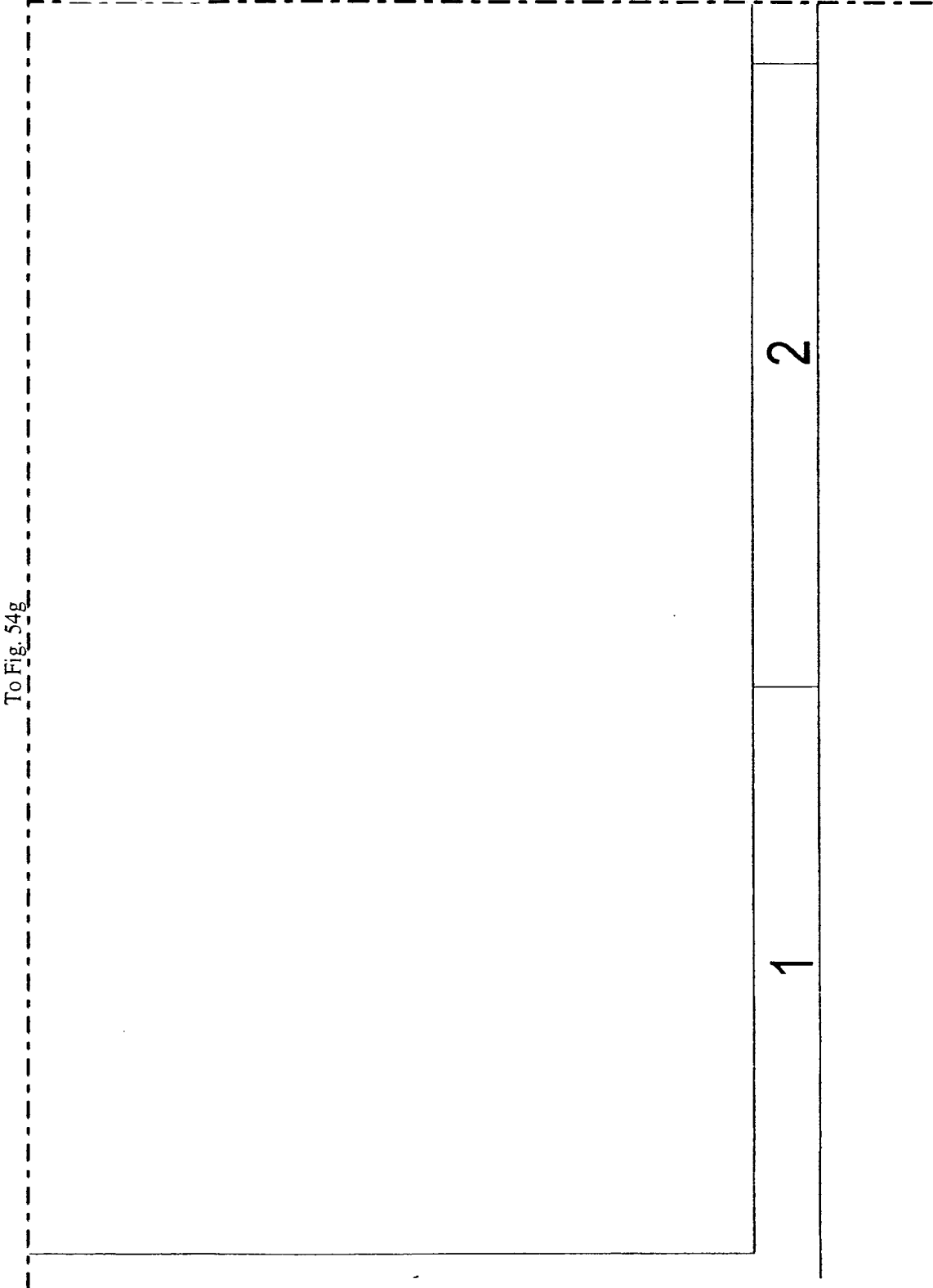


FIG. 54j

To Fig. 54k



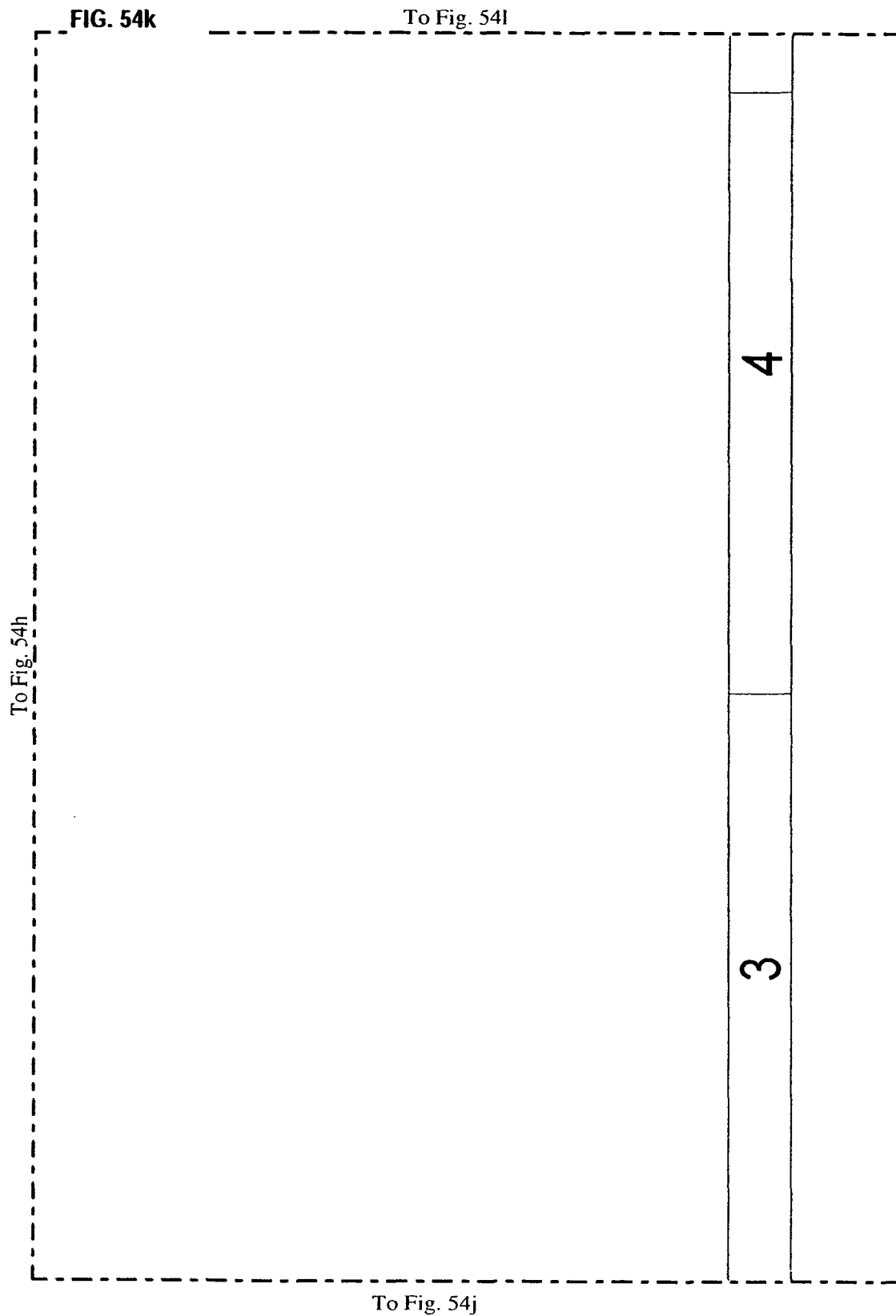
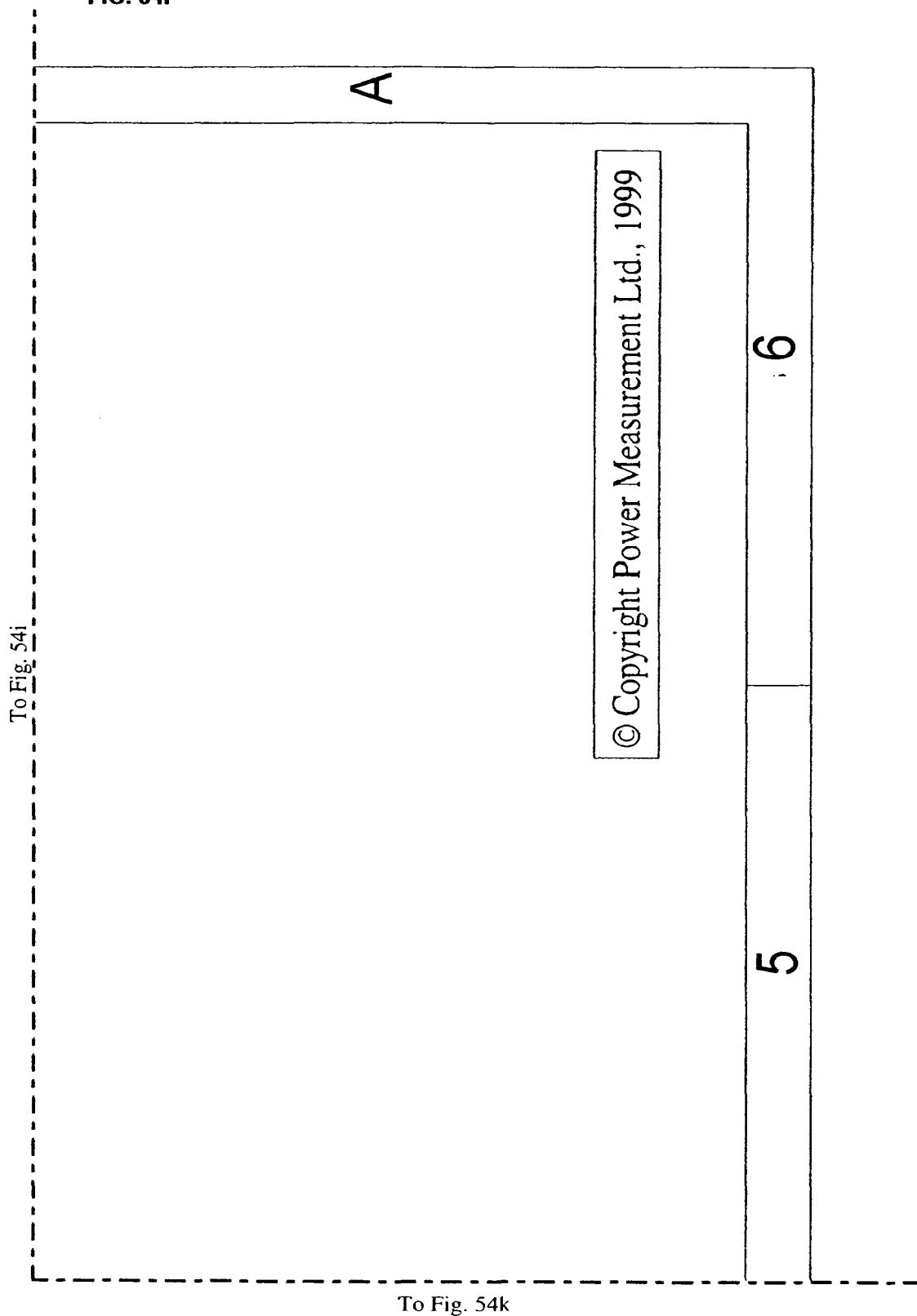
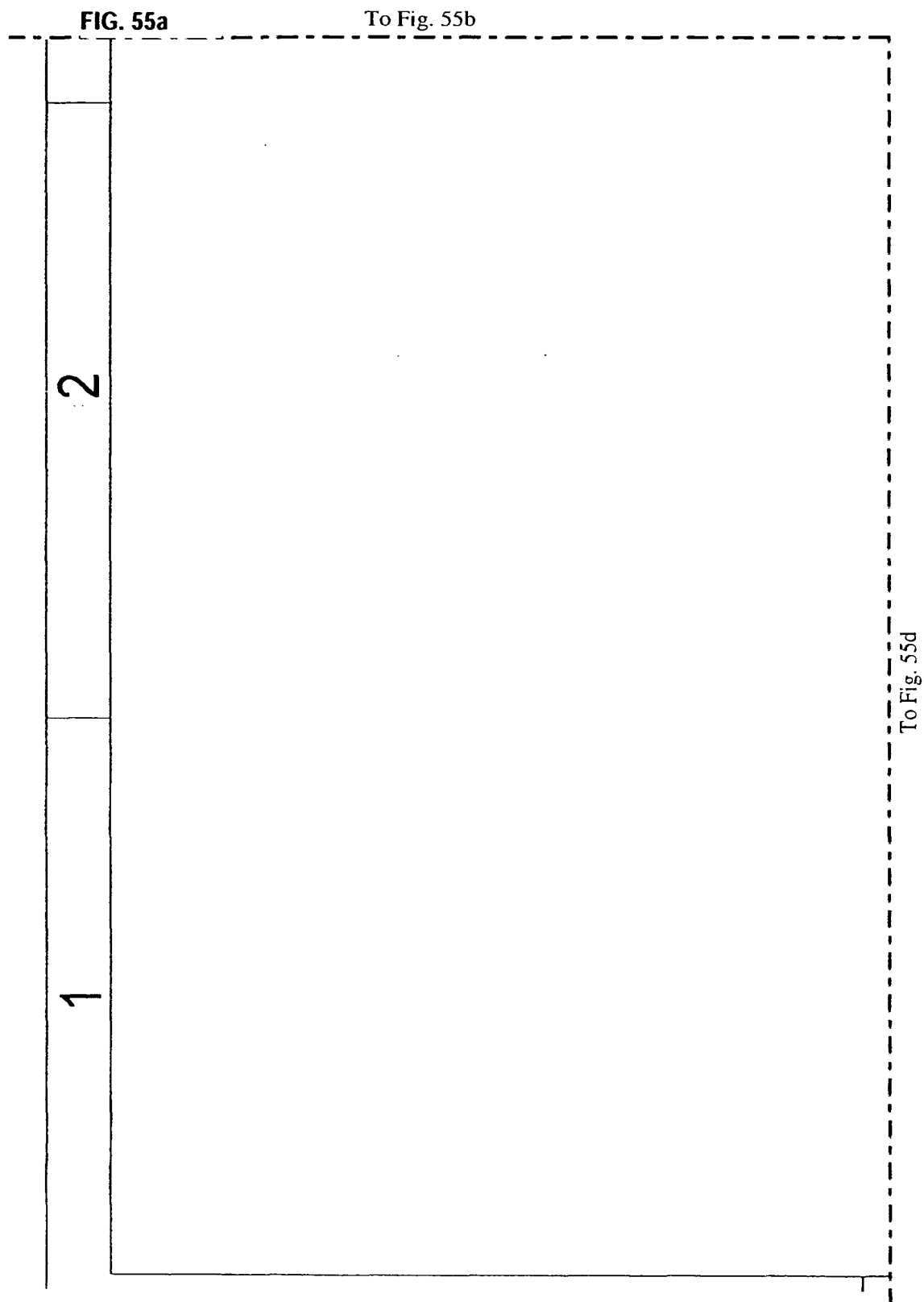


FIG. 54l





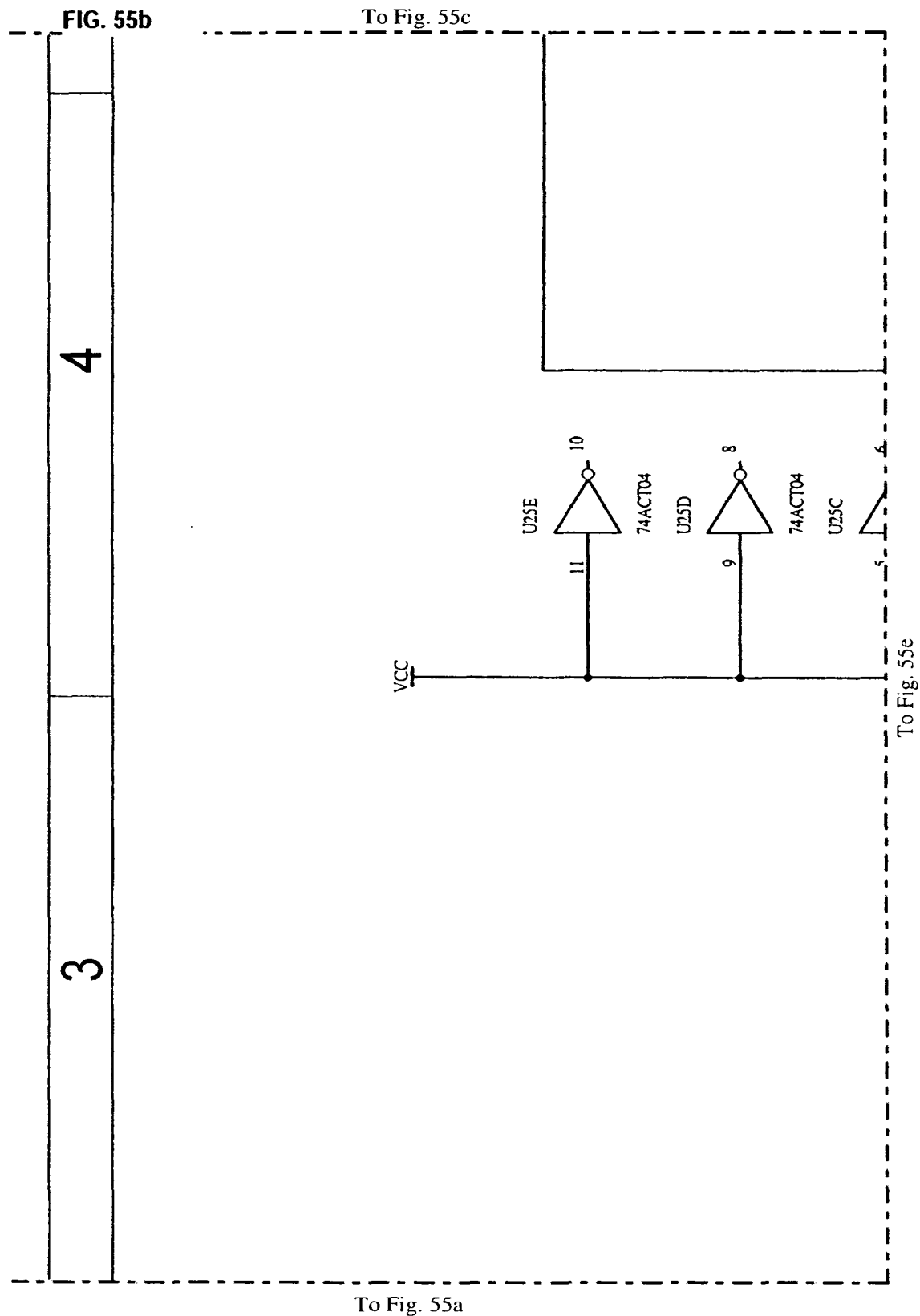
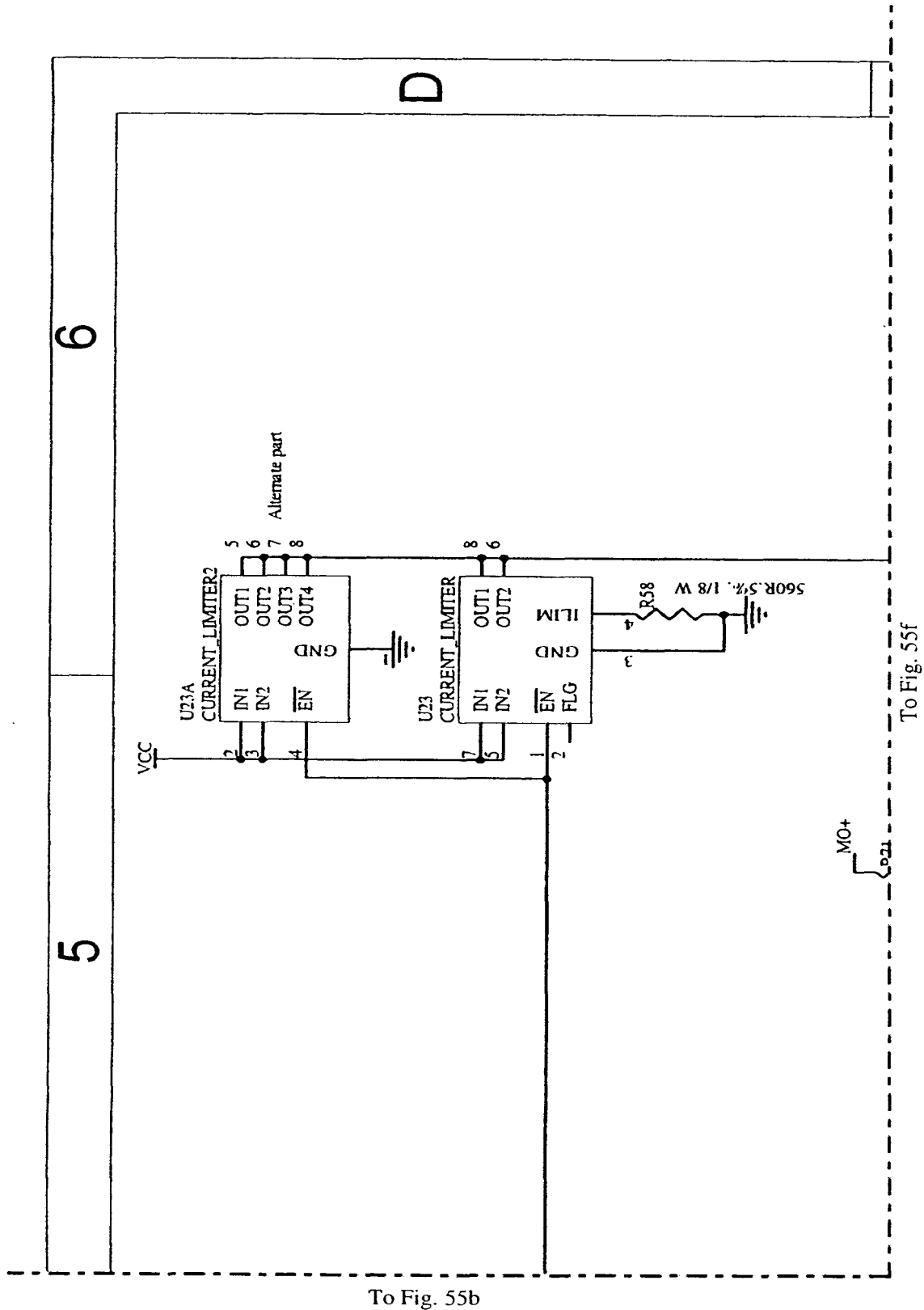


FIG. 55c

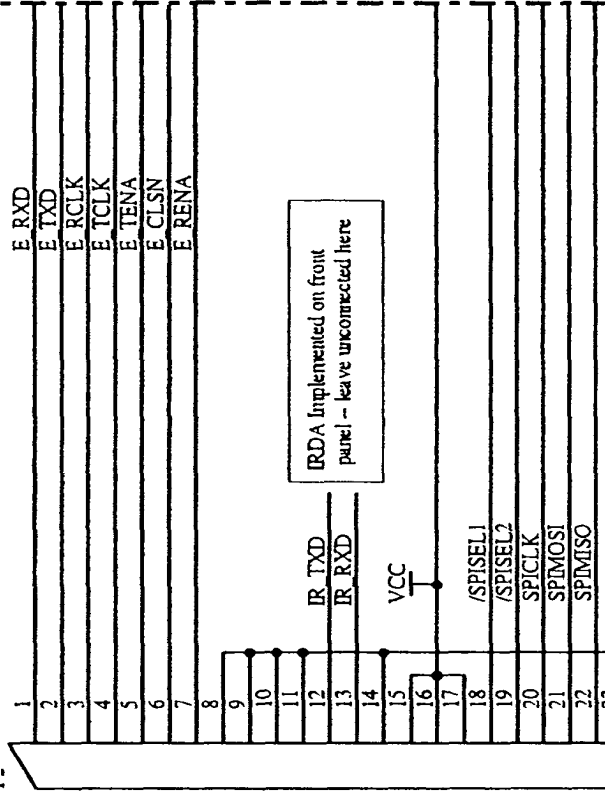


To Fig. 55a

FIG. 55d

COMMUNICATIONS CARD CONNECTOR

RA-50PINBOARDLEVELCONNECTOR
P2



To Fig. 55g

To Fig. 55e

The diagram shows a circuit with three 74ACT04 hex inverters. The first inverter (U25A) has its input (pin 1) connected to a common bus (COM4) and its output (pin 2) connected to a 18K.5% 1/8 W resistor (R65). The second inverter (U25B) has its input (pin 3) connected to the same common bus (COM4) and its output (pin 4) connected to a 100NF 50V C.S. capacitor (C40). The third inverter (U20) has its input (pin 1) connected to the common bus (COM4) and its output (pin 2) connected to the VCPU. The circuit is labeled 'To Fig. 55b' and 'To Fig. 55d'.

FIG. 55f

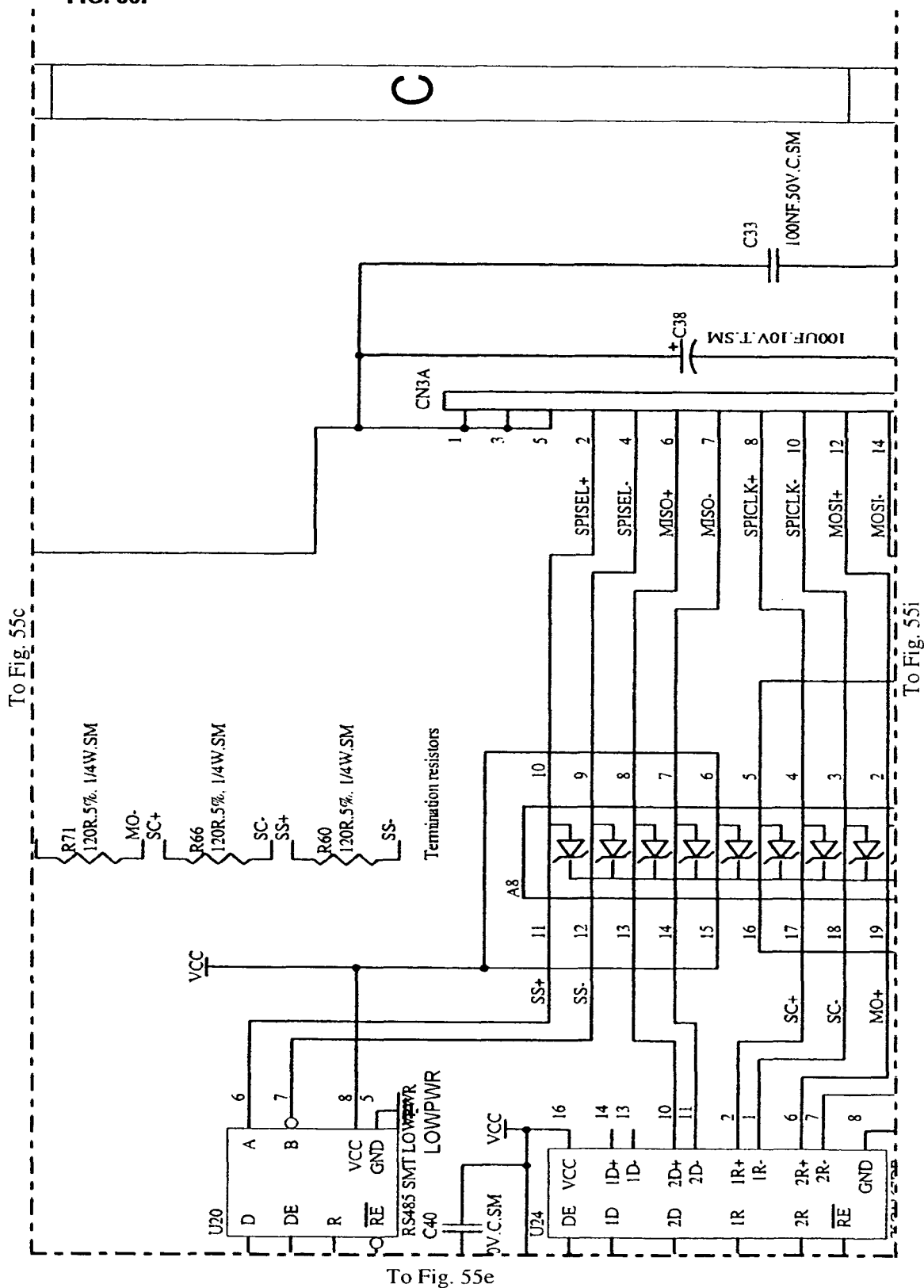
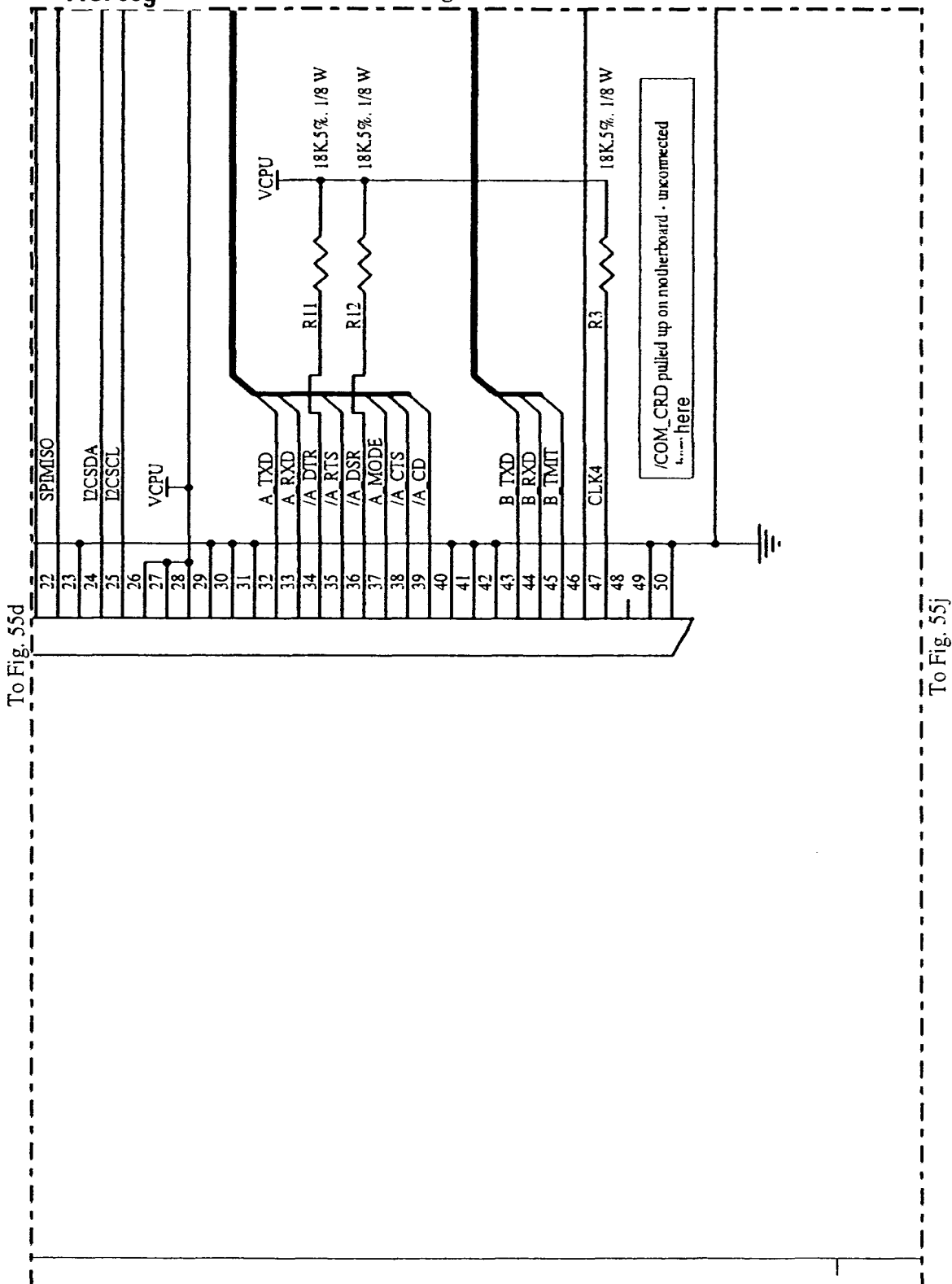


FIG. 55g

To Fig. 55h



To Fig. 55j

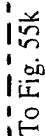


FIG. 55i

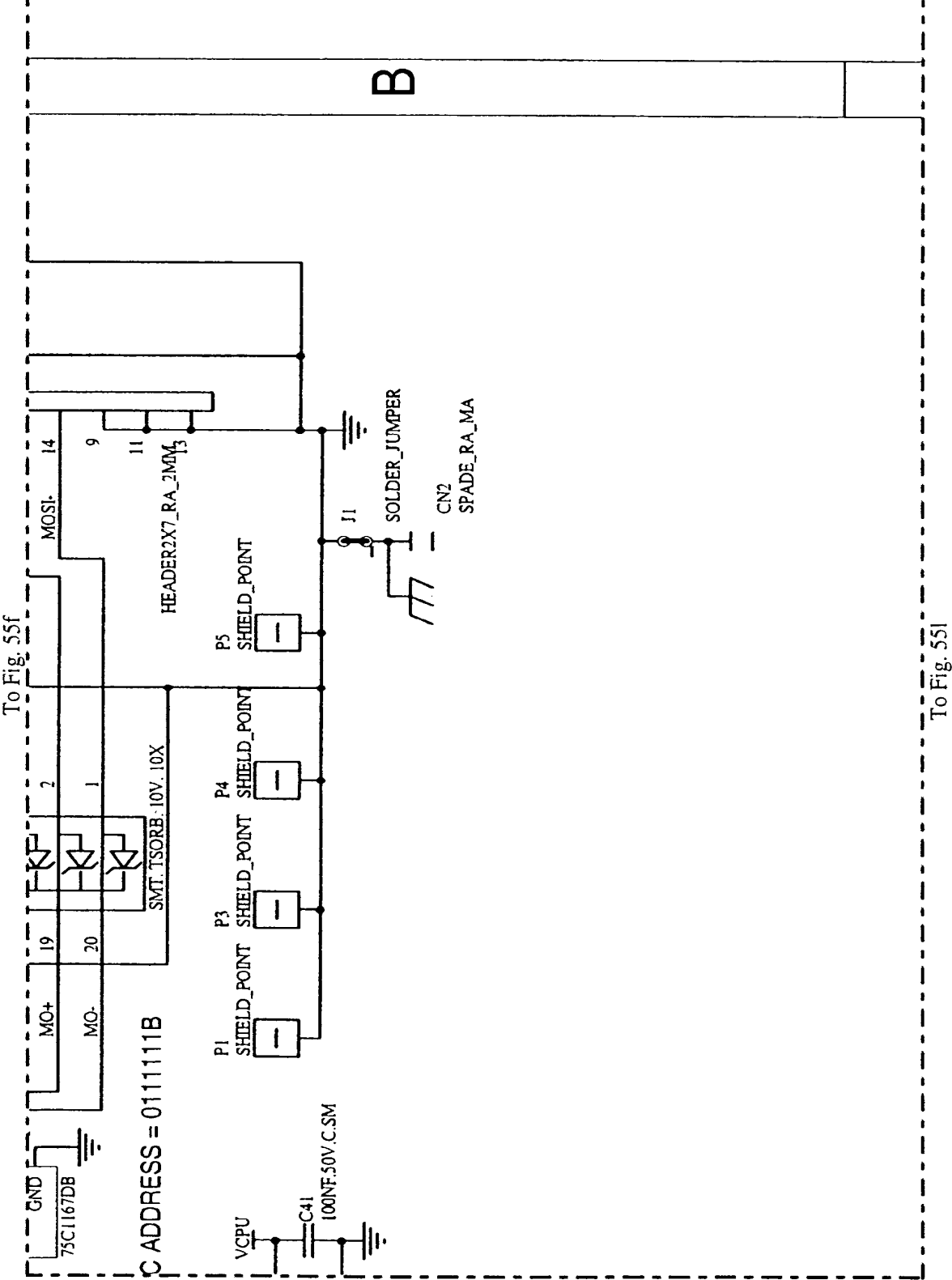
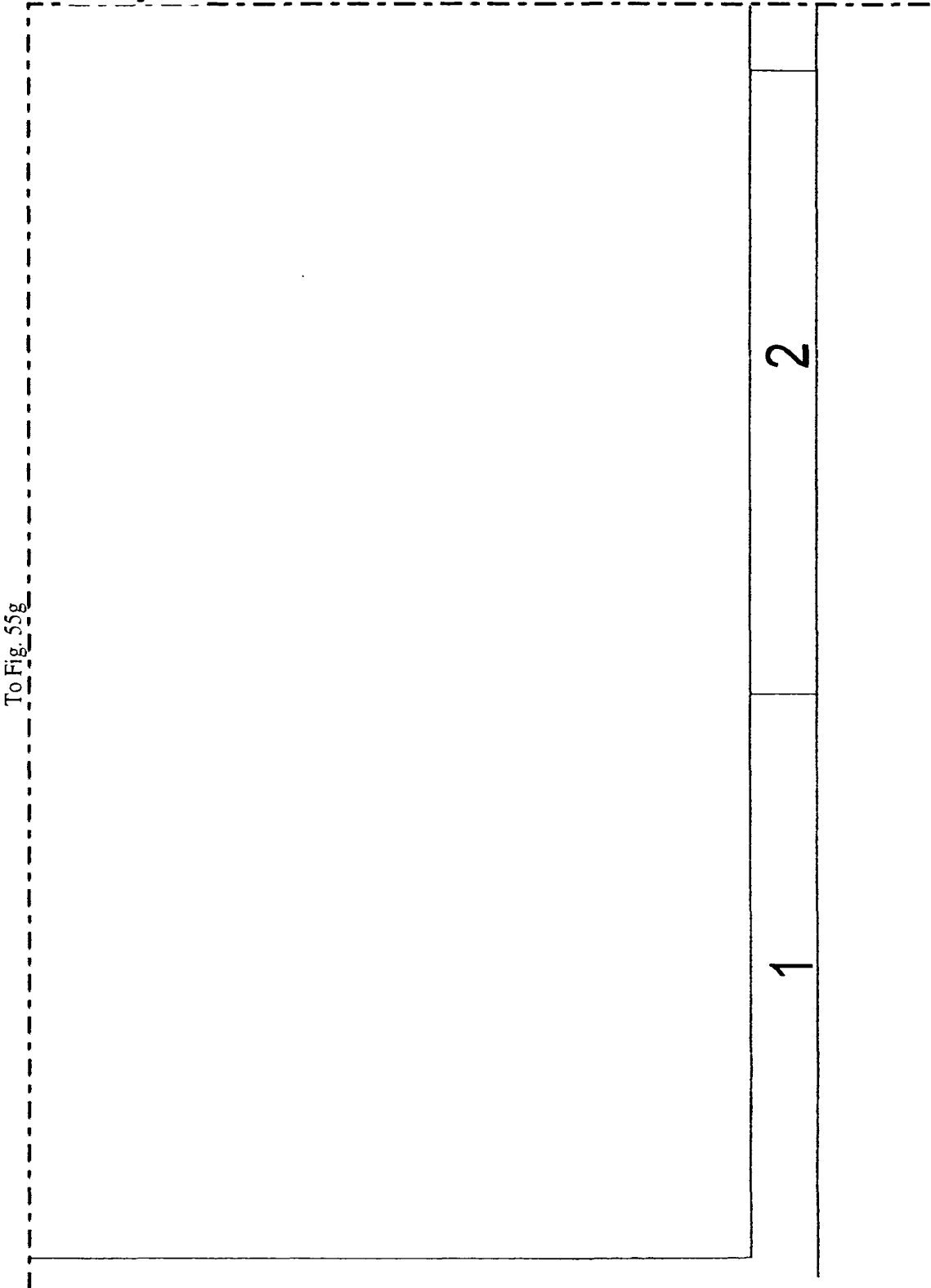


FIG. 55j

To Fig. 55k



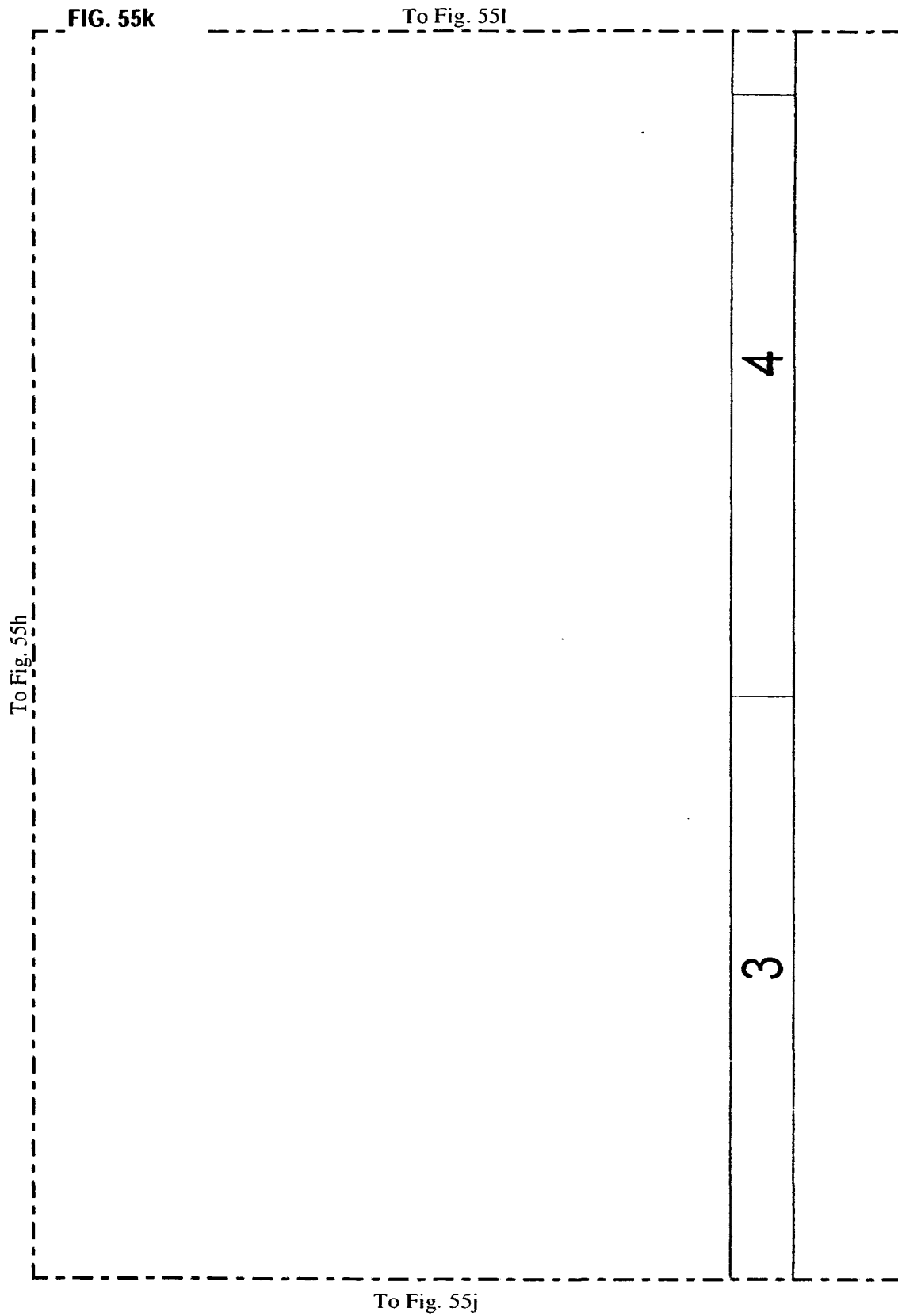


FIG. 55i

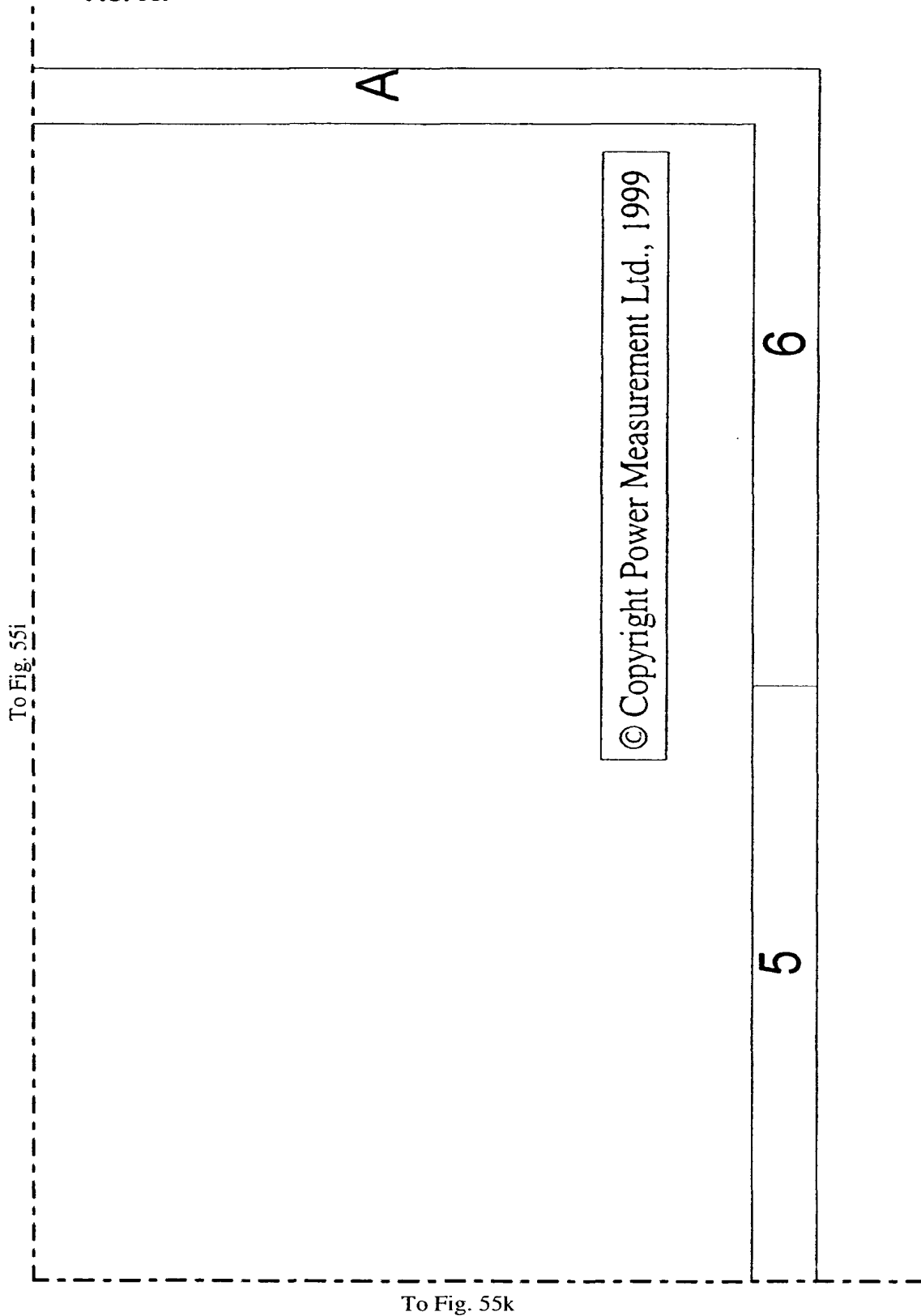


FIG. 56a

To Fig. 56b

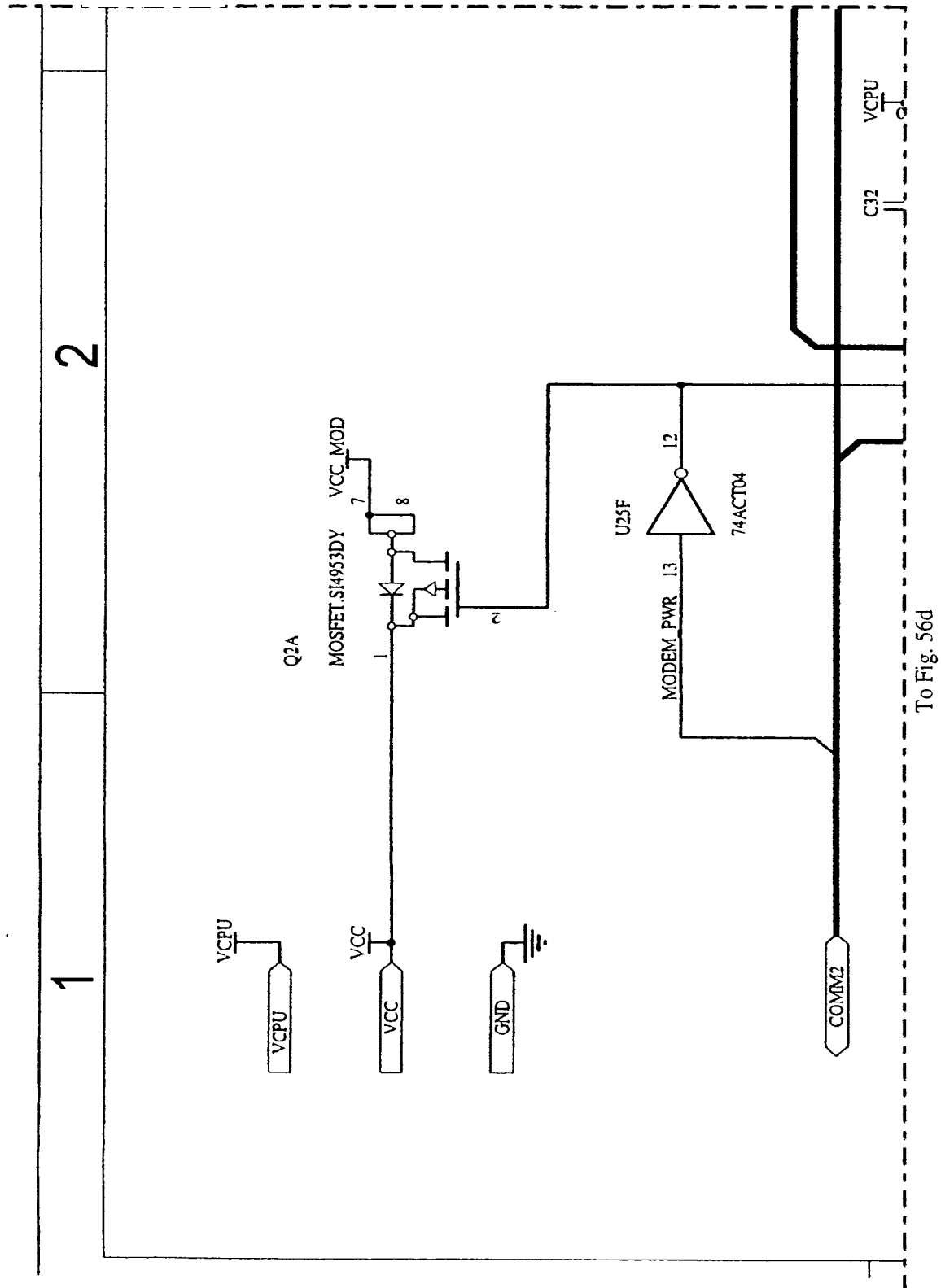
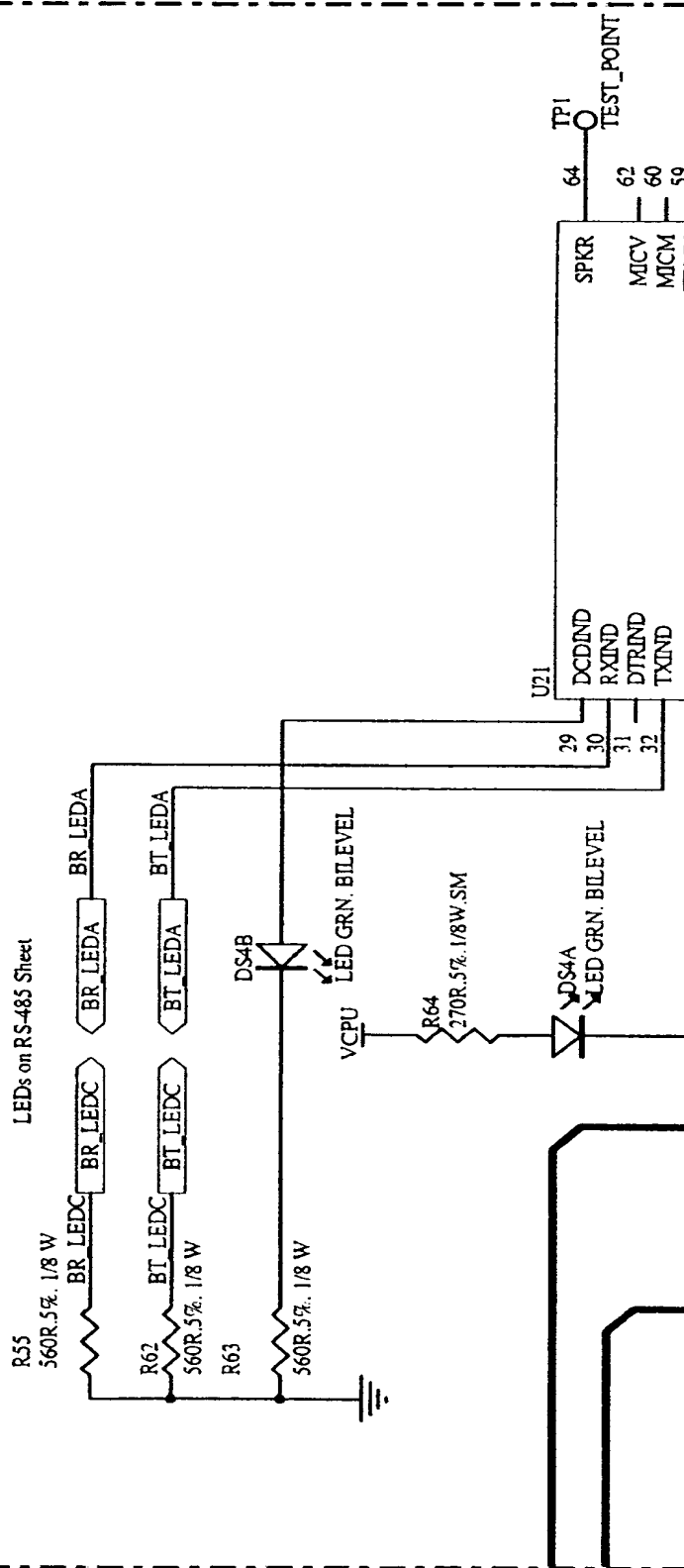


FIG. 56b

To Fig. 56c

4

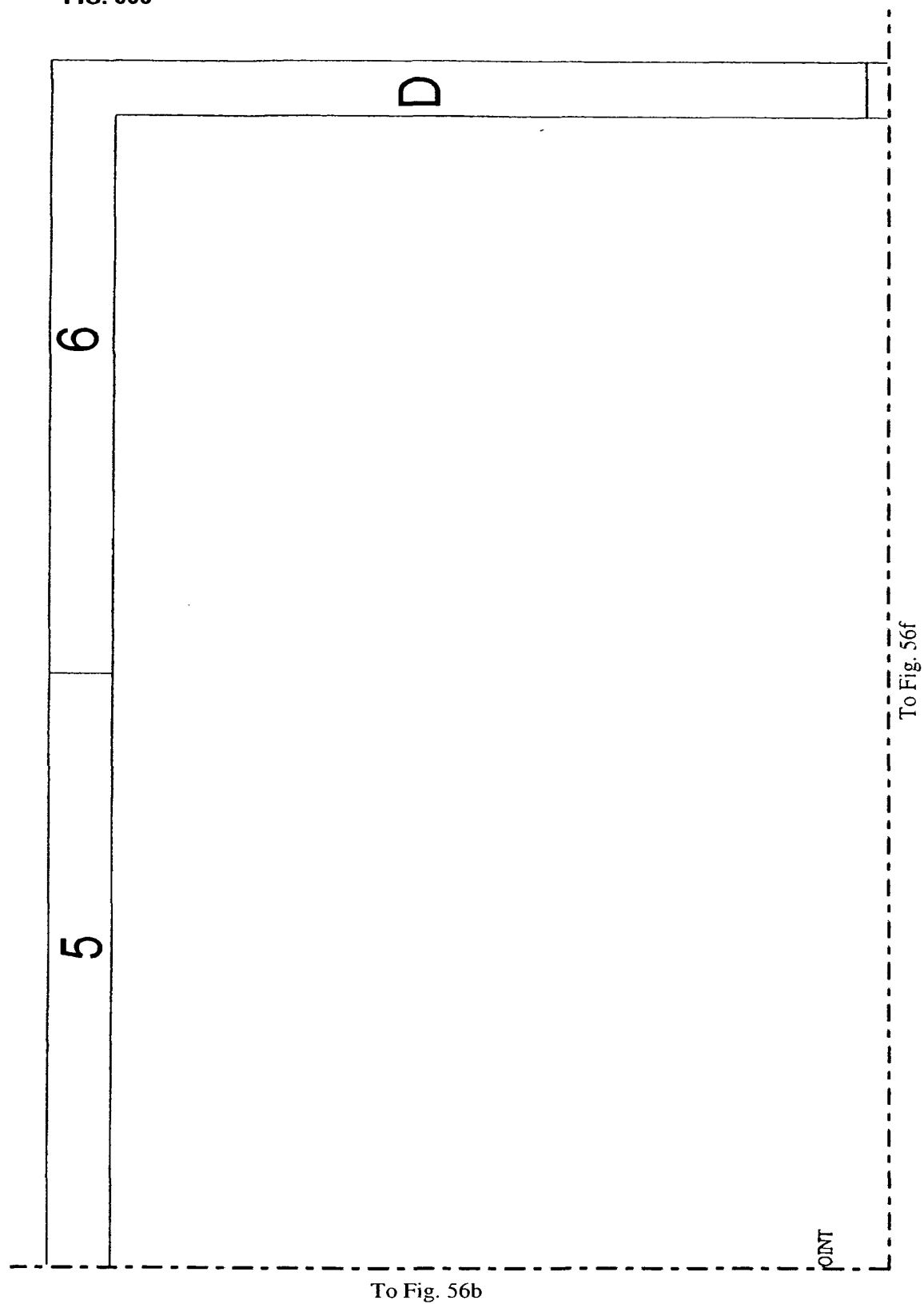
3

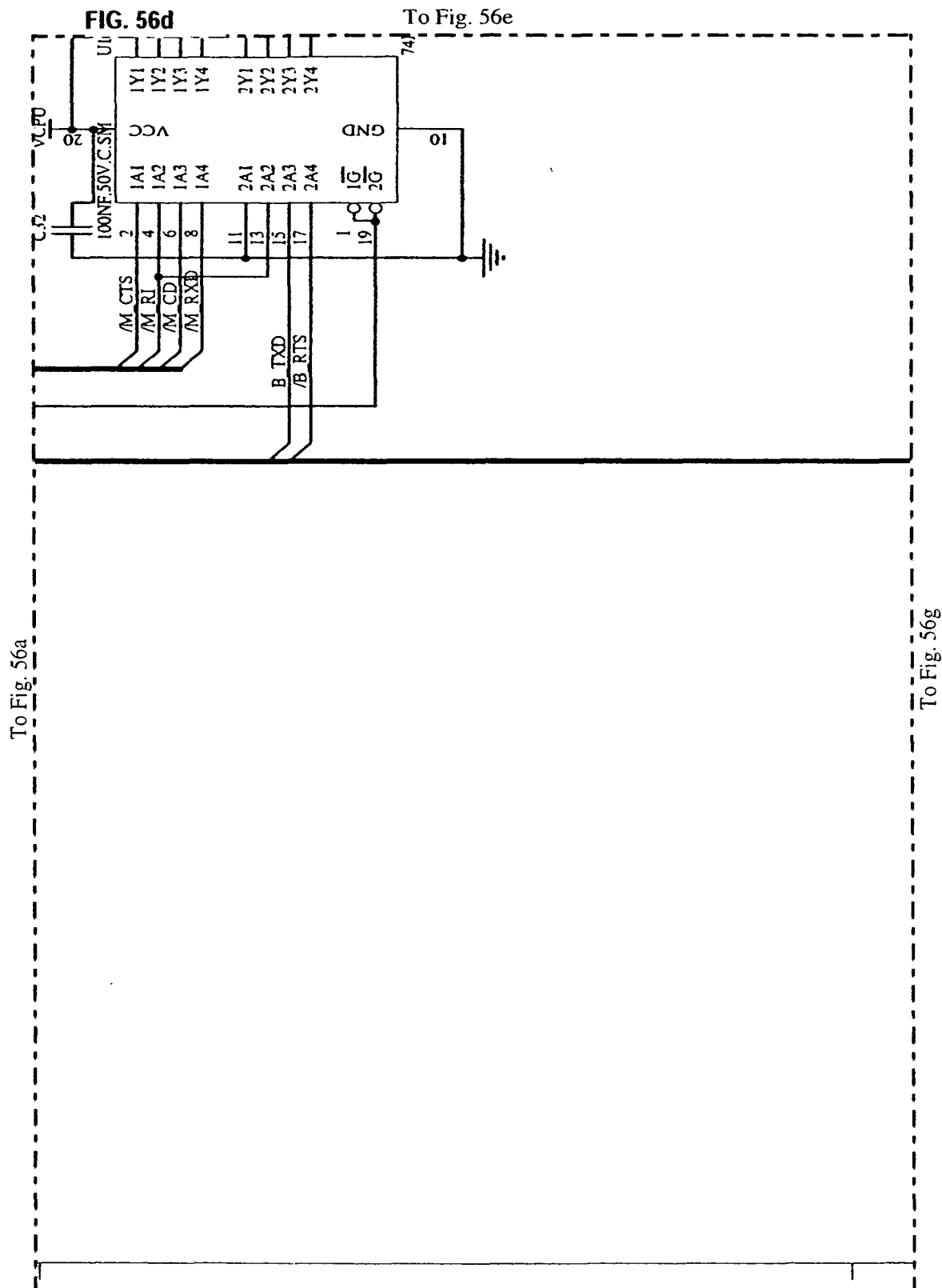


To Fig. 56e

To Fig. 56a

FIG. 56c





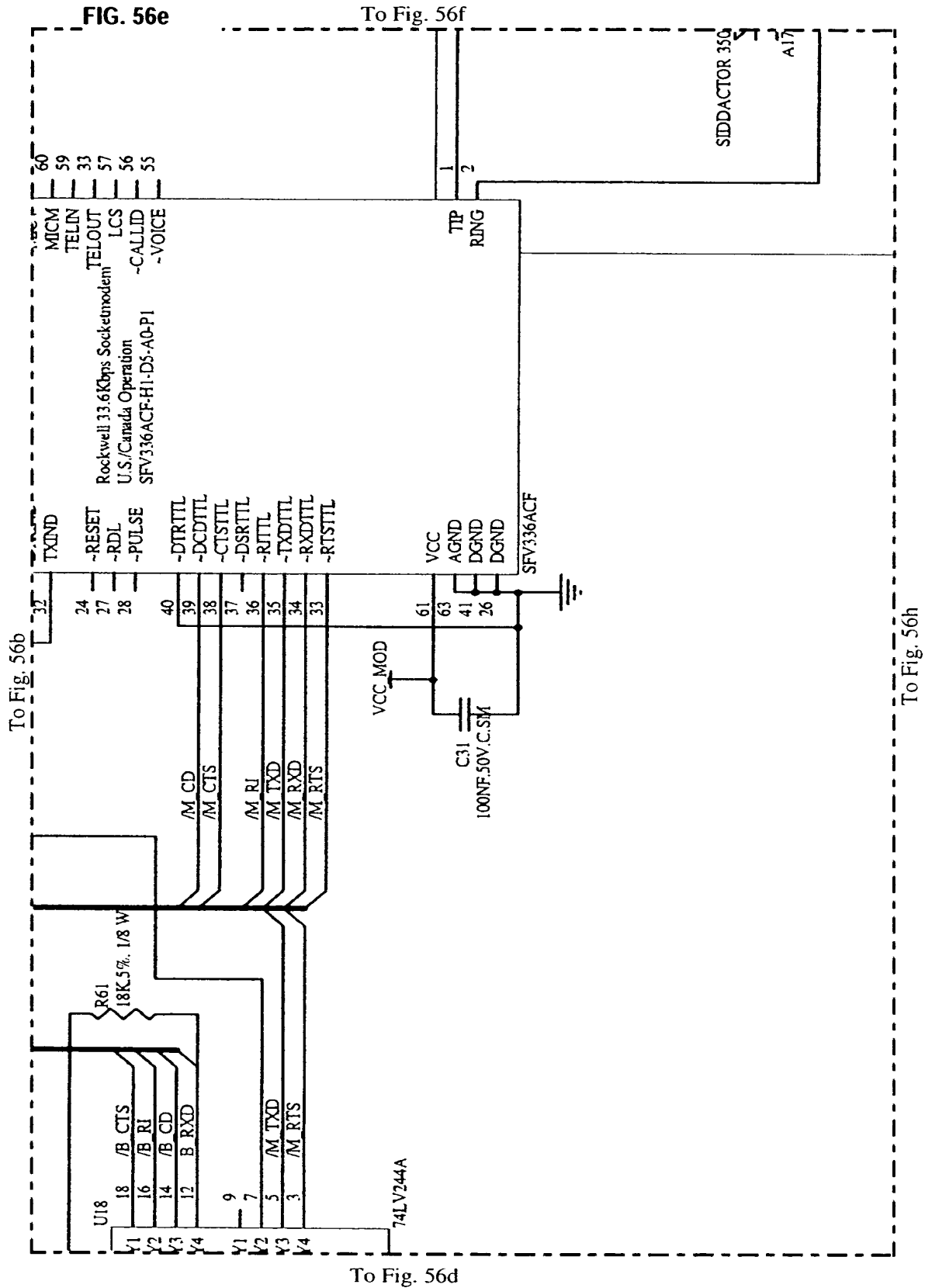


FIG. 56f

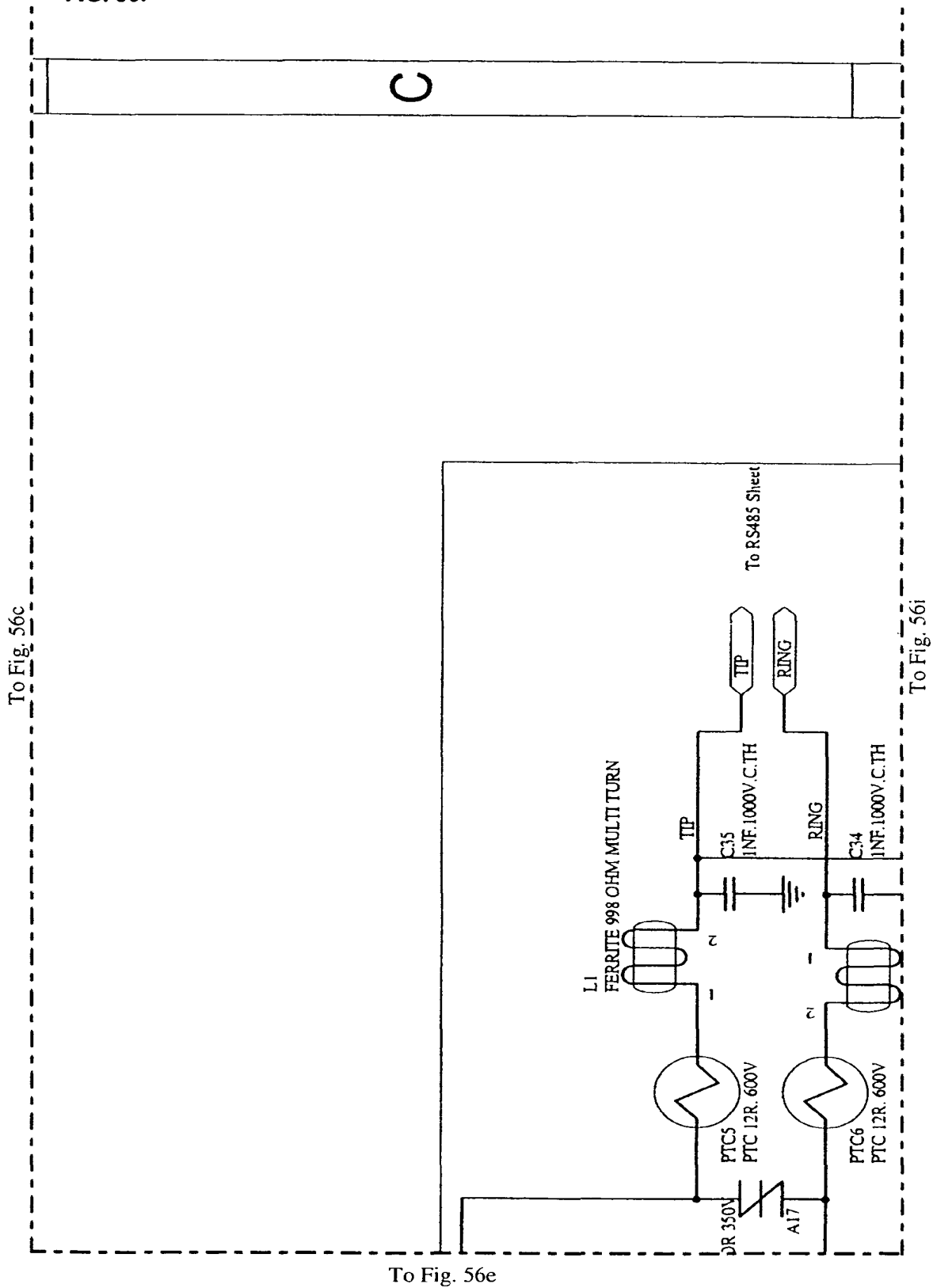


FIG. 56g

To Fig. 56h

LINE DET

To Fig. 56d

To Fig. 56j



To Fig. 56e

To Fig. 56k

To Fig. 56g

FIG. 56i

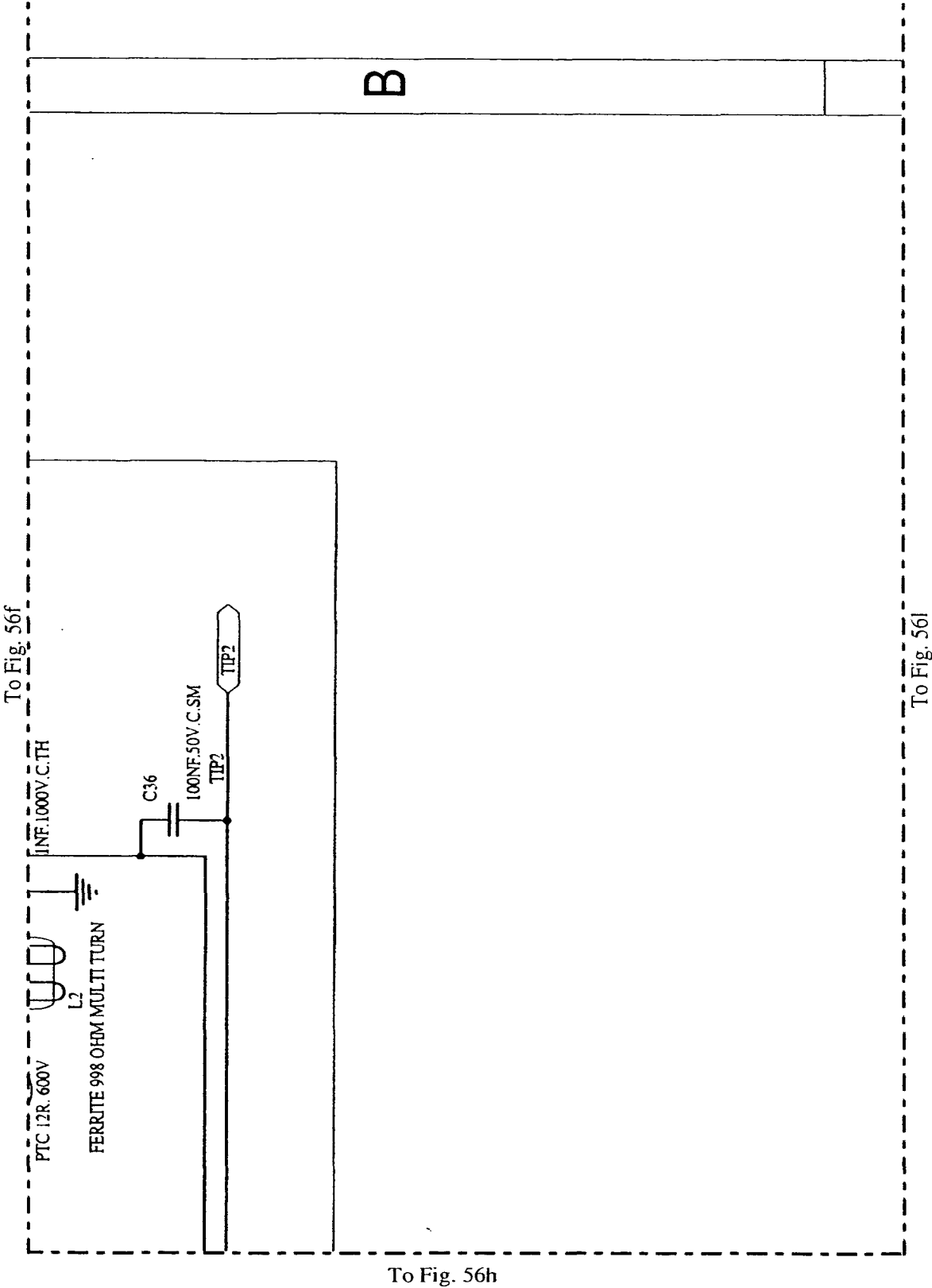


FIG. 56j

To Fig. 56k

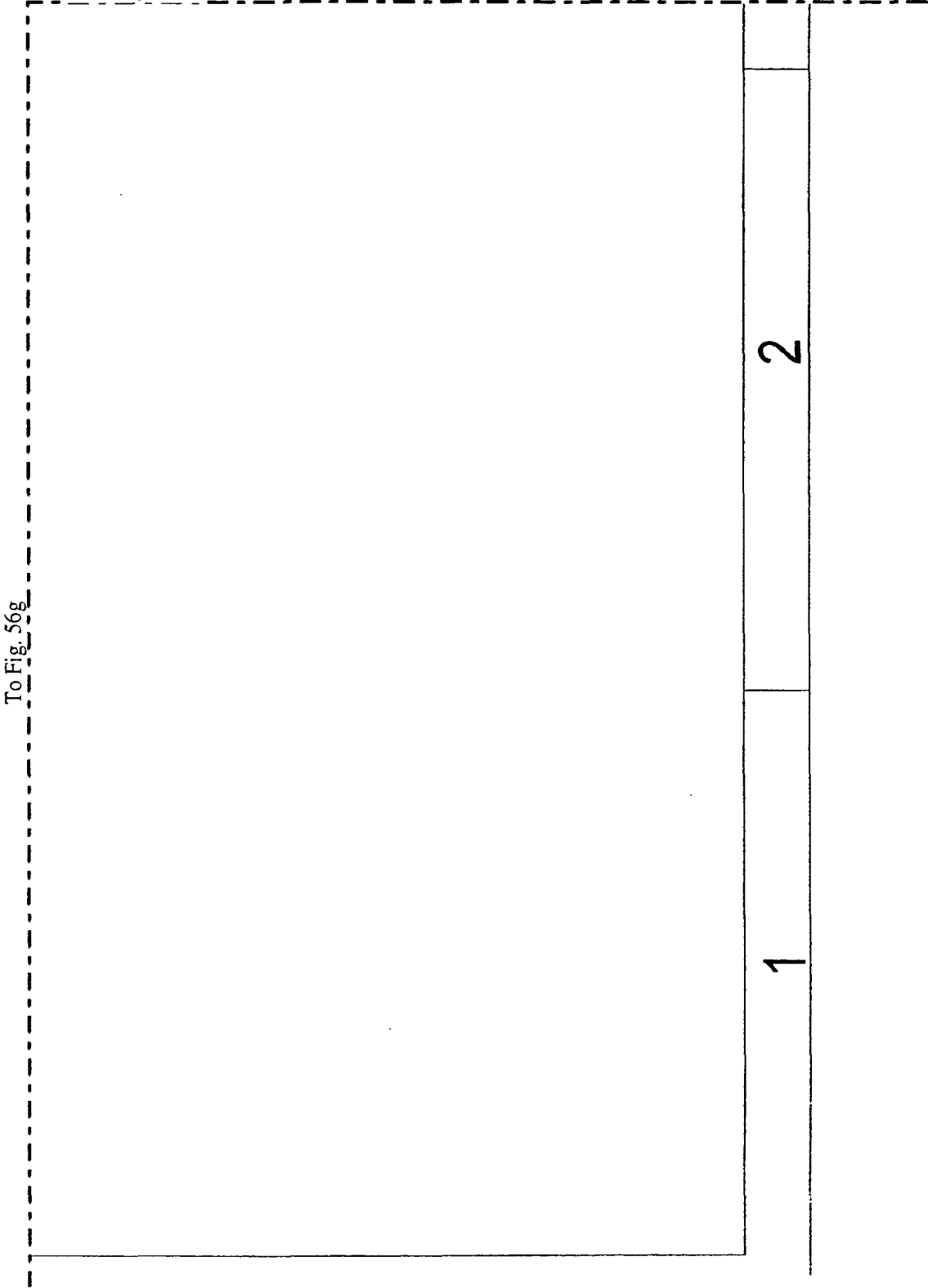


FIG. 56k

To Fig. 56l

To Fig. 56h

4

3

To Fig. 56j

FIG. 56l

